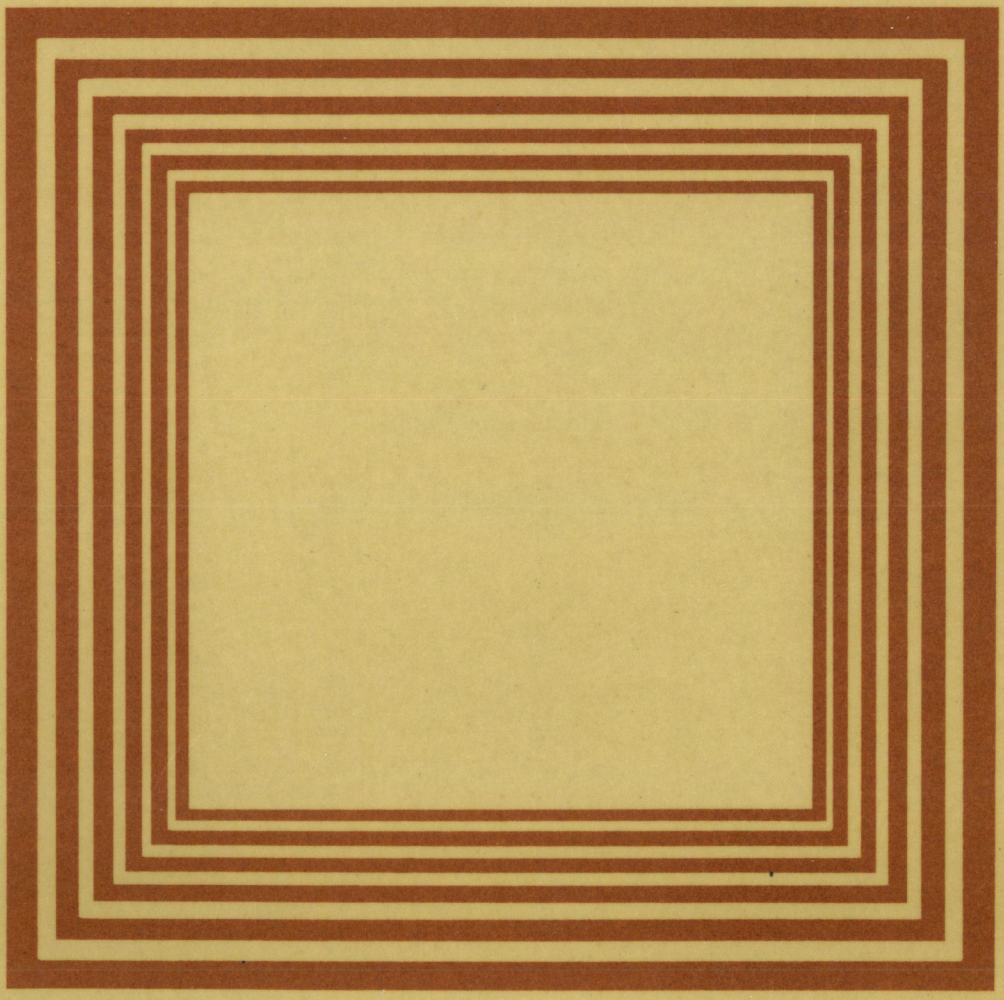
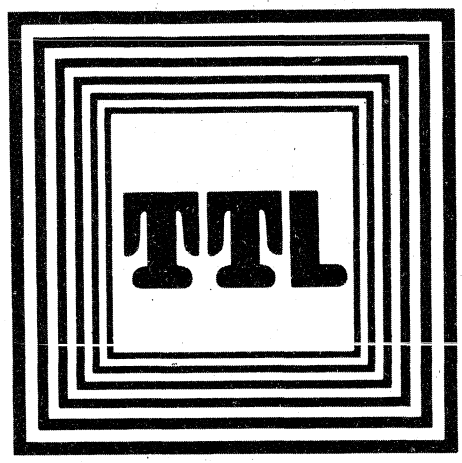
LS TTL

LOW POWER SCHOTTKY



MOTOROLA Semiconductors

LOW POWER SCHOTTKY



MOTOROLA

LOW-POWER SCHOTTKY TTL

Prepared by
Technical Information Center

This book presents technical data for a broad line of low-power Schottky TTL integrated circuits. Complete specifications for the individual circuits are provided in the form of data sheets. In addition, the general characteristics and design considerations of this popular family are discussed, and selection guides are included to simplify the task of choosing the best combination of circuits for a system.

The information in this book has been carefully checked and is believed to be reliable; however, no responsibility is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of microelectronic devices any license under the patent rights of any manufacturer.

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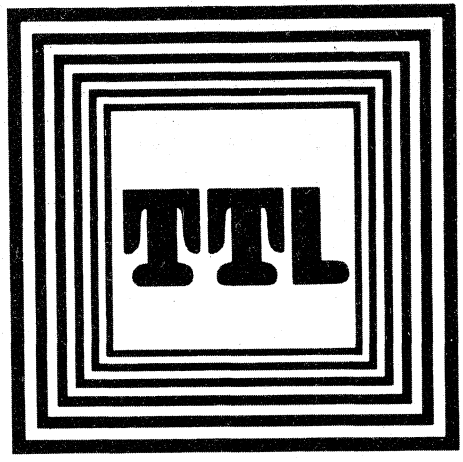
LOW POWER SCHOTTKY



CIRCUIT CHARACTERISTICS

LSTTL circuit features are best understood by examining the LS00 2-input NAND gate *(Figure 1-1)*. The input/output circuits of all LSTTL are almost identical. Although the logic function and basic structure of LS circuits are the same as conventional TTL, there are also significant differences.

INPUT CONFIGURATION. With a few exceptions, LSTTL circuits do not use the multi-emitter input structure that originally gave TTL its name. Most LS elements use a DTL type input circuit with Schottky diodes to perform the AND function, as exemplified by D3 and D4 in *Figure 1-1*. Compared to the classical multi-emitter structure, this circuit is faster and it increases the input breakdown voltage. Inputs of this type are tested for leakage with an applied input voltage of 10 V and the input breakdown voltage is typically 15 V or more. *Figure 1-2* shows the V_{OUT}/V_{IN} transfer function of an LS00 gate. The input threshold is approximately 0.1 V lower than for standard TTL.

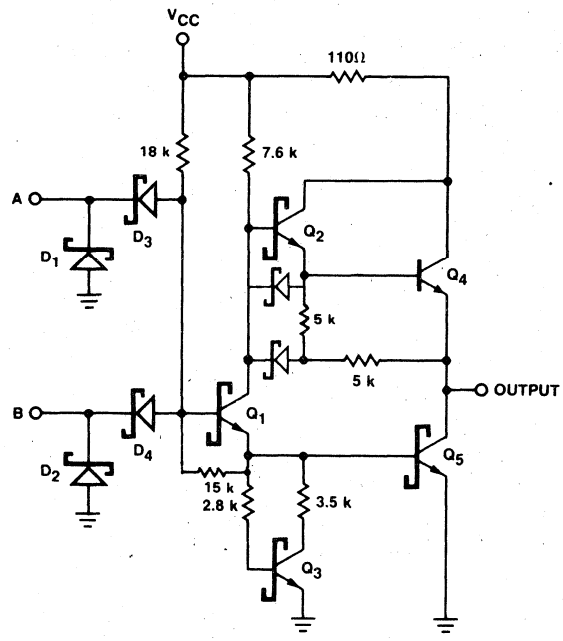


Fig. 1-1
2-INPUT NAND GATE

Another input arrangement often used in MSI has three diodes connected as shown in *Figure 1-3.* This configuration gives a slightly higher input threshold than that of *Figure 1-1.*

A third input configuration that is sometimes used employs a vertical PNP transistor as shown in *Figure 1-4.* This arrangement also gives a higher input threshold and has the additional advantage of reducing the amount of current that the signal source must sink. Both the diode cluster arrangement and the PNP input configuration have breakdown voltage ratings greater than 10 V.

All inputs are provided with clamping diodes, exemplified by D1 and D2 in *Figure 1-1.* These diodes conduct when an input signal goes negative *(Figure 1-5),* which limits undershoot and helps to control ringing on long signal lines following a HIGH-to-LOW transition. These diodes are intended only for the suppression of transient currents and should not be used as steady-state clamps in interface applications. A clamp current exceeding 2 mA and with a duration greater than 500 ns can activate a parasitic lateral NPN transistor, which in turn can steal current from internal nodes of the LS circuit and thus cause logic errors.

The effective capacitance of an LSTTL input is 5 pF for DIP and 4 pF for Flatpak. For an input that serves more than one internal function, each additional function adds 1.5 pF.

OUTPUT CONFIGURATION. The output circuitry of LSTTL have several features not found in conventional TTL. A few of these features are discussed below.

Referring to *Figure 1-1,* the base of the pull-down output transistor Q5 is returned to ground through Q3 and a pair of resistors instead of through a simple resistor. This arrangement is called a squaring network since it squares up the transfer characteristics *(Figure 1-2)* by preventing conduction in the phase splitter Q1 until the input voltage rises high enough to allow Q1 to supply base current to Q5. The squaring network also improves the propagation delay by providing a low resistance path to discharge capacitance at the base of Q5 during turn-off.

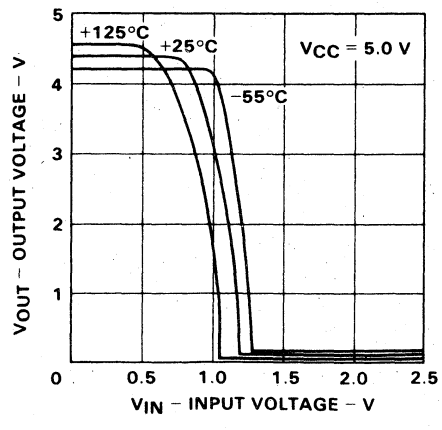


Fig. 1-2
TYPICAL OUTPUT vs
INPUT VOLTAGE CHARACTERISTIC

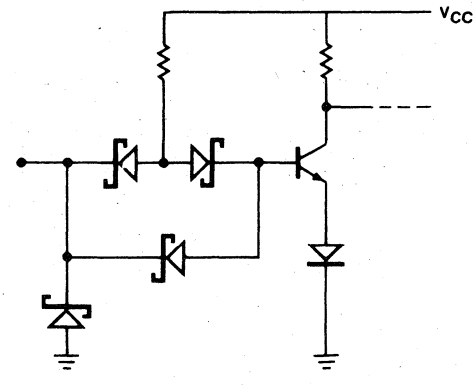


Fig. 1-3
DIODE CLUSTER INPUT

The output pull-up circuit is a 2-transistor Darlington circuit with the base of the output transistor returned through a 5 K resistor to the output terminals, unlike 74H and 74S where it is returned to ground which is a more power consuming configuration. This configuration allows the output to pull up to one V_{BE} below V_{CC} for low values of output current.

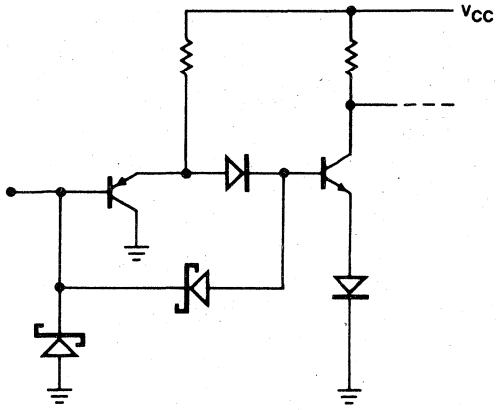


Fig. 1-4
PNP INPUT

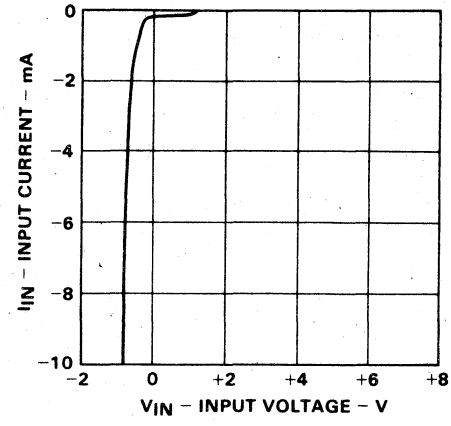


Fig. 1-5
TYPICAL INPUT CURRENT-VOLTAGE CHARACTERISTIC

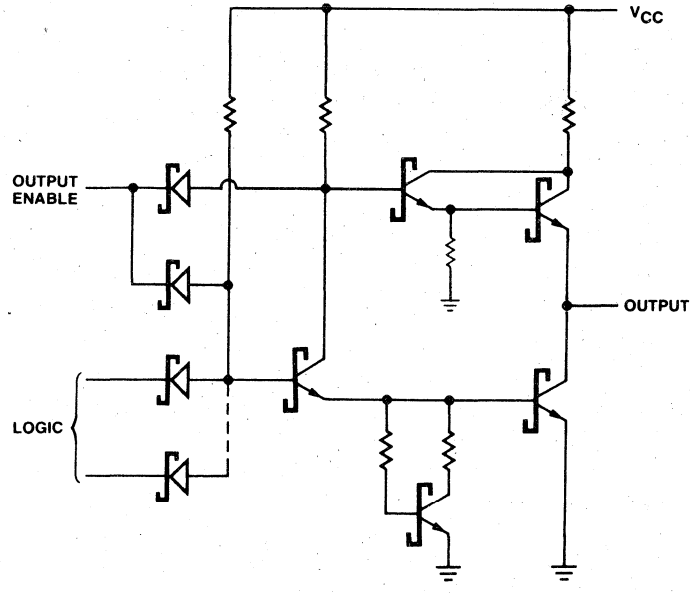


Fig. 1-6
TYPICAL 3-STATE OUTPUT CONTROL

Figure 1-6 shows the extra circuitry used to obtain the "high Z" condition in 3-state outputs. When the Output Enable signal is LOW, both the phase splitter and the Darlington pull-up are turned off. In this condition the output circuitry is non-conducting, which allows the outputs of 2 or more such circuits to be connected together in a bus application wherein only one output is enabled at any particular time.

OUTPUT CHARACTERISTICS. *Figure 1-7* shows the LOW-state output characteristics. For LOW I_{OL} values, the pull-down transistor is clamped out of deep saturation to shorten the turn-off delay. The curves also show the clamping effect when I_{OL} tends to go negative, as it often does due to reflections on a long interconnection after a negative-going transition. This clamping effect helps to minimize ringing.

The waveform of a rising output signal resembles an exponential, except that the signal is slightly rounded at the beginning of the rise. Once past this initial rounded portion, the starting-edge rate is approximately 0.5 V/ns with a 15 pF load and 0.25 V/ns with a 50 pF load. For analytical purposes, the rising waveform can be approximated by the following expression.

$$V(t) = V_{OL} + 3.7\,[1 - \exp(-t/T)]$$

where $T = 8$ ns for $C_L = 15$ pF and 16 ns for $C_L = 50$ pF

The waveform of a falling output signal resembles that part of a cosine wave between angles of 0° and 180°. Fall times from 90% to 10% are approximately 4.5 ns with a 15 pF load and 8.5 ns with a 50 pF load. Equivalent edge rates are approximately 0.8 and 0.4 V/ns respectively. For analytical purposes, the falling waveform can be approximated by the following.

$$V(t) = V_{OL} + 1.9\,\mu(t)\,[1 + \cos \omega t] - 1.9\,\mu(t-a)\,[1 + \cos \omega(t-a)]$$

where $\mu(t) = 0$ for $t < 0$; $= 1$ for $t > 0$ and $\mu(t-a) = 0$ for $t < a$; $= 1$ for $t > a$

For t in nanoseconds and $C_L = 15$ pF, $a = 7.5$ ns, $\omega = 0.42$

For $C_L = 50$ pF, $a = 14$ ns, $\omega = 0..23$

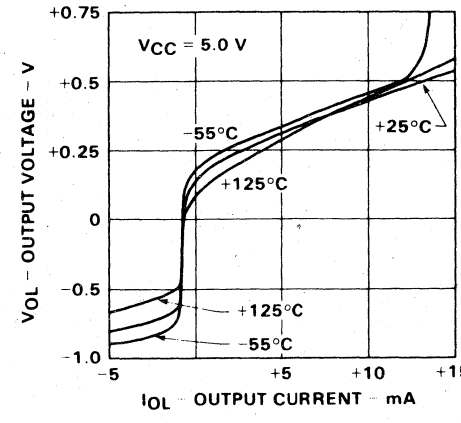


Fig. 1-7 TYPICAL OUTPUT CURRENT-VOLTAGE CHARACTERISTIC

AC SWITCHING CHARACTERISTICS. The average propagation delay of a Low Power Schottky gate is 5 ns at a load of 15 pF as shown in *Figure 1-8.* The delay times increase at an average of 0.08 ns/pF for larger values of capacitance load. These delay times are relatively insensitive to variations in power supply and temperature. The average propagation delay time changes less than 1.0 ns over temperature and less than 0.5 ns with V_{CC} for the military temperature and voltage ranges. (See *Figures 1-10* and *1-11*).

The power versus frequency characteristics of Motorola's LS family, as shown in *Figure 1-9,* indicate that at operating frequencies above 1 MHz the Low Power Schottky devices are more efficient than CMOS for most applications.

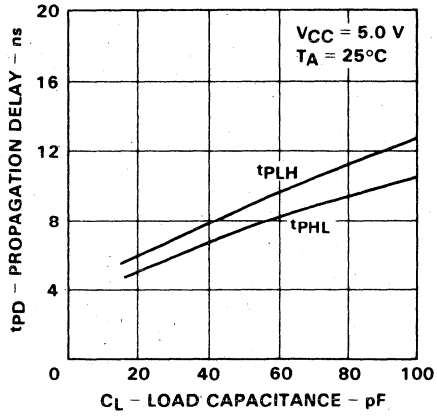


Fig. 1-8

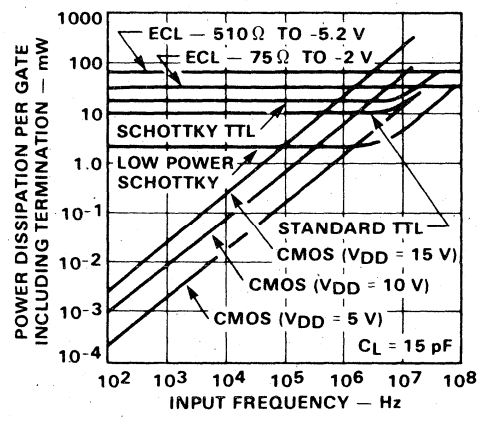


Fig 1-9

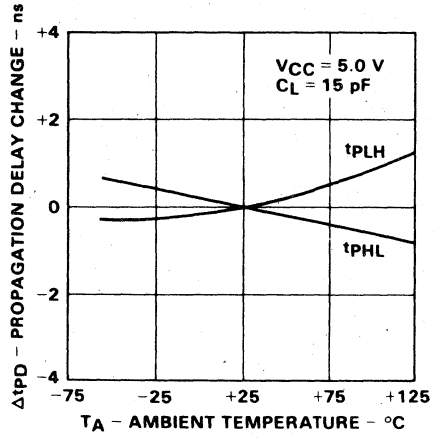


Fig. 1-10

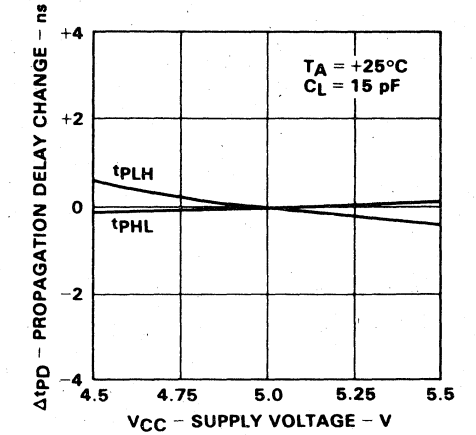


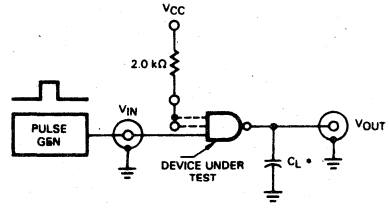
Fig. 1-11

AC WAVEFORMS

AC TEST CIRCUITS AND WAVEFORMS

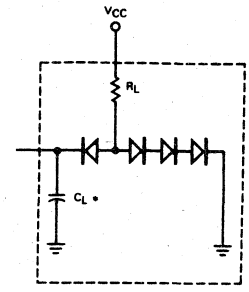
The following test circuits and conditions represent Motorola's typical AC test procedures. The output loading for standard Low Power Schottky devices is a 15 pF capacitor. Experimental evidence shows that test results using the additional diode-resistor load are within 0.2 ns of the capacitor only load. The capacitor only load also has the advantage of repeatable, easily correlated test results. The input pulse rise and fall times are specified at 6 ns to closely approximate the Low Power Schottky output transitions through the active threshold region. The specified propagation delay limits can be guaranteed with a 15 ns input rise time on all parameters except those requiring narrow pulse widths. Any frequency measurement over 15 MHz or pulse width less than 30 ns must be performed with a 6 ns input rise time.

Test Circuit for Standard Output Devices

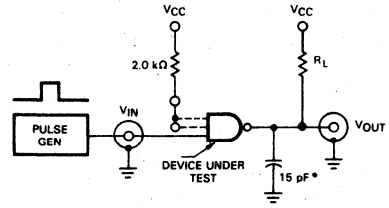


*Includes all probe and jig capacitance

Optional Load (Guaranteed—Not Tested)



Test Circuit for Open Collector Output Devices

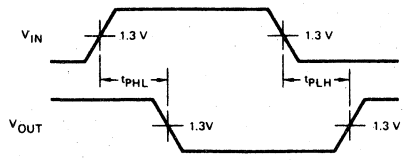


*Includes all probe and jig capacitance

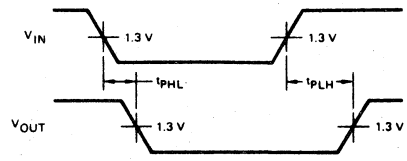
Pulse Generator Settings (unless otherwise specified)

Frequency = 1 MHz
Duty Cycle = 50%
t_{TLH} (t_r) = 6 ns
t_{THL} (t_f) = 6 ns
Amplitude = 0 to 3 V

Waveform for Inverting Outputs



Waveform for Non-inverting Outputs



ABSOLUTE MAXIMUM RATINGS

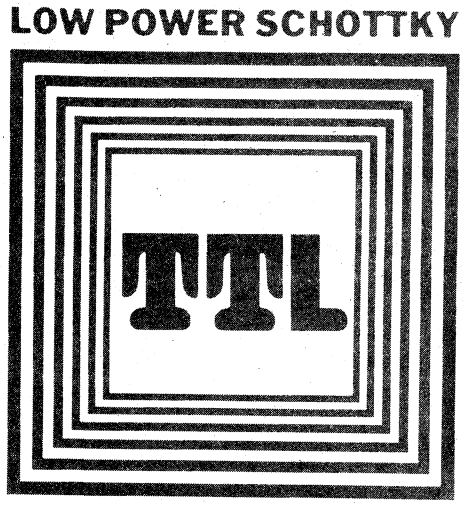
(above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc) Diode Inputs	−0.5 V to 15 V
*Input Current (dc)	−30 mA to +5.0 mA
*Input Voltage (dc) Emitter Inputs	−0.5 V to +5.5 V
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
High Level Voltage Applied to Disabled 3-State Output	7.0 V

*Either input voltage limit or input current limit is sufficient to protect the inputs—Circuits with 5.5V maximum limits are listed below.

Device types having inputs limited to 5.5 V are as follows:

SN74LS196, SN74LS197—Emitter inputs on clock terminals.
SN74LS390/393 —Emitter inputs on clock terminals.
SN74LS242/243, SN74LS245—Inputs connected to outputs.
SN74LS640/641/642/645 —Inputs connected to outputs.



Design Considerations

SUPPLY VOLTAGE AND TEMPERATURE RANGE. The nominal supply voltage (V_{CC}) for all TTL circuits is +5.0 V. Commercial grade parts are guaranteed to perform with a ±5% supply tolerance (±250 mV) over an ambient temperature range of 0°C to 70°C. MIL-grade parts are guaranteed to perform with a ±10% supply tolerance (±500 mV) over an ambient temperature range of −55°C to +125°C.

TTL families may be mixed for optimum system design. The following tables specify the worst case noise immunity in mixed systems.

Worst Case TTL DC Noise Immunity/Noise Margins

Electrical Characteristics

Item	Symbol	TTL Families	Military (−55 to +125°C)				Commercial (0 to 70°C)				Units
			V_{IL}	V_{IH}	V_{OL}	V_{OH}	V_{IL}	V_{IH}	V_{OL}	V_{OH}	
6	TTL	Standard TTL 9000, 54/74	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
7	HTTL	High Speed TTL, 54H/74H	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
8	LPTTL	Low Power TTL, 93L00 (MSI)	0.7	2.0	0.3	2.4	0.8	2.0	0.3	2.4	V
9	STTL	Schottky TTL 54S/74S, 93S00	0.8	2.0	0.5	2.5	0.8	2.0	0.5	2.7	V
10	LSTTL	Low Power Schottky TTL 54LS/74LS	0.7	2.0	0.4	2.5	0.8	2.0	0.5	2.7	V

V_{OL} and V_{OH} are the voltages generated at the output. V_{IL} and V_{IH} are the voltage required at the input to generate the appropriate levels. The numbers given above are guaranteed worst-case values.

LOW Level Noise Margins (Military)

From \ To	TTL	HTTL	LPTTL	STTL	LSTTL	Units
TTL	400	400	300	400	300	mV
HTTL	400	400	300	400	300	mV
LPTTL	500	500	400	500	400	mV
STTL	300	300	200	300	200	mV
LSTTL	400	400	300	400	300	mV

From "V_{OL}" to "V_{IL}"

HIGH Level Noise Margins (Military)

From \ To	TTL	HTTL	LPTTL	STTL	LSTTL	Units
TTL	400	400	400	400	400	mV
HTTL	400	400	400	400	400	mV
LPTTL	400	400	400	400	400	mV
STTL	500	500	500	500	500	mV
LSTTL	500	500	500	500	500	mV

From "V_{OH}" to "V_{IH}"

LOW Level Noise Margins (Commercial)

From \ To	TTL	HTTL	LPTTL	STTL	LSTTL	Units
TTL	400	400	400	400	400	mV
HTTL	400	400	400	400	400	mV
LPTTL	500	500	500	500	500	mV
STTL	300	300	300	300	300	mV
LSTTL	300	300	300	300	300	mV

From "V_{OL}" to V_{IL}"

HIGH Level Noise Margins (Commercial)

From \ To	TTL	HTTL	LPTTL	STTL	LSTTL	Units
TTL	400	400	400	400	400	mV
HTTL	400	400	400	400	400	mV
LPTTL	400	400	400	400	400	mV
STTL	700	700	700	700	700	mV
LSTTL	700	700	700	700	700	mV

From "V_{OH}" to "V_{IH}"

FAN-IN AND FAN-OUT. In order to simplify designing with Motorola TTL devices, the input and output loading parameters of all families are normalized to the following values:

> 1 TTL Unit Load (U.L.) = 40 μA
> in the HIGH state (logic "1")
>
> 1 TTL Unit Load (U.L.) = 1.6 mA
> in the LOW state (logic "0")

Input loading and output drive factors of all products described in this handbook are related to these definitions.

EXAMPLES – INPUT LOAD

1. A 7400 gate, which has a maximum I_{IL} of 1.6 mA and I_{IH} of 40 μA is specified as having an input load factor of 1 U.L. (Also called a fan-in of 1 load.)

2. The 74LS95B which has a value of I_{IL} = 0.8 mA and I_{IH} of 40 μA on the CP terminal, is specified as having an input LOW load factor of

$$\frac{0.8\text{ mA}}{1.6\text{ mA}} \text{ or } 0.5\text{ U.L.}$$

and an input HIGH load factor of

$$\frac{40\ \mu\text{A}}{40\ \mu\text{A}} \text{ or } 1\text{ U.L.}$$

3. The 74LS00 gate which has an I_{IL} of 0.36 mA and an I_{IH} of 20 μA, has an input LOW load factor of

$$\frac{0.36\text{ mA}}{1.6\text{mA}} \text{ or } 0.225\text{ U.L.}$$

(normally rounded to 0.25 U.L.) and an input HIGH load factor of

$$\frac{20\ \mu\text{A}}{40\ \mu\text{A}} \text{ or } 0.5\text{ U.L.}$$

EXAMPLES – OUTPUT DRIVE

1. The output of the 7400 will sink 16 mA in the LOW (logic "0") state and source 800 μA in the HIGH (logic "1") state. The normalized output LOW drive factor is therefore

$$\frac{16\text{ mA}}{1.6\text{ mA}} = 10\text{ U.L.}$$

and the output HIGH drive factor is

$$\frac{800\ \mu\text{A}}{40\ \mu\text{A}} \text{ or } 20\text{ U.L.}$$

2. The output of the 74LS00 will sink 8.0 mA in the LOW state and source 400 μA in the HIGH state. The normalized output LOW drive factor is

$$\frac{8.0\ \text{mA}}{1.6\ \text{mA}} \text{ or } 5\ \text{U.L.}$$

and the output HIGH drive factor is

$$\frac{400\ \mu\text{A}}{40\ \mu\text{A}} \text{ or } 10\ \text{U.L.}$$

Relative load and drive factors for the basic TTL families are given in *Table 1.*

TABLE I

FAMILY	INPUT LOAD		OUTPUT DRIVE	
	HIGH	LOW	HIGH	LOW
74LS00	0.5 U.L.	0.25 U.L.	10 U.L.	5 U.L.
7400	1 U.L.	1 U.L.	20 U.L.	10 U.L.
9000	1 U.L.	1 U.L.	20 U.L.	10 U.L.
74H00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.
74S00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.

Values for MSI devices vary significantly from one element to another. Consult the appropriate data sheet for actual characteristics.

WIRED-OR APPLICATIONS. Certain TTL devices are provided with an "open" collector output to permit the Wired-OR (actually Wired-AND) function. This is achieved by connecting open collector outputs together and adding an external pull-up resistor.

The value of the pull-up resistor is determined by considering the fan-out of the OR tie and the number of devices in the OR tie. The pull-up resistor value is chosen from a range between maximum value (established to maintain the required V_{OH} with all the OR tied outputs HIGH) and a minimum value (established so that the OR tie fan-out is not exceeded when only one output is LOW).

MINIMUM AND MAXIMUM PULL-UP RESISTOR VALUES

$$R_{X(MIN)} = \frac{V_{CC(MAX)} - V_{OL}}{I_{OL} - N_2(\text{LOW}) \bullet 1.6\,\text{mA}} \qquad R_{X(MAX)} = \frac{V_{CC(MIN)} - V_{OH}}{N_1 \bullet I_{OH} + N_2(\text{HIGH}) \bullet 40\ \mu\text{A}}$$

where:

R_X = External Pull-up Resistor
N_1 = Number of Wired-OR Outputs
N_2 = Number of Input Unit Loads (U.L.) being Driven
$I_{OH} = I_{CEX}$ = Output HIGH Leakage Current
I_{OL} = LOW Level Fan-out Current of Driving Element
V_{OL} = Output LOW Voltage Level (0.5 V)
V_{OH} = Output HIGH Voltage Level (2.4 V)
V_{CC} = Power Supply Voltage

Example: Four 74LS03 gate outputs driving four other LS gates or MSI inputs.

$$R_{X(MIN)} = \frac{5.25\ V - 0.5V}{8\ mA - 1.6\ mA} = \frac{4.75\ V}{6.4\ mA} = 742\ \Omega$$

$$R_{X(MAX)} = \frac{4.75\ V - 2.4V}{4 \bullet 100\ \mu A + 2 \bullet 40\ \mu A} = \frac{2.35\ V}{0.48\ mA} = 4.9\ k\Omega$$

where:

N_1	$= 4$
N_2(HIGH)	$= 4 \bullet 0.5$ U.L. $= 2$ U.L.
N_2(LOW)	$= 4 \bullet 0.25$ U.L. $= 1$ U.L.
I_{OH}	$= 100\ \mu A$
I_{OL}	$= 8$ mA
V_{OL}	$= 0.5$ V
V_{OH}	$= 2.4$ V

Any value of pull-up resistor between 742 Ω and 4.9 kΩ can be used. The lower values yield the fastest speeds while the higher values yield the lowest power dissipation.

UNUSED INPUTS. For best noise immunity and switching speed, unused TTL inputs should not be left floating, but should be held between 2.4 V and the absolute maximum input voltage.

Two possible ways of handling unused inputs are:

1. Connect unused input to V_{CC}. Most LSTTL inputs have a breakdown voltage >15 V and require, therefore, no series resistor. For all multi-emitter conventional TTL inputs, a 1-to-10 kΩ current limiting series resistor is recommended, to protect against V_{CC} transients that exceed 5.5 V.

2. Connect the unused input to the output of an unused gate that is forced HIGH.

CAUTION: Do not connect an unused LSTTL input to another input of the same NAND or AND function. This method, recommended for normal TTL, increases the input coupling capacitance and thus reduces the ac noise immunity.

INTERCONNECTION DELAYS. For those parts of a system in which timing is critical, designers should take into account the finite delay along the interconnections. These range from about 0.12 to 0.15 ns/inch for the type of interconnections normally used in TTL systems. Exceptions occur in systems using ground planes with STTL to reduce ground noise during a logic transition; ground planes give higher distributed capacitance and delays of about 0.15 to 0.22 ns/inch.

Most interconnections on a logic board are short enough that the wiring and load capacitance can be treated as a lumped capacitance for purposes of estimating their effect on the propagation delay of the driving circuit. When an interconnection is long enough that its delay is one-fourth to one-half of the signal transition time, the driver output waveform exhibits noticeable slope changes during a transition. This is evidence that during the initial portion of the output voltage transition the driver sees the characteristic impedance of the interconnection (normally 150 Ω to 200 Ω), which for transient conditions appears as a resistor returned to the quiescent voltage existing just before the beginning of the transition. This characteristic impedance forms a voltage divider with the driver output impedance, tending to produce a signal transition having the same rise or fall time as in the no-load condition but with a reduced amplitude. This attenuated signal travels to the far end of the interconnection, which is essentially an unterminated transmission line, where upon the signal starts doubling. Simultaneously, a reflection voltage is generated which has the same amplitude and polarity as the original signal, e.g., if the driver output signal is positive-going the reflection will be positive-going, and as it travels back toward the driver it adds to the line voltage. At the instant the reflection arrives at the driver it adds algebraically to the still-rising driver output, accelerating the transition rate and producing the noticeable change in slope.

If an interconnection is of such length that its delay is longer than half the signal transition time, the attenuated output of the driver has time to reach substantial completion before the reflection arrives. In the limit, the waveform observed at the driver output is a 2-step signal with a pedestal. In this circumstance the first load circuit to receive a full signal is the one at the far end, because of the doubling effect, while the last one to receive a full signal is the one nearest the driver since it must wait for the reflection to complete the transition. Thus, in a worst-case situation, the net contribution to the overall delay is twice the delay of the interconnection because the initial part of the signal must travel to the far end of the line and the reflection must return.

When load circuits are distributed along an interconnection, the input capacitance of each will cause a small reflection having a polarity opposite that of the signal transition, and each capacitance also slows the transition rate of the signal as it passes by. The series of small reflections, arriving back at the driver, is subtractive and has the effect of reducing the apparent amplitude of the signal. The successive slowing of the transition rate of the transmitted signal means that it takes longer for the signal to rise or fall to the threshold level of any particular load circuit. A rough but workable approach is to treat the load capacitances as an increase in the intrinsic distributed capacitance of the interconnection. Increasing the distributed capacitance of a transmission line reduces its impedance and increases its delay. A good approximation for ordinary TTL interconnections is that distributed load capacitance decreases the characteristic impedance by about one-third and increases the delay by one-half.

Another advantage of LSTTL has to do with its output impedance during a positive-going transition. Whereas the low output impedance of STTL and HTTL allows these circuits to force a larger initial swing into a low impedance interconnection, the low output impedance also has a disadvantage. It makes the reflection coefficient negative at the driven end of the interconnection, a circumstance that exists any time a transmission line is terminated by an impedance lower than its characteristic impedance. This means that when the reflection from the (essentially) open end of the interconnection arrives back at the driver it will be re-reflected with the opposite polarity. The result is a sequence of reflected signals which alternate in sign and decrease in magnitude, commonly known as ringing. The lower the driver output impedance, the greater the amplitude of the ringing and the longer it takes to damp out.

The output impedance of LSTTL, on the other hand, is closer to the characteristic impedance of the interconnections commonly used with TTL, and ringing is practically non-existent. Thus no special packaging is required. This advantage, combined with excellent speed, modest edge rates and very low transient currents, are some of the reasons that designers have found LSTTL extremely easy to work with and very cost effective.

DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATABOOK

CURRENTS – Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

I_{CC} **Supply current** – The current flowing into the V_{CC} supply terminal of a circuit with the specified input conditions and the outputs open. When not specified, input conditions are chosen to guarantee worst case operation.

I_{IH} **Input HIGH current** – The current flowing into an input when a specified HIGH voltage is applied.

I_{IL} **Input LOW current** – The current flowing out of an input when a specified LOW voltage is applied.

I_{OH} **Output HIGH current** – The leakage current flowing into a turned off open collector output with a specified HIGH output voltage applied. For devices with a pull-up circuit, the I_{OH} is the current flowing out of an output which is in the HIGH state.

I_{OL} **Output LOW current** – The current flowing into an output which is in the LOW state.

I_{OS} **Output short-circuit current** – The current flowing out of an output which is in the HIGH state when that output is short circuit to ground (or other specified potential).

I_{OZH} **Output off current HIGH** – The current flowing into a disabled 3-state output with a specified HIGH output voltage applied.

I_{OZL} **Output off current LOW** – The current flowing out of a disabled 3-state output with a specified LOW output voltage applied.

VOLTAGES – All voltages are referenced to ground. Negative voltage limits are specified as absolute values (*i.e.*, –10 V is greater than –1.0 V).

V_{CC} **Supply voltage** – The range of power supply voltage over which the device is guaranteed to operate within the specified limits.

$V_{CD(MAX)}$ **Input clamp diode voltage** – The most negative voltage at an input when 18 mA is forced out of that input terminal. This parameter guarantees the integrity of the input diode which is intended to clamp negative ringing at the input terminal.

V_{IH} **Input HIGH voltage** – The range of input voltages that represents a logic HIGH in the system.

$V_{IH(MIN)}$ **Minimum input HIGH voltage** – The minimum allowed input HIGH in a logic system. This value represents the guaranteed input HIGH threshold for the device.

V_{IL} **Input LOW voltage** – The range of input voltages that represents a logic LOW in the system.

$V_{IL(MAX)}$ **Maximum input LOW voltage** – The maximum allowed input LOW in a system. This value represents the guaranteed input LOW threshold for the device.

$V_{OH(MIN)}$ **Output HIGH voltage** – The minimum voltage at an output terminal for the specified output current I_{OH} and at the minimum value of V_{CC}.

$V_{OL(MAX)}$ **Output LOW Voltage** – The maximum voltage at an output terminal sinking the maximum specified load current I_{OL}.

V_{T+} **Positive-going threshold voltage** – The input voltage of a variable threshold device (*i.e.*, Schmitt Trigger) that is interpreted as a V_{IH} as the input transition rises from below $V_{T-(MIN)}$.

V_{T-} **Negative-going threshold voltage** – The input voltage of a variable threshold device (*i.e.*, Schmitt Trigger) that is interpreted as a V_{IL} as the input transition falls from above $V_{T+(MAX)}$.

AC SWITCHING PARAMETERS

f_{MAX} **Toggle frequency/operating frequency** – The maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.

t_{PLH} **Propagation delay time** – The time between the specified reference points, normally 1.3 V on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} **Propagation delay time** – The time between the specified reference points, normally 1.3 V on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.

t_W **Pulse width** – The time between 1.3 V amplitude points on the leading and trailing edges of a pulse.

t_h **Hold time** – The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_s **Set-up time** – The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{PHZ} **Output disable time (of a 3-state output) from HIGH level** – The time between the 1.3 V level on the input and a voltage 0.5 V below the steady state output HIGH level with the 3-state output changing from the defined HIGH level to a high-impedance (off) state.

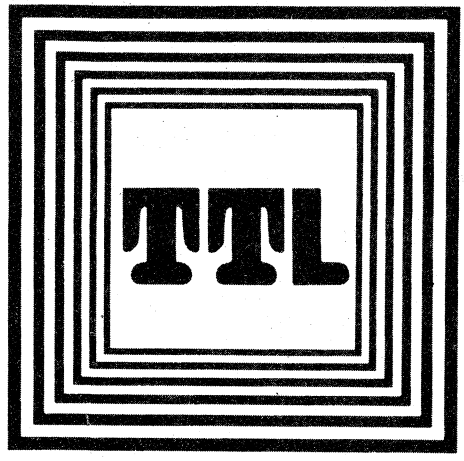
t_{PLZ} **Output disable time (of a 3-state output) from LOW level** – The time between the 1.3 V level on the input and a voltage 0.5 V above the steady state output LOW level with the 3-state output changing from the defined LOW level to a high-impedance (off) state.

t_{PZH} **Output enable time (of a 3-state output) to a HIGH level** – The time between the 1.3 V levels of the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to a HIGH level.

t_{PZL} **Output enable time (of a 3-state output) to a LOW level** – The time between the 1.3 V levels of the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to a LOW level.

t_{rec} **Recovery time** – The time between the 1.3 V level on the trailing edge of an asynchronous input control pulse and the 1.3 V level on a synchronous input (clock) pulse such that the device will respond to the synchronous input.

LOW POWER SCHOTTKY



Selection Information

SSI SELECTOR AND REPLACEMENT GUIDE

Function	Low Power Schottky 5 ns/2 mW	Std. TTL 54/74 10 ns/10 mW	High Speed 54H/74H 6 ns/22 mW	High Speed Schottky 3 ns/19 mW
NAND Gates				
Hex Inverters	54LS/74LS04	54/7404	54H/74H04	54S/74S04
Hex Inverters (o. c.)	54LS/74LS05	54/7405	54H/74H05	54S/74S05
Hex Schmitt Trigger	54LS/74LS14	54/7414		
Quad 2-Input	54LS/74LS00	54/7400	54H/74H00	54S/74S00
Quad 2-Input (o. c.)	54LS/74LS01	54/7401	54H/74H01	
Quad 2-Input (o. c.)	54LS/74LS03	54/7403		54S/74S03
Quad 2-Input (48 mA)	54LS/74LS37	54/7437		
Quad 2-Input (o. c. 48 mA)	54LS/74LS38	54/7438		
Quad 2-Input (o. c. 15 V)	54LS/74LS26			
Quad 2-Input Schmitt	54LS/74LS132	54/74132		54S/74S132
Triple 3-Input (o. c.)	54LS/74LS12	54/7412		
Triple 3-Input	54LS/74LS10	54/7410	54H/74H10	54S/74S10
Dual 4-Input Schmitt	54LS/74LS13	54/7413		
Dual 4-Input	54LS/74LS20	54/7420	54H/74H20	54S/74S20
Dual 4-Input (o. c.)	54LS/74LS22	54/7422	54H/74H22	54S/74S22
Dual 4-Input Buffer	54LS/74LS40	54/7440	54H/74H40	54S/74S40
8-Input	54LS/74LS30	54/7430	54H/74H30	54S/74S30
13-Input	54LS/74LS133			54S/74S133

SSI SELECTOR AND REPLACEMENT GUIDE

Function	Low Power Schottky 5 ns/2 mW	Std. TTL 54/74 10 ns/10 mW	High Speed 54H/74H 6 ns/22 mW	High Speed Schottky 3 ns/19 mW
NOR Gates				
Quad 2-Input	54LS/74LS02	54/7402		54S/74S02
Quad 2-Input Buffer	54LS/74LS28			
Quad 2-Input (o. c.)	54LS/74LS33			
Triple 3-Input	54LS/74LS27	54/7427		
Dual 5-Input	54LS/74LS260			54S/74S260
AND Gates				
Quad 2-Input	54LS/74LS08	54/7408	54H/74H08	54S/74S08
Quad 2-Input (o. c.)	54LS/74LS09	54/7409	54H/74H09	54S/74S09
Triple 3-Input	54LS/74LS11	54/7411	54H/74H11	54S/74S11
Triple 3-Input (o. c.)	54LS/74LS15		54H/74H15	54S/74S15
Dual 4-Input	54LS/74LS21	54/7421	54H/74H21	54S/74S21
OR Gates				
Dual 2-Input	54LS/74LS32	54/7432		54S/74S32
Exclusive OR Gate				
Quad 2-Input	54LS/74LS86	54/7486		54S/74S86
Quad 2-Input	54LS/74LS386			
Quad 2-Input (o. c)	54LS/74LS136			
Exclusive NOR Gate				
Quad 2-Input (o. c.)	54LS/74LS266	9386 (8242)		

SSI SELECTOR AND REPLACEMENT GUIDE

Function	Low Power Schottky 5 ns/2 mW	Std. TTL 54/74 10 ns/10 mW	High Speed 54H/74H 6 ns/22 mW	High Speed Schottky 3 ns/19 mW
AND-OR-INVERT GATES				
Dual 2-2-Input	54LS/74LS51	54/7451	54H/74H51	54S/74S51
2-2-3-3-Input	54LS/74LS54	—	—	—
4-4-Input	54LS/74LS55	—	—	—
BUFFERS (3-STATE)		—	—	—
Quad 3-State LOW Enable	54LS/74LS125A	54/74125	—	—
Quad 3-State HIGH Enable	54LS/74LS126A	54/74126	—	—
Hex Buffer 3-State Common Enable	54LS/74LS365A	—	—	—
Hex Inverting 3-State Common Enable	54LS/74LS366A	—	—	—
Hex Buffer 4-Bit & 2-Bit	54LS/74LS367A	—	—	—
Hex Inverting 4 Bit-&-2 Bit	54LS/74LS368A	—	—	—

SSI SELECTOR AND REPLACEMENT GUIDE

Function	Low Power Schottky 5 ns/2 mW	Std. TTL 54/74 10 ns/10 mW	High Speed 54H/74H 6 ns/22 mW	High Speed Schottky 3 ns/19 mW
DUAL FLIP-FLOPS				
Dual JK	(54LS/74LS73)A	(54/7473)	54H/74H73	
Dual JK	54LS/74LS76A	54/7476	54H/74H76	
Dual JK	54LS/74LS78A		54H/74H78	
Dual JK	54LS/74LS107A	54/74107		
Dual JK	54LS/74LS109A	9024		54S/74S109
Dual JK	54LS/74LS112A			54S/74S112
Dual JK	54LS/74LS113A			54S74S113
Dual JK	54LS/74LS114A			54S/74S114
Dual D	54LS/74LS74A	54/7474	54H/74H74	54S/74S74

MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

Description	Device No.	No. of Inputs		Output Pulse Range	Typ. Power Dissipation
		Positive	Negative		
Dual	54LS/74LS221	1	1	20 ns-70 s	23 mW

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

Description	Device No.	No. of Inputs		Output Pulse Range	Typ. Power Dissipation
		Positive	Negative		
Single	74LS/54LS122	2	2	45 ns-∞	30 mW
Dual	74LS/54LS123	1	1	45 ns-∞	60 mW

MSI SELECTOR GUIDE BY FUNCTION

Counters

A= Asynchronous S = Synchronous

Function	DEVICE NO.	Modulo	Parallel Load	Clock Transition	Max Clock Rate MHz (typ)	Clock to Q Output Delay ns (typ)	Power Dissipation mW (typ)
Asynchronous	54LS/74LS90	2x5		⌐	50	33	45
Asynchronous	54LS/74LS92	2x6		⌐	50	33	45
Asynchronous	54LS/74LS93	2x8		⌐	50	46	45
Asynchronous	54LS/74LS196	2x5	A	⌐	60	48	60
Asynchronous	54LS/74LS197	2x8	A	⌐	70	60	60
Asynchronous	54LS/74LS290	2x5		⌐	50	10	45
Asynchronous	54LS/74LS293	2x8		⌐	50	10	45
Asynchronous	54LS/74LS390	2x5 2x5		⌐	50	10	100
Asynchronous	54LS/74LS393	2x8 2x8		⌐	50	10	100
Asynchronous	54LS/74LS490	2x5 2x5		⌐	50	6	100
Synchronous	54LS/74LS160A	10 Presettable	S	⌐	45	15	95
Synchronous	54LS/74LS161A	16 Presettable	S	⌐	45	15	95
Synchronous	54LS/74LS162A	10 Presettable	S	⌐	45	15	95
Synchronous	54LS/74LS163A	16 Presettable	S	⌐	45	15	95
Up/Down	54LS/74LS168	10 Presettable	S	⌐	32	15	100
Up/Down	54LS/74LS169	16 Presettable	S	⌐	32	15	100
Up/Down	54LS/74LS190	10	A	⌐	40	20	90
Up/Down	54LS/74LS191	16	A	⌐	40	20	90
Up/Down	54LS/74LS192	10	A	⌐	40	30	85
Up/Down	54LS/74LS193	16	A	⌐	40	30	85
Up/Down	54LS/74LS568		S	⌐	35		147
Up/Down	54LS/74LS569		S	⌐	35		147

MSI SELECTOR GUIDE BY FUNCTION

ARITHMETIC OPERATORS

(CLA = Carry Lookahead)

Function	Device No.	Description	No. of Bits	Typical t_{pd} ns	Power Dissipation mW (typ)
Adder	54LS/74LS83A	Full Binary 4-Bit w/Carry	4	15	95
Adder	54LS/74LS283	Full Binary 4-Bit w/Carry	4	15	95
Arithmetic Logic Unit	54LS/74LS181	ALU with External CLA	4	20	105
Carry Lookahead Generator	54LS/74LS182	Carry Lookahead	—	—	—

COMPARATORS

Description	Device No.	Typical Compare Time	Typical Total Power Dissipation
4-Bit Magnitude Comparator	54LS/74LS85	23.5 ns	52 mW

RANDOM-ACCESS READ-WRITE MEMORIES

Description	Device No.	Type of Output	Organization	Typical Address Time
64 Bit Array	54LS/74LS89	o.c.	16 x 4	
64 Bit Array	54LS/74LS189	3-State	16 x 4	
64 Bit Array	54LS/74LS289	o.c.	16 x 4	

CLOCK GENERATOR CIRCUITS

Description	Device No.	Typical Power Dissipation
Dual VCO with Enable	54LS/74LS124	90 mW
Dual Voltage Controlled Osc. with Enable	54LS/74LS326	90 mW
Dual VCO	54LS/74LS325	150 mW
Dual VCO	54LS/74LS327	150 mW
Voltage Controlled Osc. with Enable	54LS/74LS324	90 mW

PARITY GENERATOR/CHECKER

Description	Device No.	Typical Time Delay	Typical Power Dissipation
9-Bit Odd/Even Parity Generator/Checker	54LS/74LS280	31 ns	80 mW

MSI SELECTOR GUIDE BY FUNCTION

DECODER/DEMULTIPLEXERS

Unit Load (UL) = 40 μA HIGH/1.6 mA LOW

Function	Device No.	Address Inputs	Active LOW Enable	Active LOW Outputs	Open Collector Output Voltage	Address Delay ns (typ)	Enable Delay ns (typ)	Power Dissipation mW (typ)	Fan-out (UL)
Dual 1-of-4	54LS/74LS139	2+2	1+1	4+4	—	22	19	34	5
Dual 1-of-4	54LS/74LS155	2	2+2	4+4	—	18	15	30	5
Dual 1-of-4	54LS/74LS156	2	2+2	4+4	5.5 V	33	26	31	5
Dual 1-of-4	54LS/74LS256	2+2	1	4+4	—	30	19	60	5
BCD to 7-Segment	54LS/74LS47	4	—	7	15 V	50	—	35	15
BCD to 7-Segment	54LS/74LS48	4	—	7	5.5 V	50	—	125	4
BCD to 7-Segment	54LS/74LS49	4	—	7	5.5 V	50	—	40	5
BCD to 7-Segment	54LS/74LS247	4	—	7	15 V	50	—	35	15
BCD to 7-Segment	54LS/74LS248	4	—	7	5.5 V	50	—	125	4
BCD to 7-Segment	54LS/74LS249	4	—		5.5 V	50	—	40	5
1-of-8	54LS/74LS259	3	1	8	—	30	19	60	5
1-of-8	54LS/74LS42	3	1	8	—	17	17	35	5
1-of-8	54LS/74LS138	3	3	8	—	22	21	34	5
1-of-10	54LS/74LS42	4(BCD)	—	10	—	17	—	35	5

OPEN-COLLECTOR DISPLAY DECODERS/DRIVERS

Description	Device No.	Output Sink Current	Off-State Output Voltage	Typical Power Dissipation
BCD to Decimal Decoder/Driver	54LS/74LS145	12-80 mA	15 V	35 mW
BCD to Seven Segment Decoder/Driver	54LS/74LS47	12-24 mA	15 V	35 mW
	54LS/74LS48	2-6 mA	5.5 V	125 mW
	54LS/74LS247	12-24 mA	15 V	35 mW
	54LS/74LS248	2-6 mA	5.5 V	125 mW
	54LS/74LS49	4-8 mA	5.5 V	40 mW
	54LS/74LS249	4-8 mA	5.5 V	40 mW

MSI SELECTOR GUIDE BY FUNCTION

LATCHES AND FLIP-FLOPS

Unit Load (UL) = 40 μA HIGH/1.6 mA LOW

Function	Device No.	Data Inputs	Common Clear	Enable/Clock Inputs (Level)	Required Enable/ Clock Pulse Width ns (typ)	Enable/Clock to Q Delay ns (typ)	Data to Q Delay ns (typ)	Power Dissipation mW (typ)
4-Bit RS Latch	54LS/74LS279	4x(RS)	—	—	—	—	14	19
4-Bit D Latch	54LS/74LS75	4xD	—	2(L)	10	15	15	32
4-Bit D Latch	54LS/74LS77	4xD	—	2(L)	10	15	15	32
4-Bit D Latch	54LS/74LS197	4xD	L	1(L)	20	28	24	60
4-Bit D Latch	54LS/74LS375	4xD	—	2(L)	10	15	15	32
8-Bit D Latch	54LS/74LS373	8xD	—	1(H)	10	14	10	120
8-Bit D Latch	54LS/74LS573	8xD	—	1(H)	10	14	10	120
Dual 4-Bit Addressable Latch	54LS/74LS256	1xD	L	1(L) 2 Add Bits	11	18	28	70
8-Bit Addressable Latch	54LS/74LS259	1xD	L	1(L) 3 Add Bits	11	18	28	70
4-Bit D Flip-Flop	54LS/74LS175	4xD	L	1(⌐)	20	21	—	55
4-Bit D Flip-Flop	54LS/74LS298	4x2	—	1(¬)	20	20	—	65
4-Bit D Flip-Flop	54LS/74LS174	6	L	1(⌐)	20	21	—	80
4x4 Register File	54LS/74LS170	4xD	—	2	25	—	26	125
4x4 Register File (3-State)	54LS/74LS670	4xD	—	2	25	—	24	150
Quad D Flip-Flop	54LS/74LS379	4xD	—	1(⌐)	20	21	—	—
Hex D Flip-Flop	54LS/74LS378	6xD	—	1(⌐)	20	21	—	—
Octal D Flip-Flop	54LS/74LS377	8xD	—	1(⌐)	20	21	—	—
Octal D Flip-Flop	54LS/74LS273	3xD	L	1(⌐)	15	17	—	85
Octal D Flip-Flop	54LS/74LS374	8xD	—	1(⌐)	12	22	—	135
Octal D Flip-Flop	54LS/74LS574	8xD	—	1(⌐)	12	22	—	135

MICROPROCESSOR SUPPORT FUNCTIONS

Description	Device No.	Typical Power Dissipation	Output
Transceivers and Bus Drivers	54LS/74LS240	98 mW	Inverting 3-State
	54LS/74LS241	100 mW	Non-Inverting 3-State
	54LS/74LS242	128 mW	Inverting 3-State
	54LS/74LS243	128 mW	Non-Inverting 3-State
	54LS/74LS244	100 mW	Non-Inverting 3-State
	54LS/74LS245	207 mW	Non-Inverting 3-State
	54LS/74LS540	98 mW	Inverting 3-State
	54LS/74LS541	100 mW	Non-Inverting 3-State
	54LS/74LS640		Inverting 3-State
	54LS/74LS642		Non-Inverting 3-State
	54LS/74LS641		Non-Inverting 3-State
	54LS/74LS645		Non-Inverting 3-State

MSI SELECTOR GUIDE BY FUNCTION

MULTIPLEXERS

Unit Load (UL) = 40 μA HIGH/1.6 mA LOW

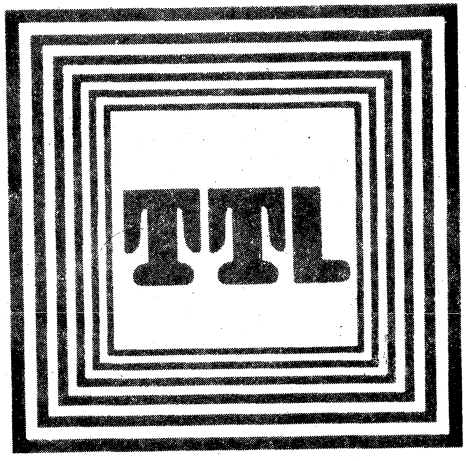
Function	Device No.	Enable Inputs	True Output	Complement Output	Select Delay ns (typ)	Enable Delay ns (typ)	Data Delay ns (typ)	Power Dissipation mW (typ)	Fan-Out (UL)
Quad 2-Input	54LS/74LS157	1	x	—	18	14	9	49	5
Quad 2-Input	54LS/74LS158	1	—	x	16	12	7	24	5
Quad 2-Input	54LS/74LS257A	1	3-State	—	14	16	12	50	5
Quad 2-Input	54LS/74LS258A	1	—	3-State	12	16	10	35	5
Quad 2-Input	54LS/74LS298	Clocked (edge-trigger)	x Latched	—	—	20	—	65	5
Quad 2-Input	54LS/74LS398	Clocked (edge-trigger)	x Latched	x Latched	—	20	—	37	5
Quad 2-Input	54LS/74LS399	Clocked (edge-trigger)	x Latched	—	—	20	—	37	5
Dual 4-Input	54LS/74LS153	2	x	—	18	16	10	31	5
Dual 4-Input	54LS/74LS253	2	3-State	—	18	16	10	43	5
Dual 4-Input	54LS/74LS352	2	—	x	17	15	8	30	5
Dual 4-Input	54LS/74LS353	2	—	3-State	20	12	10	43	5
8-Input	54LS/74LS151	1	x	x	28	25	18	30	5
8-Input	54LS/74LS251	1	3-State	3-State	29	21	18	33	5

MSI SELECTOR GUIDE BY FUNCTION

REGISTERS
A = Asynchronous, S= Synchronous

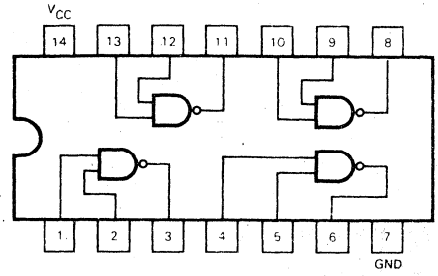
Function	Device No.	No. of Bits	Serial Entry	Parallel Entry No. of Bits	Clock Edge	Max Clock Freq MHz (typ)	Clock to Output Delay ns (typ)	Power Dissipation mW (typ)
Parallel-In/Parallel-out Shift Right	54LS/74LS95B	4	D	4S	⌜	36	20	65
Parallel-in/Parallel-out Shift Right	54LS/74LS195A	4	J, K	4S	⌟	39	17	70
Parallel-in/Parallel-out Shift Right	54LS/74LS295A	4	D	4S	⌟	28	40	75
Parallel-in/Parallel-out Shift Right	54LS/74LS395A	4	D	4S	—	45	20	95
Parallel-in/Parallel-out Bi-Directional	54LS/74LS194A	4	DR, DL	4S	⌟	36	16	75
Parallel-in/Parallel-out Bi-Directional	54LS/74LS299	8	D	8S	⌟	40	15	175
Parallel-in/Parallel-out Bi-Directional	54LS/74LS323	8	D	8S	⌟	40	15	175
Serial-in/Parallel-out	54LS/74LS164	8	2D	—	⌟	18	50	95
Serial-in/Parallel-out	54LS/74LS502	8	D	—	⌟	25	18	325
Parallel-in/Parallel-out	54LS/74LS174	6	—	6S	⌟	40	21	65
Parallel-in/Parallel-out	54LS/74LS175	4	—	4S	⌟	40	21	45
Parallel-in/Parallel-out	54LS/74LS298	4	—	2D MUX	⌜	30	21	65
Parallel-in/Parallel-out	54LS/74LS273	8	—	8S	⌟	45	18	85
Parallel-in/Parallel-out	54LS/74LS374	8	—	8S	⌟	55	20	135
Parallel-in/Parallel-out	54LS/74LS377	8	—	8S	⌟	45	18	85
Parallel-in/Parallel-out	54LS/74LS378	6	—	6S	⌟	45	20	65
Parallel-in/Parallel-out	54LS/74LS379	4	—	4S	⌟	45	15	75
Parallel-in/Parallel-out	54LS/74LS398	4	—	2D MUX	⌟	35	20	37
Parallel-in/Parallel-out	54LS/74LS399	4	—	2D MUX	⌟	35	20	37
Parallel-in/Parallel-out	54LS/74LS574	8	—	8S	⌟	55	20	135
Multiport Registers	54LS/74LS170	16	—	4A	⌜	—	25	125
Multiport Registers	54LS/74LS670	16	—	4A	⌜	—	30	150
Successive Approximation Register	54LS/74LS502	8	D	—	⌟	25	18	325
Parallel-in/Serial-out	54LS/74LS165	8	D	—	—	35	—	105
	OTHER REGISTERS							
D-Register	54LS/74LS173	4	—	—	—	50	—	85

LOW POWER SCHOTTKY



Data Sheets

QUAD 2-INPUT NAND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS00X	4.5 V	5.0 V	5.5 V	55°C to 125°C
SN74LS00X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

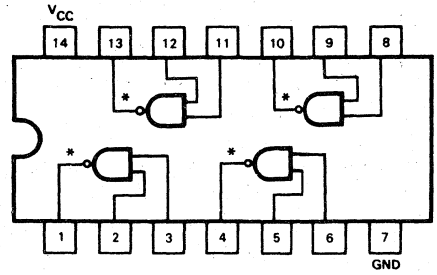
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			-0.65	-1.5	V	V_{CC} = MIN, I_{IN} = -18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = -400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				-0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-15		-100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.8	1.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			2.4	4.4	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		5.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		5.0	10	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

QUAD 2-INPUT NAND GATE



*OPEN COLLECTOR OUTPUTS

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS01X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS01X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

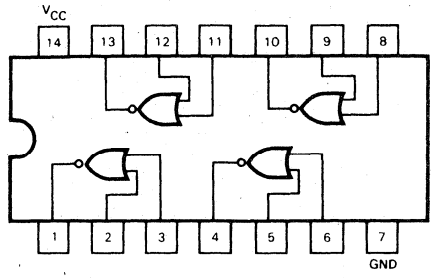
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 10 V, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			0.8	1.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			2.4	4.4	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	18	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

QUAD 2-INPUT NOR GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS02X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS02X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

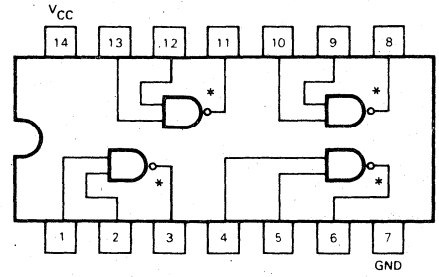
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			1.6	3.2	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			2.4	5.4	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		5.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		5.0	10	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

QUAD 2-INPUT NAND GATE



*OPEN COLLECTOR OUTPUTS

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS03X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS03X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

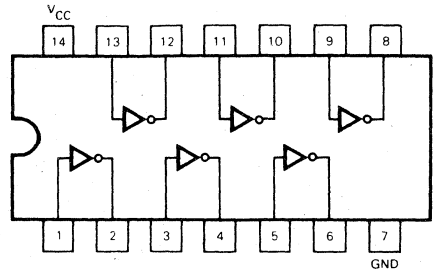
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			0.8	1.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			2.4	4.4	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	18	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

HEX INVERTER



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS04X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS04X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

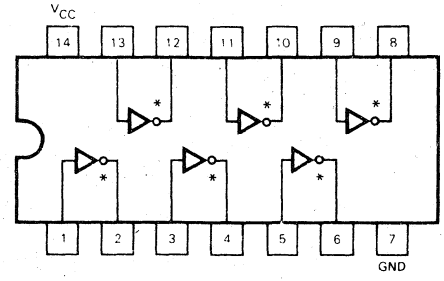
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			1.2	2.4	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			3.6	6.6	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		5.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		5.0	10	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

HEX INVERTER



*OPEN COLLECTOR OUTPUTS

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS05X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS05X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

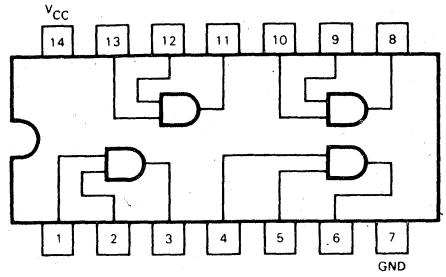
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			1.2	2.4	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			3.6	6.6	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	18	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

QUAD 2-INPUT AND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS08X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS08X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

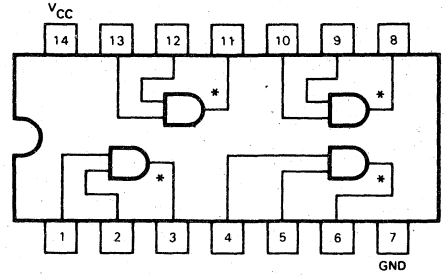
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			2.4	4.8	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			4.4	8.8	mA	V_{CC} = MAX, V_{IN} = 0 V

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		8.0	11	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		7.5	13	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

QUAD 2-INPUT AND GATE (WITH OPEN-COLLECTOR OUTPUT)



*Open Collector Outputs

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS09X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS09X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

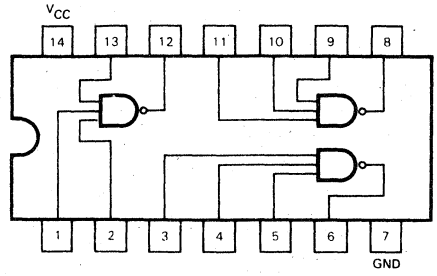
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IH}
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			2.4	4.8	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			4.4	8.8	mA	V_{CC} = MAX, V_{IN} = 0 V

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		13	20	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

TRIPLE 3-INPUT NAND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS10X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS10X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type: W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

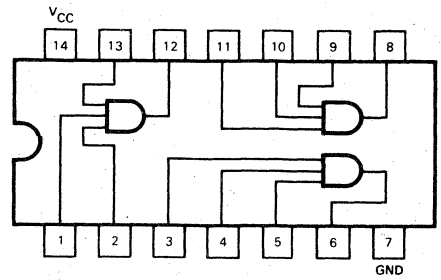
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.6	1.2	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			1.8	3.3	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		6.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		6.0	10	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

TRIPLE 3-INPUT AND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS11X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS11X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

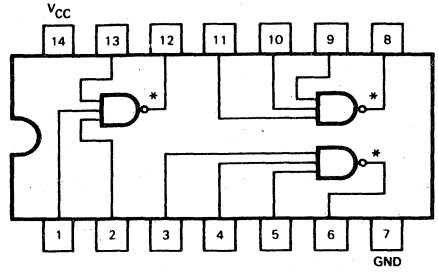
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			1.8	3.6	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			3.3	6.6	mA	V_{CC} = MAX, V_{IN} = 0 V

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		8.5	11	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		7.5	13	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

TRIPLE 3-INPUT NAND GATE



*OPEN COLLECTOR OUTPUTS

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS12X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS12X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IH}
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			1.8	3.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			3.3	6.6	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	4.0	8.5	13	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	7.5	11	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

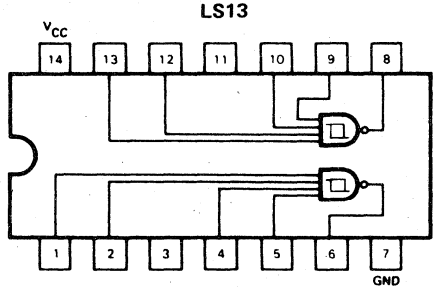
SCHMITT TRIGGERS – DUAL GATE/HEX INVERTER

DESCRIPTION – The LS13 and LS14 contain logic gates/inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional inverters.

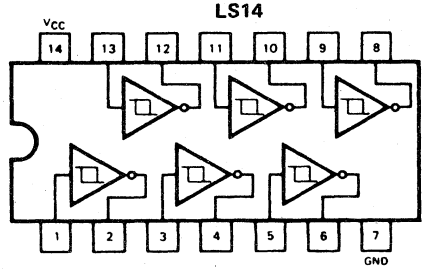
Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

LOGIC AND CONNECTION DIAGRAMS

LS13



LS14



VIN VERSUS VOUT TRANSFER FUNCTION

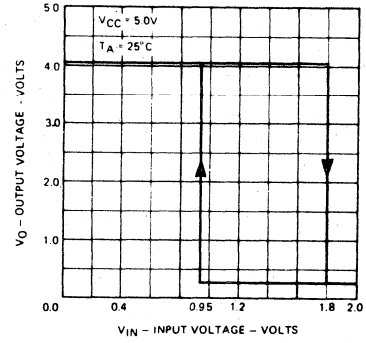


Fig. 1

THRESHOLD VOLTAGE AND HYSTERESIS VERSUS POWER SUPPLY VOLTAGE

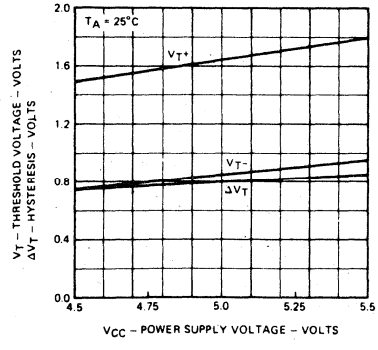


Fig. 2

THRESHOLD VOLTAGE AND HYSTERESIS VERSUS TEMPERATURE

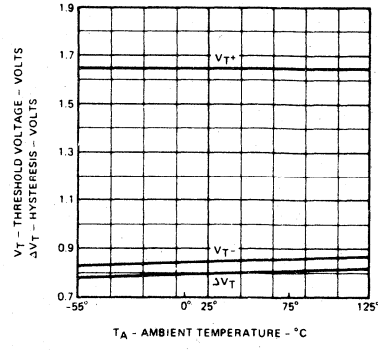


Fig. 3

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS13X, SN54LS14X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS13X, SN74LS14X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

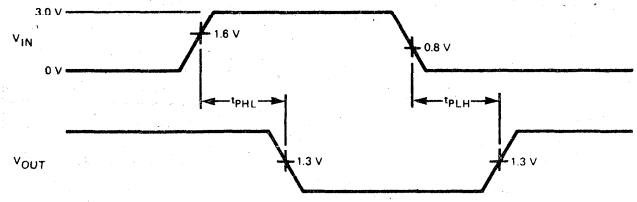
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{T+}	Positive-Going Threshold Voltage		1.5	1.8	2.0	V	V_{CC} = 5.0 V
V_{T-}	Negative-Going Threshold Voltage		0.6	0.95	1.1	V	V_{CC} = 5.0 V
$V_{T+}-V_{T-}$	Hysteresis		0.4	0.8		V	V_{CC} = 5.0 V
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{T+}	Input Current at Positive-Going Threshold			−0.14		mA	V_{CC} = 5.0 V, V_{IN} = V_{T+}
I_{T-}	Input Current at Negative-Going Threshold			−0.18		mA	V_{CC} = 5.0 V, V_{IN} = V_{T-}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			8.6	16	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			12	21	mA	V_{CC} = MAX, V_{IN} = 4.5 V

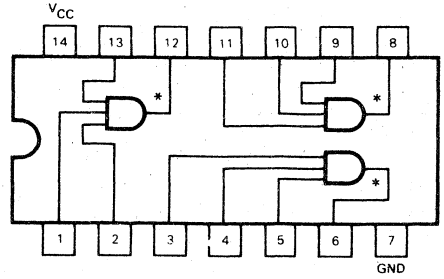
AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	MAX LS13	MAX LS14	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay, Input to Output	22	22	ns	V_{CC} = 5.0 V
t_{PHL}	Propagation Delay, Input to Output	27	22	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.



TRIPLE 3-INPUT AND GATE



*OPEN COLLECTOR OUTPUTS

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS15X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS15X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

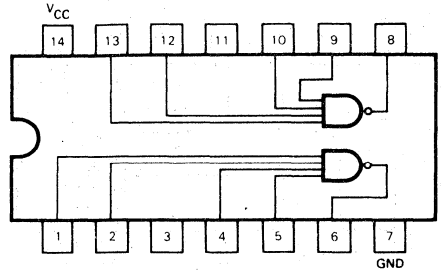
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IH}
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			1.8	3.6	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			3.3	6.6	mA	V_{CC} = MAX, V_{IN} = 0 V

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	7.0	13	20	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	5.0	10	15	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

DUAL 4-INPUT NAND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS20X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS20X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

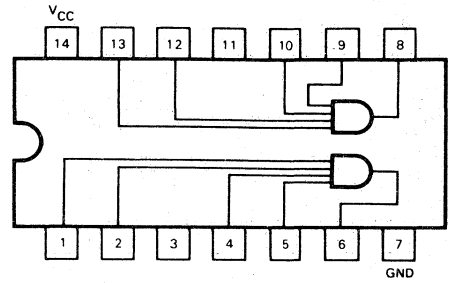
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.4	0.8	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			1.2	2.2	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output	3.0	7.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	7.0	10	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

DUAL 4-INPUT AND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS21X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS21X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

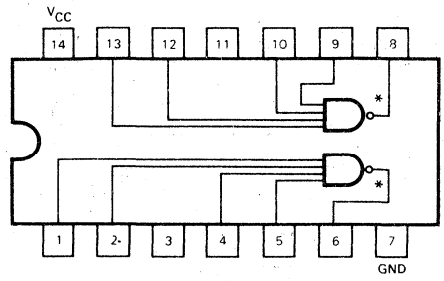
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			1.2	2.4	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			2.2	4.4	mA	V_{CC} = MAX, V_{IN} = 0 V

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		10	12	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		8.0	15	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

DUAL 4-INPUT NAND GATE



*OPEN COLLECTOR OUTPUTS

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS22X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS22X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

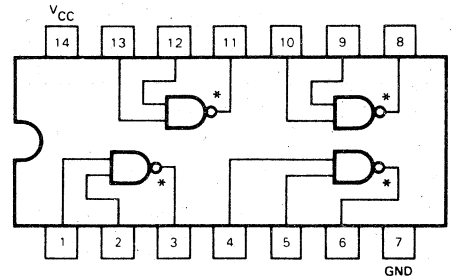
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			0.4	0.8	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			1.2	2.2	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	18	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

SN54LS26/SN74LS26
QUAD 2-INPUT NAND BUFFER



*Open Collector Outputs

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS26X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS26X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

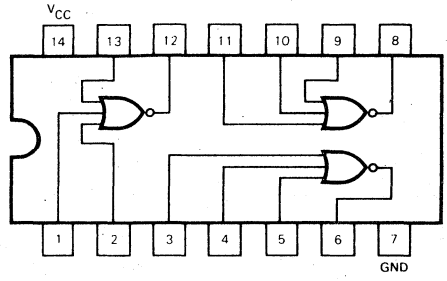
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				50	μA	V_{CC} = MIN, V_{OH} = 12 V, V_{IN} = V_{IL}
					1000	μA	* V_{CC}=MIN. V_{OH}=15 V, V_{IN}=V_{IL}
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			0.8	1.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			2.4	4.4	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	18	ns	C_L = 15 pF, R_L = 2.0 k

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

TRIPLE 3-INPUT NOR GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS27X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS27X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

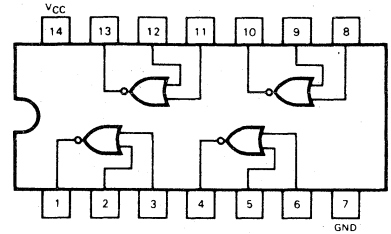
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			2.0	4.0	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			3.4	6.8	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		8.0	13	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		8.0	13	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

SN54LS28/SN74LS28
QUAD 2-INPUT NOR BUFFER



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS28X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS28X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

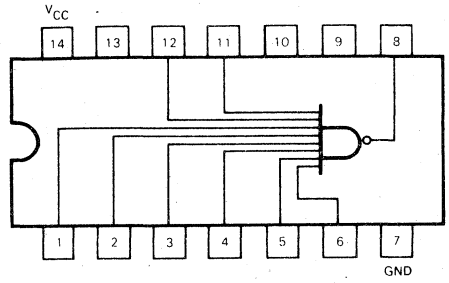
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54 74			0.7 0.8	V	Guaranteed Input LOW Voltage for All Inputs
V_{CD}	Input Clamp Diode			0.85	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54 74	2.5 2.7	3.06		V	I_{OH} = −1.2 mA V_{CC} = MIN, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage	54, 74 74		0.22 0.26	0.4 0.5	V	I_{OL} = 12 mA I_{OL} = 24 mA V_{CC} = MIN, V_{IN} = V_{IH}
I_{IH}	Input HIGH Current			0.1 0.1	20 100	μA μA	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short-Circuit Current		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current Input HIGH			2.1	3.6	mA	V_{CC} = MAX
I_{CCL}	Supply Current Input LOW			11	13.8	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay		8.5	24	ns	C_L = 50 pF, RL = 667 Ω
t_{PHL}	Propagation Delay		10.5	24	ns	V_{CC} = 5.0 V

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

8-INPUT NAND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS30X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS30X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

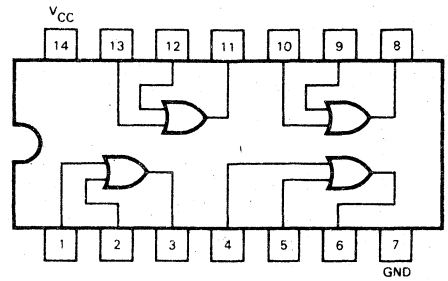
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.35	0.5	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			0.6	1.1	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		7.0	12	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		13	20	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

QUAD 2-INPUT OR GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS32X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS32X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			3.1	6.2	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			4.9	9.8	mA	V_{CC} = MAX, V_{IN} = 0 V

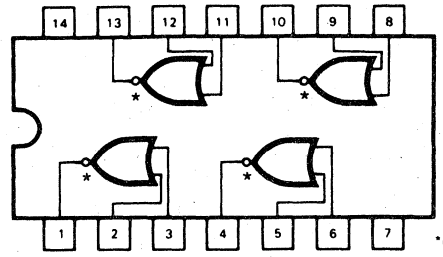
AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output	3.0	7.0	11	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	7.0	11	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

SN54LS33/SN74LS33

QUAD 2-INPUT NOR BUFFER OPEN COLLECTOR



*Open Collector Outputs

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS33X	4.5 V	5.0 V	5.5 V	-55°C to +125°C
SN74LS33X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

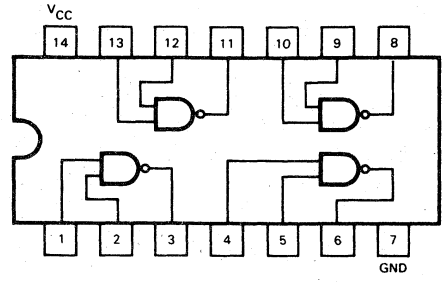
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			-0.65	-1.5	V	V_{CC} = MIN, I_{IN} = -18 mA
I_{OH}	Output High Current				250	μA	V_{CC} = MIN, V_{OH}=5.5 V, V_{IN}=V_{IL}
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 12 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 24 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			0.1	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				-0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			2	3.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			10	13.8	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		11	18	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		14	22	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

QUAD 2-INPUT NAND BUFFER



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS37X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS37X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type, W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

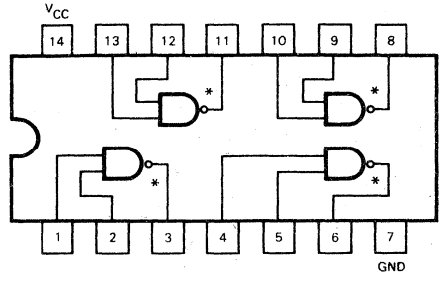
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −1.2 mA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 12 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 24 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−30		−130	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.9	2.0	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			6.0	12	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		10	20	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	20	ns	C_L = 45 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

QUAD 2-INPUT NAND BUFFER



*OPEN COLLECTOR OUTPUTS

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS38X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS38X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

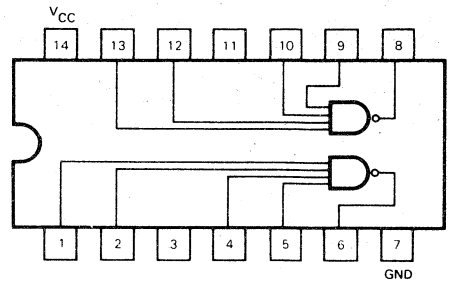
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				250	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 12 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 24 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			0.9	2.0	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			6.0	12	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	22	ns	C_L = 45 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

DUAL 4-INPUT NAND BUFFER



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS40X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS40X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −1.2 mA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 12 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 24 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−30		−130	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.45	1.0	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			3.0	6.0	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		10	24	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	24	ns	C_L = 45 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

SN54LS42/SN74LS42

ONE-OF-TEN DECODER

DESCRIPTION — The LSTTL/MSI SN54LS42/SN74LS42 is a Multipurpose Decoder designed to accept four BCD inputs and provide ten mutually exclusive outputs. The LS42 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

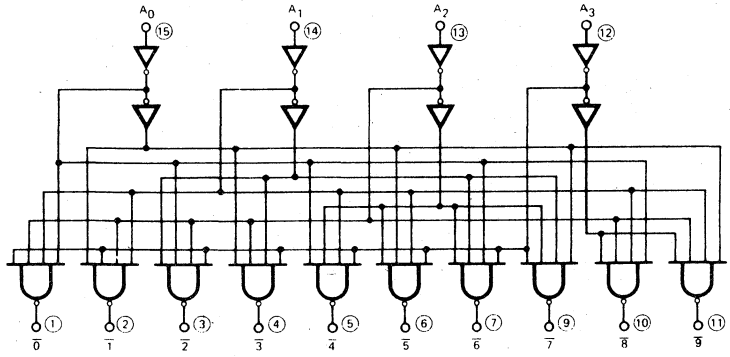
- MULTI-FUNCTION CAPABILITY
- MUTUALLY EXCLUSIVE OUTPUTS
- DEMULTIPLEXING CAPABILITY
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

		LOADING (Note a) HIGH	LOW
$A_0 - A_3$	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{0}$ to $\overline{9}$	Outputs, Active LOW (Note b)	10 U.L.	5(2.5) U.L.

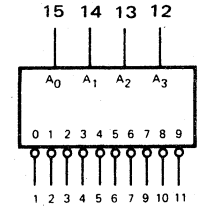
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



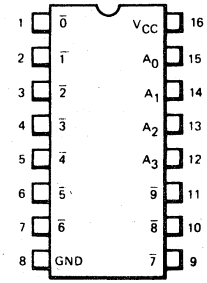
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS42 decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with active LOW input enables.

The logic design of the LS42 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input A_3 produces a useful inhibit function when the LS42 is used as a one-of-eight decoder. The A_3 input can also be used as the Data input in an 8-output demultiplexer application.

TRUTH TABLE

A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS42X	4.5 V	5.0 V	5.5 V	–55°C to +125°C
SN74LS42X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			7.0	12	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay (2 Levels)		11 18	18 25	ns	Fig. 2	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay (3 Levels)		12 19	20 27	ns	Fig. 1	

AC WAVEFORMS

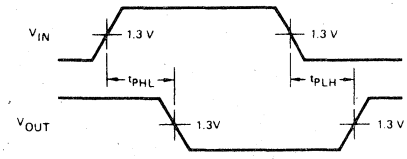


Fig. 1

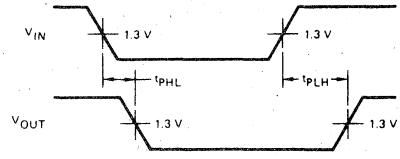


Fig. 2

SN54LS47/SN74LS47

BCD TO 7-SEGMENT DECODER/DRIVER

Advance Information

DESCRIPTION —The 54LS/74LS47 is Low Power Schottky BCD to 7-Segment Decoder/Drivers consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. They offer active LOW, high sink current outputs for driving indicators directly. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output and ripple-blanking input.

The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a 7-segment display indicator. The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the 54LS/74LS47 is designed to withstand the relatively high voltages required for 7-segment indicators.

The 54LS/74LS47 outputs will withstand 15 V with a maximum reverse current of 250 μA. Indicator segments requiring up to 24 mA of current may be driven directly from the 74LS47 high performance output transistors. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

The 54LS/74LS47 incorporates automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) may be performed at any time which the BI/BRO node is a HIGH level. This device also contains an overriding blanking input (BI) which can be used to control the lamp intensity or to inhibit the outputs.

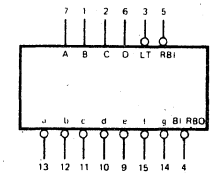
- **LAMP INTENSITY MODULATION CAPABILITY**
- **OPEN COLLECTOR OUTPUTS**
- **LAMP TEST PROVISION**
- **LEADING/TRAILING ZERO SUPPRESSION**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **INPUTS FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
A, B, C, D	BCD Inputs	0.5 U.L.	0.25 U.L.
$\overline{RBI}$	Ripple Blanking Input	0.5 U.L.	0.25 U.L.
$\overline{LT}$	Lamp Test Input	0.5 U.L.	0.25 U.L.
$\overline{BI/RBO}$	Blanking Input or	0.5 U.L.	0.75 U.L.
	Ripple Blanking Output	1.2 U.L.	2.0 U.L.
$\bar{a}$, to $\bar{g}$	Outputs	Open Collector	15 (7.5) U.L.

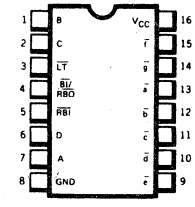
Notes:
a) 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW
b) Output current measured at V_{OUT} = 0.5 V
Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL

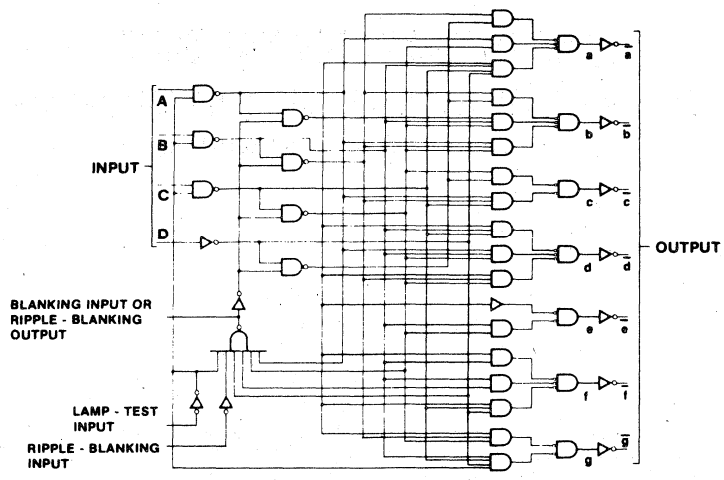


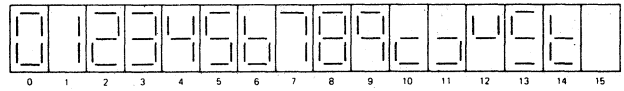
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



LOGIC DIAGRAM





NUMERICAL DESIGNATIONS – RESULTANT DISPLAYS

TRUTH TABLE

	INPUTS							OUTPUTS							
DECIMAL OR FUNCTION	$\overline{LT}$	$\overline{RBI}$	D	C	B	A	$\overline{BI/RBO}$	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	NOTE
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	A
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	A
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{BI}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	B
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	C
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	D

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

NOTES:

(A) $\overline{BI/RBO}$ is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output ($\overline{RBO}$). The blanking out (BI) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.

(B) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level regardless of the state of any other input condition.

(C) When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output (RBO) goes to a LOW level (response condition).

(D) When the blanking input/ripple-blanking output ($\overline{BI/RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS47X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS47X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54 74			0.7 0.8	V	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage, BI/RBO		2.4	4.2		V	V_{CC} = MIN, I_{OH} = −50 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage BI/RBO	54,74		0.25	0.4	V	I_{OL} = 1.6 mA; V_{CC} = MIN, V_{IN} = V_{IN}, or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 3.2 mA
$I_{O(off)}$	Off State Output Current a thru g				250	μA	V_{CC} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table, $V_{O(off)}$ = 15 V
$V_{O(on)}$	On State Outout Voltage a thru g	54, 74		0.25	0.4	V	$I_{O(on)}$ = 12 mA; V_{CL} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	$I_{O(on)}$ = 24 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current BI/RBO Any Input except BI/RBO				−1.2 −0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	BI/RBO Output Short Circuit Current (Note 4)		−0.3		−2.0	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			7	13	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.
5. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PHL} t_{PLH}	Propagation Delay, Address Input to Segment output			100 100	ns ns	V_{CC} = 5.0 V
t_{PHL} t_{PLH}	Propagation Delay, RBI Input To Segment Output			100 100	ns ns	C_L = 15 pF

AC WAVEFORMS

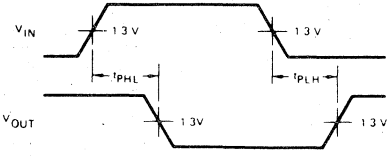


Fig. 1

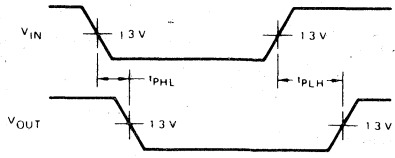


Fig. 2

SN54LS48/SN74LS48 • SN54LS49/SN74LS49

BCD TO 7-SEGMENT DECODER

Advance Information

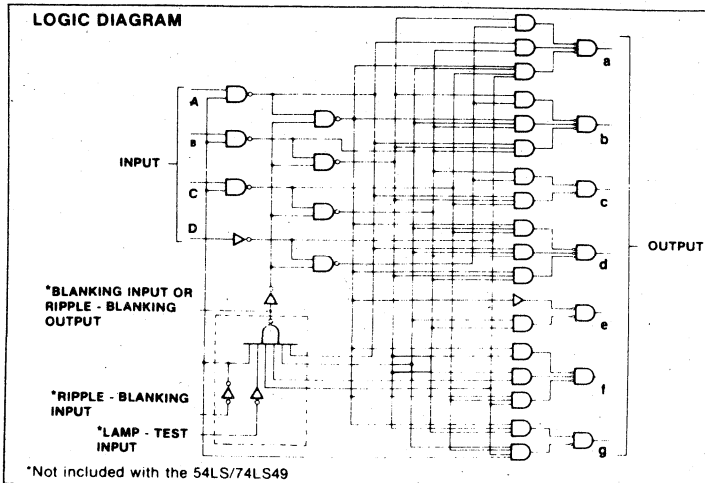
DESCRIPTION — The 54LS/74LS48 and 54LS/74LS49 are BCD to 7-Segment Decoders consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. The 54LS/74LS49 offers active HIGH open-collector outputs for current-sourcing applications to drive logic circuits or discrete, active components. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking input for the 54LS/74LS48. Four NAND gates and four input buffers provide BCD data and its complement and a buffer provides blanking input for the 54LS/74LS49.

The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive other components. The relative positive logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables.

The 54LS/74LS48 circuit incorporates automatic leading and/or trailing edge zero-blanking control (RBI and RBO). Lamp Test (LT) may be activated any time when the BI/RBO node is HIGH. Both devices contain on overriding blanking input (BI) which can be used to control the lamp intensity or to inhibit the outputs.

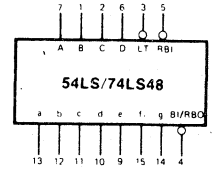
- **LAMP INTENSITY MODULATION CAPABILITY**
- **INTERNAL PULL-UPS ELIMINATE NEED FOR EXTERNAL RESISTORS ON 54LS/74LS48**
- **OPEN COLLECTOR OUTPUTS ON 54LS/74LS49**
- **INPUT CLAMP DIODES ELIMINATE HIGH-SPEED TERMINATION EFFECTS**
- **INPUTS FULLY TTL AND CMOS COMPATIBLE**

LOGIC DIAGRAM

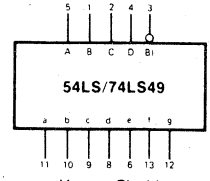


*Not included with the 54LS/74LS49

LOGIC SYMBOL

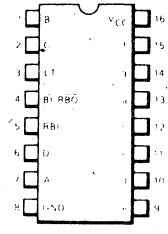


V_{CC} = Pin 16
GND = Pin 8

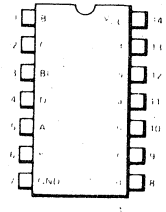


V_{CC} = Pin 14
GND = Pin 7

DIP (TOP VIEW)
54LS/74LS48



54LS/74LS49

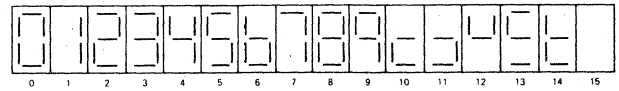


This is advance information and specifications are subject to change without notice.

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
		0.5 U.L.	0.25 U.L.
A, B, C, D,	BCD Inputs	0.5 U.L.	0.25 U.L.
$\overline{RBI}$	Ripple Blanking (Active Low) Input	0.5 U.L.	0.25 U.L.
$\overline{LT}$	Lamp Test (Active Low) Input	0.5 U.L.	0.75 U.L.
$\overline{BI}/\overline{RBO}$	Blanking Input or Ripple Blanking Output (Active Low)	1.2 U.L. 0.5 U.L.	2.0 U.L. 0.25 U.L.
$\overline{BI}$	Blanking (Active Low) Input	Open Collector	3.75 (1.25) U.L. (48)
a to g	Outputs (Note b)	Open Collector	5 (2.5) U.L. (49)

NOTES:
a) Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW
b) Output current measured at V_{OUT} = 0.5 V
Output LOW drive factor is 54LS/74LS48: 1.25 U.L. for Military (54), 3.75 U.L. for Commercial (74).
54LS/74LS49: 2.5 U.L. for Military (54), 5 U.L. for Commercial (74) Temperature Ranges.



NUMERICAL DESIGNATIONS – RESULTANT DISPLAYS

TRUTH TABLE
54LS/74LS48

	INPUTS						OUTPUTS							
DECIMAL OR FUNCTION	$\overline{LT}$	$\overline{RBI}$	D	C	B	A	$\overline{BI}/\overline{RBO}$	a	b	c	d	e	f	g	NOTE
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
$\overline{BI}$	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
$\overline{RBI}$	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
$\overline{LT}$	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

NOTES:
(1) $\overline{BI}/\overline{RBO}$ is wired-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X=input may be HIGH or LOW.

(2) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level, regardless of the state of any other input condition.

(3) When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).

(4) When the blanking input/ripple-blanking output ($\overline{BI}/\overline{RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp-test input, all segment outputs go to a LOW level.

TRUTH TABLE
54LS/74LS49

	INPUTS					OUTPUTS							
DECIMAL OR FUNCTION	D	C	B	A	$\overline{BI}$	a	b	c	d	e	f	g	NOTE
0	L	L	L	L	H	H	H	H	H	H	H	L	1
1	L	L	L	H	H	L	H	H	L	L	L	L	
2	L	L	H	L	H	H	H	L	H	H	L	H	
3	L	L	H	H	H	H	H	H	H	L	L	H	
4	L	H	L	L	H	L	H	H	L	L	H	H	
5	L	H	L	H	H	H	L	H	H	L	H	H	
6	L	H	H	L	H	L	L	H	H	H	H	H	
7	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	H	H	H	H	L	L	L	L	L	L	L	
$\overline{BI}$	X	X	X	X	L	L	L	L	L	L	L	L	2

NOTES:
(1) The blanking input must be open or held at a HIGH level when output functions 0 through 15 are desired.

(2) When a LOW level is applied to the blanking input all segment outputs go to a LOW level regardless of the state of any other input condition. X = input may be HIGH or LOW.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS48X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS48X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guarantee Input HIGH Voltage	
V_{IL}	Input LOW Voltage	74			0.8	V	Guarantee Input LOW Voltage	
		54			0.7	V		
V_{CD}	Input Clamp Diode Voltage				−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage		2.4	4.2		μA	V_{CC} = MIN, I_{OH} = −50 μA V_{IN} = V_{IH} or U.L. per Truth Table	
I_O	Output Current a thru g		−1.3			mA	V_{CC} = MIN, V_O = 0.85 V Input Conditioner as for V_{OH}	
V_{OL}	Output LOW Voltage	54, 74			0.4	V	I_{OL} = 4 mA	V_{CC} = MIN, V_{IH} = 2.0 V
		74			0.5	V	I_{OL} = 8 mA	V_{IL} = V_{IL} MAX
I_{IH}	Input Current HIGH				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input Current LOW				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{CC}	Power Supply Current			8.0	15	mA	V_{CC} = MAX	

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
t_{PHL}	Propagation delay time, HIGH-to-LOW level output from A input			100	ns	C_L = 15 pF, R_L = 4.0 kΩ,
t_{PLH}	Propagation delay time, LOW-to-HIGH level output from A input			100	ns	
t_{PHL}	Propagation delay time, HIGH-to-LOW level output from $\overline{RBI}$ input			100	ns	C_L = 15 pF, R_L = 6.0 kΩ,
t_{PLH}	Propagation delay time, LOW-to-HIGH level output from $\overline{RBI}$ input			100	ns	

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS49X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS49X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

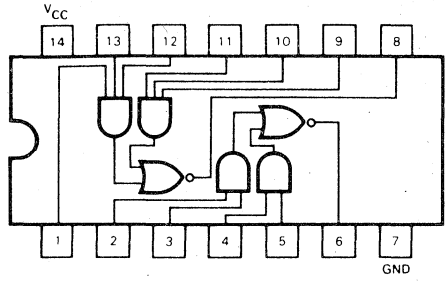
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guarantee Input HIGH Voltage	
V_{IL}	Input LOW Voltage	74			0.8	V	Guarantee Input LOW Voltage	
		54			0.7	V		
V_{CD}	Input Clamp Diode Voltage				−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
I_{OH}	Output HIGH Current				250	μA	V_{CC} = MIN, V_{IH} = 2.0 V V_{IL} = V_{IL} MAX, V_{OH} = 5.5 V	
V_{OL}	Output LOW Voltage	54, 74			0.4	V	I_{OL} = 4 mA	V_{CC} = MIN, V_{IH} = 2.0 V
		74			0.5	V	I_{OL} = 8 mA	V_{IL} = V_{IL} MAX
I_{IH}	Input Current HIGH				20 0.1	μA mA	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input Current LOW				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{CC}	Power Supply Current			8.0	15	mA	V_{CC} = MAX	

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
t_{PHL}	Propagation delay time, HIGH-to-LOW level output from A input			100	ns	C_L = 15 pF, R_L = 2.0 kΩ,
t_{PLH}	Propagation delay time, LOW-to-HIGH level output from A input			100	ns	
t_{PHL}	Propagation delay time, HIGH-to-LOW level output from $\overline{RBI}$ input			100	ns	C_L = 15 pF, R_L = 6.0 kΩ,
t_{PLH}	Propagation delay time, LOW-to-HIGH level output from $\overline{RBI}$ input			100	ns	

DUAL 2-WIDE 2-INPUT/3-INPUT AND-OR-INVERT GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS51X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS51X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

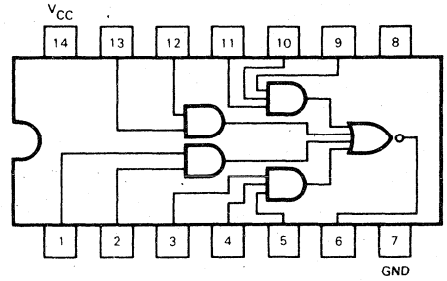
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.8	1.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			1.4	2.8	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		8.0	13	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		8.0	13	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

3-2-2-3-INPUT AND-OR-INVERT GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS54X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS54X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

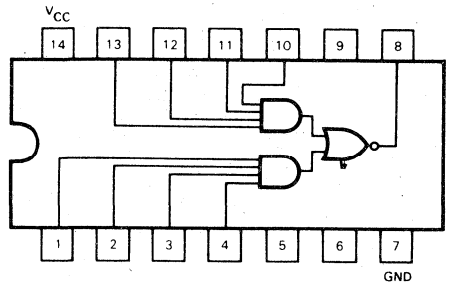
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.8	1.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			1.0	2.0	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

2-WIDE 4-INPUT AND-OR-INVERT GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS55X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS55X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.4	0.8	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			0.7	1.3	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	C_L = 15 pF

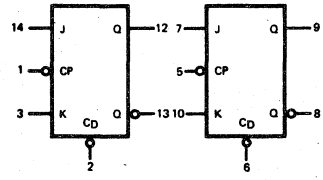
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

Advance Information

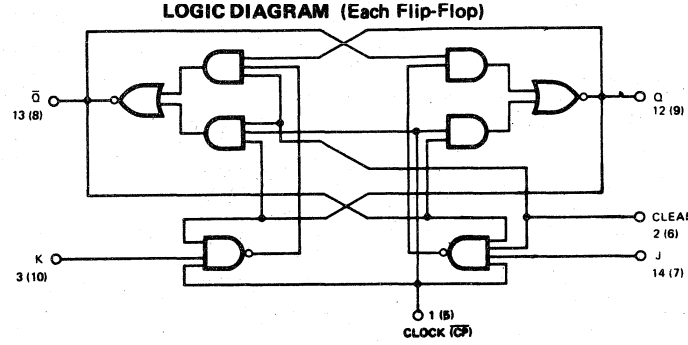
DESCRIPTION — The SN54LS73A/SN74LS73A offers individual J, K, clear, and clock inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC SYMBOL



V_{CC} = Pin 4
GND = Pin 11

LOGIC DIAGRAM (Each Flip-Flop)



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
SN54LS73AX	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS73AX	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA V_{IL} per Truth Table
I_{IH}	Input HIGH Current J, K				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Clear				60		
	Clock				80		
	J, K				0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V
	Clear				0.3		
	Clock				0.4		
I_{IL}	Input LOW Current J, K				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	Clear				−0.8		
	Clock				−0.8		
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	6.0	mA	V_{CC} = MAX, V_{CP} = 0 V

This is advance information and specifications are subject to change without notice.

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Reset (Clear)	L	X	X	L	H
Toggle	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	l	h	L	H
Load "1" (Set)	H	h	l	H	L
Hold	H	l	l	q	$\overline{q}$

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		11 16	20 20	ns	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clear to Output		11 16	20 20	ns	Fig. 2	

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_WCP(H)	Clock Pulse Width (HIGH)	18	12		ns	Fig. 3	
t_WCP(L)	Clock Pulse Width (LOW)	15	10		ns		
t_W	Clear Pulse Width	15	10		ns	Fig. 2	
t_s(H)	Set-up Time HIGH, J or K to Clock	20	13		ns	Fig. 3	V_{CC} = 5.0 V
t_h(H)	Hold Time HIGH, J or K to Clock	0	−10		ns		
t_s(L)	Set-up Time LOW, J or K TO Clock	15	10		ns		
t_h(L)	Hold Time LOW, J or K to Clock	0	−13		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

AC WAVEFORMS

Fig. 1 CLOCK TO OUTPUT DELAYS, DATA SET-UP AND HOLD TIMES, CLOCK PULSE WIDTH

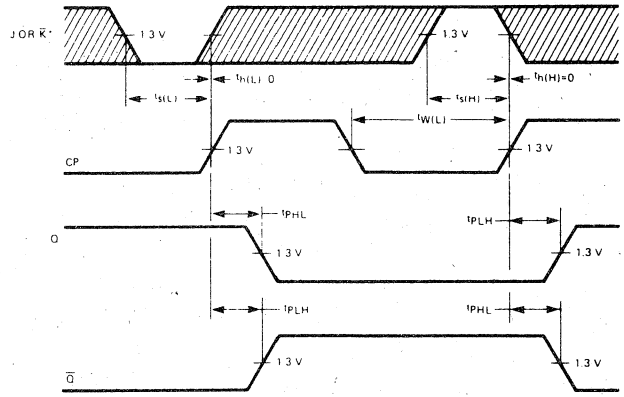


Fig. 2 SET AND CLEAR TO OUTPUT DELAYS, SET AND CLEAR PULSE WIDTHS

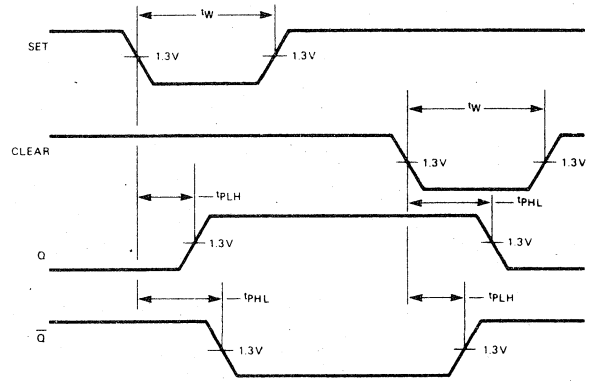
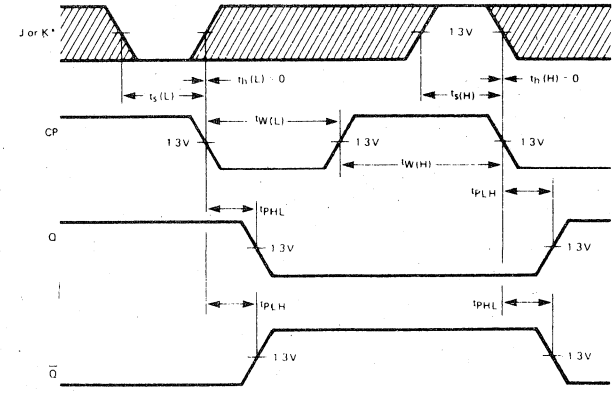


Fig. 3 CLOCK TO OUTPUT DELAYS, DATA SET-UP AND HOLD TIMES, CLOCK PULSE WIDTH



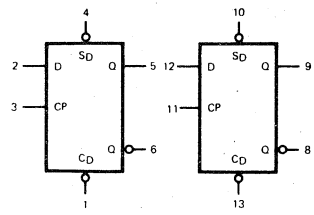
*The shaded areas indicate when the input is permitted to change for predicatable output performance.

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The SN54LS74A/SN74LS74A dual edge-triggered flip-flip utilizes Schottky TTL circuitry to produce high speed D-type flip-flops. Each flip-flop has individual clear and set inputs, and also complementary Q and Q outputs.

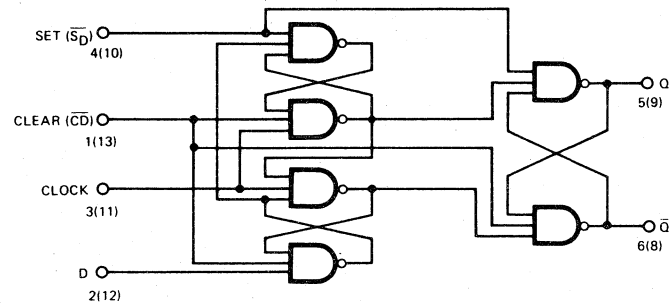
Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or the LOW level, the D input signal has no effect.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

LOGIC DIAGRAM
(EACH FLIP-FLOP)



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS74AX	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS74AX	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current Data, Clock Set, Clear				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Data, Clock Set, Clear				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current Data, Clock Set, Clear				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	8.0	mA	V_{CC} = MAX, V_{CP} = 0 V

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	D	Q	$\overline{Q}$
Set	L	H	X	H	L
Reset (Clear)	H	L	X	L	H
*Undetermined	L	L	X	H	H
Load "1" (Set)	H	H	h	H	L
Load "0" (Reset)	H	H	l	L	H

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

AC CHARACTERISTICS: T_A = 25°C (See SN54LS73A for Waveforms)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Maximum Clock Frequency		30	45		MHz	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output			9 13	20 30	ns	Fig. 1	
t_{PLH} t_{PHL} t_{PHL}	Propagation Delay, Set or Clear to Output	CP = L CP = H		8 13 13	15 25 24	ns	Fig. 2	

AC SET-UP REQUIREMENTS: T_A = 25°C (See SN54LS73A for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_wCP(H)	Clock Pulse Width (HIGH)	18	12		ns	Fig. 1	V_{CC} = 5.0 V
t_w	Set or Clear Pulse Width	15	10		ns	Fig. 2	
t_s(H)	Set-up Time HIGH, Data to Clock	10	6		ns	Fig. 1	
t_h(H)	Hold Time HIGH, Data to Clock	0	−14		ns		
t_s(L)	Set-up Time LOW, Data to Clock	20	14		ns		
t_h(L)	Hold Time LOW, Data to Clock	0	−6		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

SN54LS75/SN74LS75 • SN54LS77/SN74LS77

4-BIT D LATCH

Advance Information

DESCRIPTION – The TTL/MSI 54LS/74LS75 and 54LS/74LS77 are latches used as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the Enable is HIGH and the Q output will follow the data input as long as the Enable remains HIGH. When the Enable goes LOW, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the Enable is permitted to go HIGH.

The 54LS/74LS75 features complementary Q and $\overline{Q}$ output from a 4-bit latch and is available in the 16-pin packages. For higher component density applications the 54LS/74LS77 4-bit latch is available in the 14-pin package with Q outputs omitted.

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
D_1–D_4	Data Inputs	0.5 U.L.	0.25 U.L.
E_{0-1}	Enable Input Latches 0, 1	2.0 U.L.	1.0 U.L.
E_{2-3}	Enable Input Latches 2, 3	2.0 U.L.	1.0 U.L.
Q_1–Q_4	Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q_1}$–$\overline{Q_4}$	Complimentary Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.

Notes:

a. 1 Unit Load (U.L.) = 40μA LOW

b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

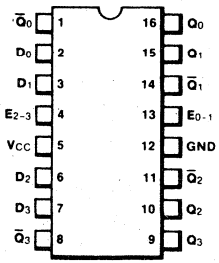
TRUTH TABLE
(Each latch)

t_n	t_{n+1}
D	Q
H	H
L	L

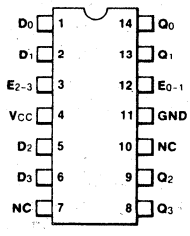
NOTES:
t_n = bit time before clock negative-going transition
t_{n+1} = bit time after clock negative-going transition.

CONNECTION DIAGRAMS
DIP (TOP VIEW)

54LS/75LS75

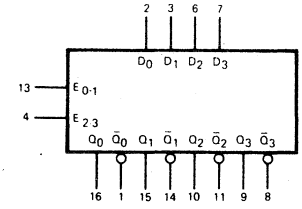


54LS/74LS77



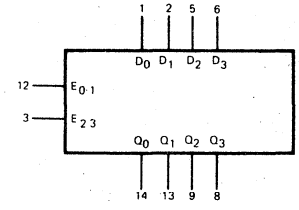
LOGIC SYMBOLS

54LS/74LS75



V_{CC} = Pin 5
GND = Pin 12

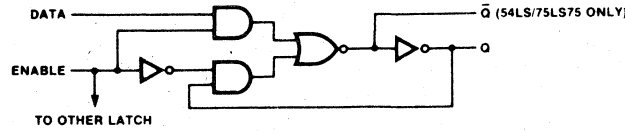
54LS/74LS77



V_{CC} = Pin 4
GND = Pin 11
NC = Pin 7, 10

This is advance information and specifications are subject to change without notice.

LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

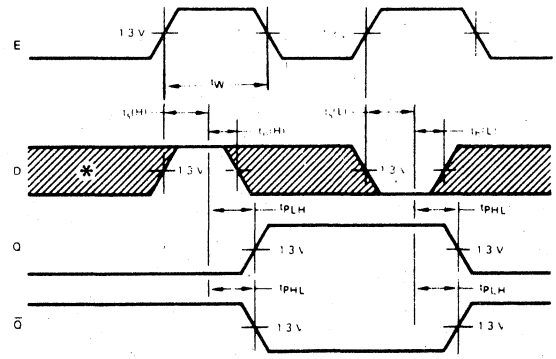
PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS75X SN54LS77X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS75X SN74LS77X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_wCP	Minimum Enable Pulse Width	20			ns	Fig. 1
t_s	Set-up Time, Data to Enable (HIGH or LOW)	20			ns	Fig. 1
t_h	Hold Time, Data to Enable (HIGH or LOW)	0			ns	Fig. 1

AC WAVEFORMS



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

DEFINITION OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54 74			0.7 0.8	V	Guaranteed Input LOW Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54 74	2.5 2.7	3.4 3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54, 74 74		0.25 0.35	0.4 0.5	V	I_{OL} = 4.0 mA V_{CC} = MIN, V_{IN} = V_{IH} I_{OL} = 8.0 mA or V_{IL} per Truth Table
I_{IH}	Input HIGH Current D E				20 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Input HIGH Current at MAX Input Voltage D E				0.1 0.4	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current D E				−0.4 −1.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.3	12	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS : T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, D to Q			27 17	ns	V_{CC} = 5.0 V C_L = 15 pF Fig. 1
t_{PLH} t_{PHL}	Propagation Delay, D to $\overline{Q}$ (LS75)			20 15	ns	
t_{PLH} t_{PHL}	Propagation Delay, Enable to Q			27 25	ns	
t_{PLH} t_{PHL}	Propagation Delay, Enable to $\overline{Q}$			30 15	ns	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54 74			0.7 0.8	V	Guaranteed Input LOW Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54 74	2.5 2.7	3.4 3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54, 74 74		0.25 0.35	0.4 0.5	V	I_{OL} = 4.0 mA V_{CC} = MIN, V_{IN} = V_{IH} I_{OL} = 8.0 mA or V_{IL} per Truth Table
I_{IH}	Input HIGH Current D E				20 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Input HIGH Current at MAX Input Voltage D E				0.1 0.4	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current D E				−0.4 −1.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.3	12	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS : T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, D to Q			19 17	ns	V_{CC} = 5.0 V C_L = 15 pF Fig. 1
t_{PLH} t_{PHL}	Propagation Delay, Enable to Q			18 18	ns	

SN54LS76A/SN74LS76A

DUAL JK FLIP-FLOP WITH SET AND CLEAR

Advance Information

DESCRIPTION — The 54LS/74LS76A offers individual J, K, Clock Pulse, Direct Set and Direct Clear inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The Logic Level of the J and K inputs will perform according to the Truth Table as long as minimum set-up times are observed. Input data is transferred to the outputs on the HIGH-to-LOW clock transitions.

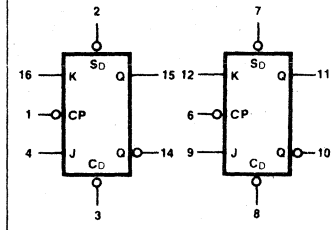
MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

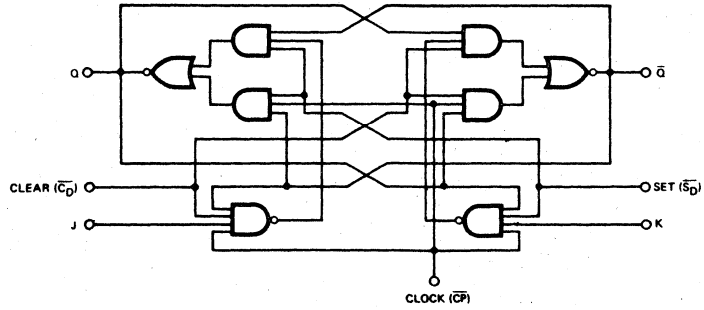
H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Immaterial
l,h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.

LOGIC SYMBOL



V_{CC} = Pin 5
GND = Pin 13

LOGIC DIAGRAM



This is advance information and specifications are subject to change without notice.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS76AX	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS76AX	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH}
		74		0.35	0.5		I_{OL} = 8.0 mA; or V_{IL} per Truth Table
I_{IH}	Input HIGH Current J, K Set, Clear Clock				20 60 80	μA	V_{CC} = MAX, V_{In} = 2.7 V
	J, K Set, Clear Clock				0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current J, K Set, Clear, Clock				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	6.0	mA	V_{CC} = MAX, V_{CP} = 0 V

AC CHARACTERISTICS: T_A = 25°C (See Introduction for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 3	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		11 16	20 20	ns	Fig. 3	
t_{PLH} t_{PHL}	Propagation Delay, Set or Clear to Output		16 16	20 20	ns	Fig. 2	

AC SET-UP REQUIREMENTS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_wCP(H)	Clock Pulse Width (HIGH)	18	12		ns	Fig. 3	V_{CC} = 5.0 V
t_wCP(L)	Clock Pulse Width (LOW)	15	10		ns		
t_w	Set or Clear Pulse Width	15	10		ns	Fig. 2	
t_s(H)	Set-up Time HIGH, J or K to Clock	20	13		ns	Fig. 3	
t_h(H)	Hold Time HIGH, J or K to Clock	0	−10		ns		
t_s(L)	Set-up Time LOW, J or K to Clock	15	10		ns		
t_h(L)	Hold Time LOW, J or K to Clock	0	−13		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.
5. HOLD TIME (t) is defined as the minimum time following the clock transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH-to-LOW and still be recognized.

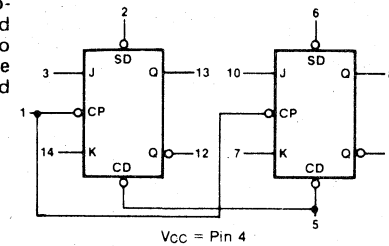
Advance Information

SN54LS78A/SN74LS78A

DUAL JK FLIP FLOP

DESCRIPTION – The 54LS/74LS78A offers individual J, K, and Direct Set inputs as well as common Clock Pulse and Common Direct Clear Inputs. These dual Flip-Flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The Logic Level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the Truth Table as long as minimum set-up times are observed. Input data is transferred to the outputs on the HIGH-to-LOW Clock Transition.

LOGIC SYMBOL



V_{CC} = Pin 4
GND = Pin 11

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS78AX	4.5 V	5.0 V	5.5 V	-55°C to +125°C
SN74LS78AX	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			-0.65	-1.5	V	V_{CC} = MIN, I_{IN} = -18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = -400 μA; V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current J, K Set, Clear Clock				20 60 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	J, K Set, Clear Clock				0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current J, K **Set, Clear, Clock**				-0.4 -0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-20		-100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	6.0	mA	V_{CC} = MAX, V_{CP} = 0 V

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Immaterial
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 3	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		11 16	20 20	ns	Fig. 3	
t_{PLH} t_{PHL}	Propagation Delay, Set or Clear to Output		11 16	20 20	ns	Fig. 2	

AC SET-UP REQUIREMENTS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_WCP(H)	Clock Pulse Width (HIGH)	18	12		ns	Fig. 3	V_{CC} = 5.0 V
t_WCP(L)	Clock Pulse Width (LOW)	15	10		ns		
t_W	Set or Clear Pulse Width	15	10		ns	Fig. 2	
t_s(H)	Set-up Time HIGH, J or K to Clock	20	13		ns	Fig. 3	
t_h(H)	Hold Time HIGH, J or K to Clock	0	−10		ns		
t_s(L)	Set-up Time LOW, J or K to Clock	15	10		ns		
t_h(L)	Hold Time LOW, J or K to Clock	0	−13		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH-to-LOW and still be recognized.

SN54LS83A/SN74LS83A

4-BIT BINARY FULL ADDER WITH FAST CARRY

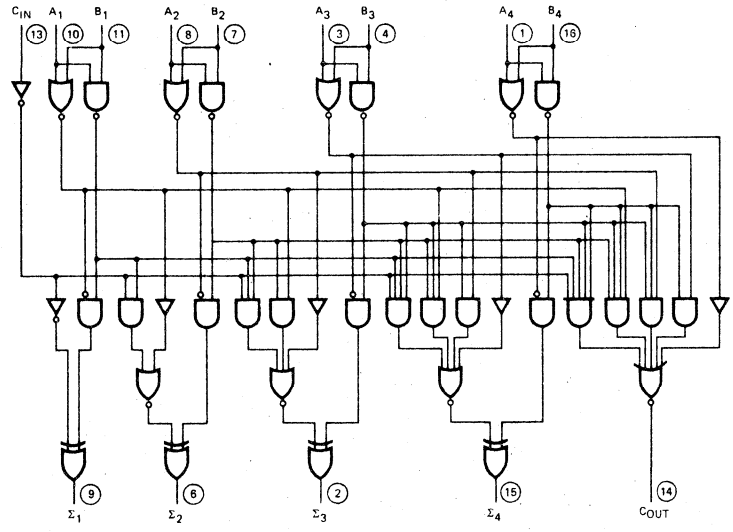
DESCRIPTION – The SN54LS83A/SN74LS83A is a high-speed 4-Bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words ($A_1 - A_4$, $B_1 - B_4$) and a Carry Input (C_{IN}). It generates the binary Sum outputs ($\Sigma_1 - \Sigma_4$) and the Carry Output (C_{OUT}) from the most significant bit. The LS83 operates with either active HIGH or active LOW operands (positive or negative logic). The SN54LS283/SN74LS283 is recommended for new designs since it is identical in function with this device and features standard corner power pins.

PIN NAMES

		LOADING (Note a) HIGH	LOW
$A_1 - A_4$	Operand A Inputs	1.0 U.L.	0.5 U.L.
$B_1 - B_4$	Operand B Inputs	1.0 U.L.	0.5 U.L.
C_{IN}	Carry Input	0.5 U.L.	0.25 U.L.
$\Sigma_1 - \Sigma_4$	Sum Outputs (Note b)	10 U.L	5(2.5) U.L.
C_{OUT}	Carry Output (Note b)	10 U.L	5(2.5) U.L.

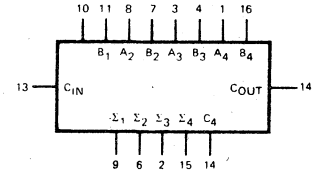
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for commercial (74) Temperature Ranges.

LOGIC DIAGRAM



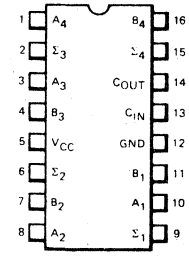
V_{CC} = Pin 5
GND = Pin 12
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 5
GND = Pin 12

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS83A adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs ($\Sigma_1 - \Sigma_4$) and outgoing carry (C_{OUT}) outputs.

$$C_{IN}+(A_1+B_1)+2(A_2+B_2)+4(A_3+B_3)+8(A_4+B_4) = \Sigma_1+2\Sigma_2+4\Sigma_3+8\Sigma_4+16C_{OUT}$$

Where: (+) = plus

Due to the symmetry of the binary add function the LS83A can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH inputs, Carry In can not be left open, but must be held LOW when no carry in is intended.

Example:

	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}	
logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10+9=19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry+5+6=12)

Interchanging inputs of equal weight does not affect the operation, thus C_{IN}, A_1, B_1, can be arbitrarily assigned to pins 10, 11, 13, etc.

ABSOLUTE MAXIMUM RATINGS above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS83AX	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS83AX	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current C_{IN} Any A or B				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	C_{IN} Any A or B				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current C_{IN} Any A or B				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			22	39	mA	V_{CC} = MAX, All Inputs 0 V
				19	34	mA	V_{CC} = MAX, A Inputs = 4.5 V

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, C_{IN} Input to Any Σ Output			24 24	ns	V_{CC} = 5.0 V C_L = 15 pF Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to Σ Outputs			24 24	ns	
t_{PLH} t_{PHL}	Propagation Delay, C_{IN} Input to C_{OUT} Output			17 17	ns	
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to C_{OUT} Output			17 17	ns	

AC WAVEFORMS

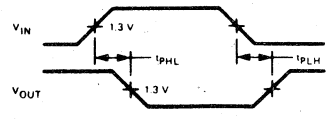


Fig. 1

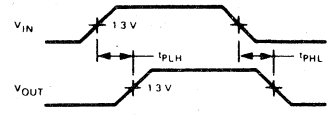


Fig. 2

SN54LS85/SN74LS85
4-BIT MAGNITUDE COMPARATOR

DESCRIPTION — The 54LS/74LS85 is a 4-Bit Magnitude Comparator which compares two 4-bit words (A, B), each word having four Parallel Inputs (A_0-A_3, B_0-B_3); A_3, B_3 being the most significant inputs. Operation is not restricted to binary codes, the device will work with any monotonic code. Three Outputs are provided: "A greater than B" ($O_{A>B}$), "A less than B" ($O_{A<B}$), "A equal to B" ($O_{A=B}$). Three Expander Inputs, $I_{A>B}$, $I_{A<B}$, $I_{A=B}$, allow cascading without external gates. For proper compare operation, the Expander Inputs to the least significant position must be connected as follows: $I_{A<B} = I_{A>B} = L$, $I_{A=B} = H$. For serial (ripple) expansion, the $O_{A>B}$, $O_{A<B}$ and $O_{A=B}$ Outputs are connected respectively to the $I_{A>B}$, $I_{A<B}$, and $I_{A=B}$ inputs of the next most significant comparator, as shown in Figure 1. Refer to Applications section of data sheet for high speed method of comparing large words.

The Truth Table on the following page describes the operation of the 54LS/74LS85 under all possible logic conditions. The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a series expansion scheme. The lower five lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

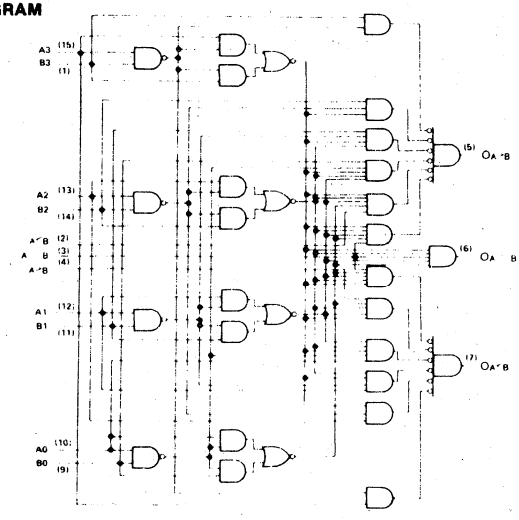
- **EASILY EXPANDABLE**
- **BINARY OR BCD COMPARISON**
- **$O_{A>B}$, $O_{A<B}$, AND $O_{A=B}$ OUTPUTS AVAILABLE**

PIN NAMES

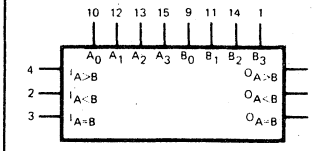
		LOADING (Note a) HIGH	LOW
A_0-A_3, B_0-B_3	Parallel Inputs	1.5 U.L.	0.75 U.L.
$I_{A=B}$	A = B Expander Inputs	1.5 U.L.	0.75 U.L.
$I_{A<B}$, $I_{A>B}$	A < B, A > B, Expander Inputs	0.5 U.L.	0.25 U.L.
$O_{A>B}$	A Greater Than B Output (Note b)	10 U.L.	5 (2.5) U.L.
$O_{A<B}$	B Greater Than A Output (Note b)	10 U.L.	5 (2.5) U.L.
$O_{A=B}$	A Equal to B Output (Note b)	10 U.L.	5 (2.5) U.L.

Notes.
a. 1 TTL Unit Load (U.L.) = 40μA HIGH/1.6mA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM

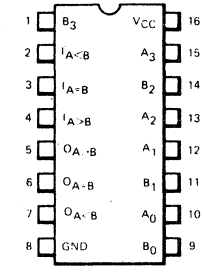


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

TRUTH TABLE

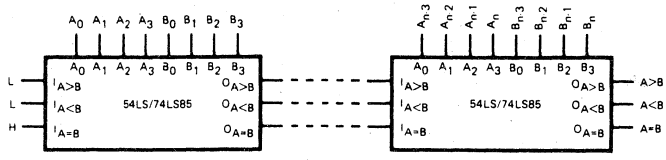
COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	H	L	H	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	H	H	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	H	H	H	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	H	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	L	L	L

H = HIGH Level
L = LOW Level
X = IMMATERIAL

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS85X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS85X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.



L = LOW Level
H = HIGH Level

Fig. 1. COMPARING TWO n-BIT WORDS

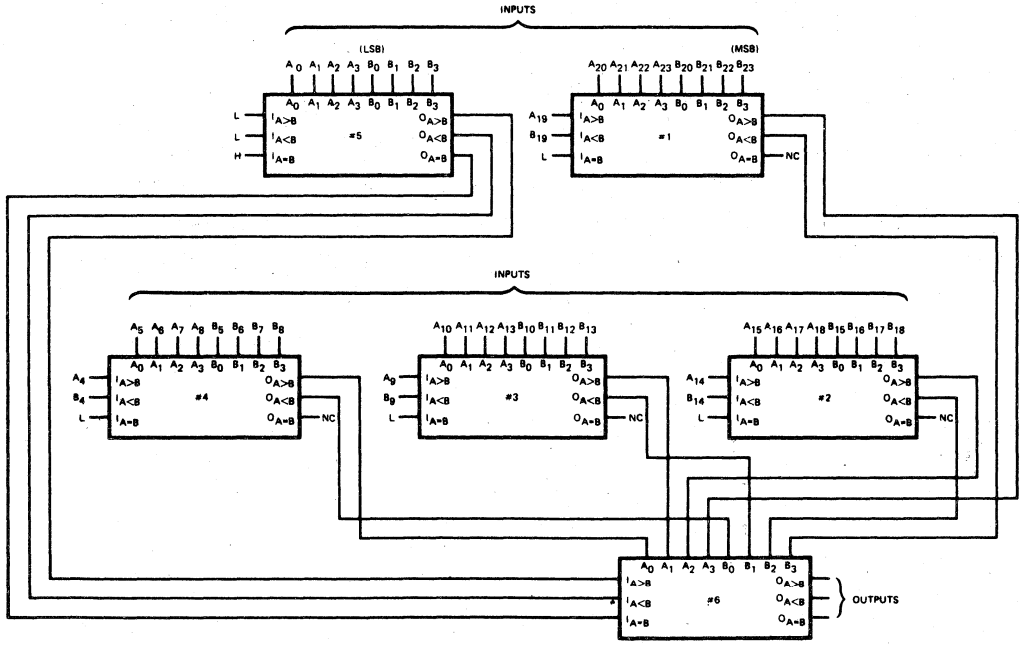
APPLICATIONS

Figure 2 shows a high speed method of comparing two 24-bit words with only two levels of device delay. With the technique shown in Figure 1, six levels of device delay result when comparing two 24-bit words. The parallel technique can be expanded to any number of bits, see Table I.

TABLE I

WORD LENGTH	NUMBER OF PKGS.
1-4 Bits	1
5-24 Bits	2 - 6
25-120 Bits	8 - 31

NOTE:
The 54LS/74LS85 can be used as a 5-bit comparator only when the outputs are used to drive the A_0-A_3 and B_0-B_3 inputs of another 54LS/74LS85 as shown in Figure 2 in positions #1, 2, 3, and 4.



MSB = Most Significant Bit
LSB = Least Significant Bit

L = LOW Level
H = HIGH Level
NC = No Connection

Fig. 2. COMPARISON OF TWO 24-BIT WORDS

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5			
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH}
		74		0.35	0.5		I_{OL} = 8.0 mA; or V_{IL} per Truth Table
I_{IH}	Input HIGH Current A_0-A_3, B_0-B_3, $I_{A=B}$				60	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	$I_{A<B}$, $I_{A>B}$				20		
	A_0-A_3, B_0-B_3, $I_{A=B}$				0.3	mA	V_{CC} = MAX, V_{IN} = 10 V
	$I_{A<B}$, $I_{A>B}$				0.1		
I_{IL}	Input LOW Current A_0-A_3, B_0-B_3, $I_{A=B}$				−1.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	$I_{A<B}$, $I_{A>B}$				−0.4		
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			11	20	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the table, are chosen to guarantee operations under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS : T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Any A or B Data Input to		25	36	ns	Fig. 1, 2
t_{PHL}	Any Output		20	30		
t_{PLH}	$A=B$ Input to $A>B$ or		15	22	ns	Fig. 1, 2
t_{PHL}	$A<B$ Output		12	17		
t_{PLH}	$A=B$ Input to		14	12	ns	Fig. 1, 2
t_{PHL}	$A=B$ Output		12	17		
t_{PLH}	$A>B$ or $A<B$ Input		25	36	ns	Fig. 1, 2
t_{PHL}	to Any Output		20	30		

AC WAVEFORMS

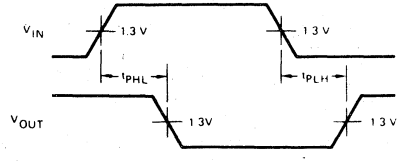


Fig. 1

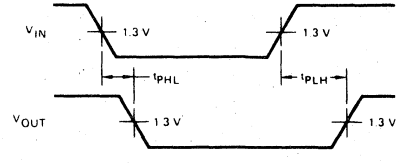
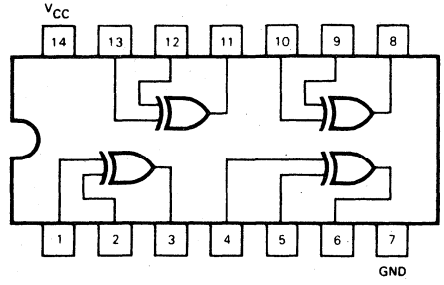


Fig. 2

QUAD 2-INPUT EXCLUSIVE OR GATE



TRUTH TABLE

IN		OUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS86X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS86X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA $V_{IN} \leq V_{IH}$ or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current			6.1	10	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, Other Input LOW			12 17	ns	V_{CC} = 5.0 V
t_{PLH} t_{PHL}	Propagation Delay, Other Input HIGH			10 12	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

Advance Information

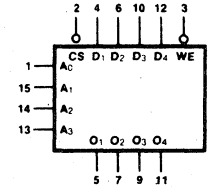
SN54LS89/SN74LS89

64-BIT RANDOM ACCESS MEMORY WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION – The 54LS/74LS89 is a high-speed, low-power 64-bit Random Access Memory organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading, and addresses are fully decoded on-chip. Outputs are open-collector type and are in the off (HIGH) state when both the Chip Select (CS) and Write Enable (WE) are HIGH. For all other combinations of CS and WE the outputs are active, presenting the complement of either the stored data (READ mode) or the information present on the D inputs.

- **OPEN–COLLECTOR OUTPUTS FOR WIRED-AND APPLICATIONS**
- **BUFFERED INPUTS MINIMIZE LOADING**
- **ADDRESS DECODING ON-CHIP**
- **DIODE CLAMPED INPUTS MINIMIZE RINGING**
- **LOW POWER SCHOTTKY DESIGN MINIMIZES POWER CONSUMPTION**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

AN	Address Input
$\overline{CS}$	Chip Select (active LOW) Input
D_n	Data Input
O_n	Data (inverted) Output
$\overline{WE}$	Write Enable (active LOW) Input

FUNCTION TABLE

INPUTS $\overline{CS}$	INPUTS $\overline{WE}$	OPERATION	CONDITION OF OUTPUTS
L	H	Write	Complement of Data Inputs
L	H	Read	Complement of Selected Word
H	L	Inhibit Entry	Complement of Data Inputs
H	H	Hold	HIGH (Off)

H = HIGH Voltage Level
L = LOW Voltage Level

This is advance information and specifications are subject to change without notice.

SN54LS90/SN74LS90 • SN54LS92/SN74LS92

DECADE COUNTER — DIVIDE-BY-TWELVE COUNTER

SN54LS93/SN74LS93

4-BIT BINARY COUNTER

DESCRIPTION — The SN54LS90/SN74LS90, SN54LS92/SN74LS92 and SN54LS93/SN74LS93 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS90), divide-by-six (LS92) or divide-by-eight (LS93) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to $\overline{CP}$) to form BCD, bi-quinary, modulo-12, or modulo-16 counters. All of the counters have a 2-input gated Master Reset (Clear), and the LS90 also has a 2-input gated Master Set (Preset 9).

- **LOW POWER CONSUMPTION . . . TYPICALLY 45 mW**
- **HIGH COUNT RATES . . . TYPICALLY 50 MHz**
- **CHOICE OF COUNTING MODES . . . BCD, BI-QUINARY, DIVIDE-BY-TWELVE, BINARY**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

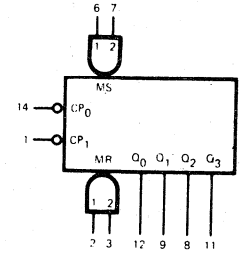
		LOADING (Note a) HIGH	LOW
$\overline{CP}_0$	Clock (Active LOW going edge) Input to ÷2 Section	3.0 U.L.	1.5 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷5 Section (LS90), ÷6 Section (LS92)	2.0 U.L.	2.0 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷8 Section (LS93)	1.0 U.L.	1.0 U.L.
MR_1, MR_2	Master Reset (Clear) Inputs	0.5 U.L.	0.25 U.L.
MS_1, MS_2	Master Set (Preset-9, LS90) Inputs	0.5 U.L.	0.25 U.L.
Q_0	Output from ÷2 Section (Notes b & c)	10 U.L.	5(2.5) U.L.
Q_1, Q_2, Q_3	Outputs from ÷5 (LS90), ÷6 (LS92), ÷8 (LS93) Sections (Note b)	10 U.L.	5(2.5) U.L.

NOTES:

a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.
c. The Q_0 Outputs are guaranteed to drive the full fan-out plus the $\overline{CP}_1$ input of the device.

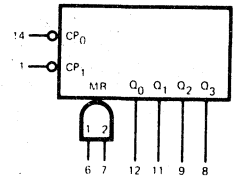
LOGIC SYMBOL

LS90



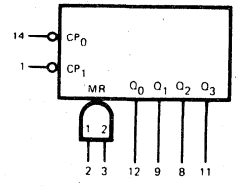
V_{CC} = Pin 5
GND = Pin 10
NC = Pins 4, 13

LS92



V_{CC} = Pin 5
GND = Pin 10
NC = Pins 2, 3, 4, 13

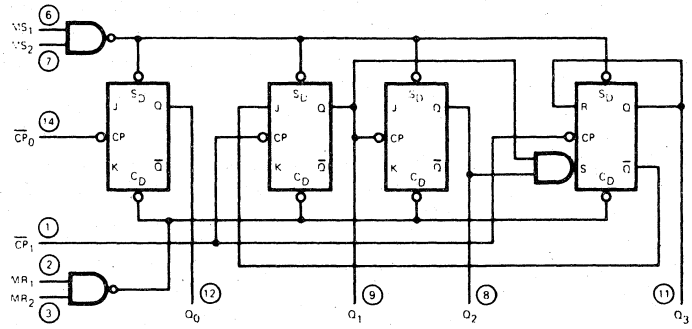
LS93



V_{CC} = Pin 5
GND = Pin 10
NC = Pins 4, 6, 7, 13

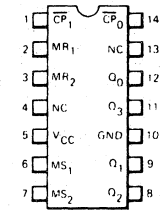
LOGIC DIAGRAM

LS90



○ = Pin Numbers
V_{CC} = Pin 5
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)

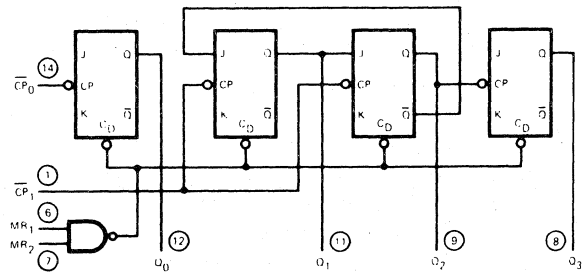


NC = No Internal Connection

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

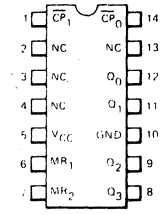
LOGIC DIAGRAM

LS92



○ = Pin Numbers
V_{CC} = Pin 5
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)

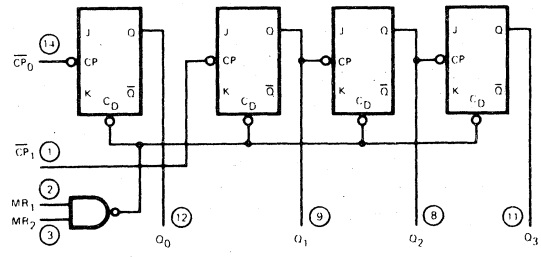


NC = No Internal Connection

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

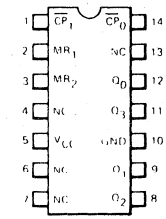
LOGIC DIAGRAM

LS93



○ = Pin Numbers
V_{CC} = Pin 5
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



NC = No Internal Connection

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS90, LS92, and LS93 are 4-bit ripple type Decade, Divide-By-Twelve, and Binary Counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS90), divide-by-six (LS92), or divide-by-eight (LS93) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device.

A gated AND asynchronous Master Reset ($MR_1 \bullet MR_2$) is provided on all counters which overrides and clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ($MS_1 \bullet MS_2$) is provided on the LS90 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.:

LS90

A. BCD Decade (8421) Counter – The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Bi-quinary Divide-By-Ten Counter – The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output Q_0.

C. Divide-By-Two and Divide-By-Five Counter – No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain binary divide-by-five operation at the Q_3 output.

LS92

A. Modulo 12, Divide-By-Twelve Counter – The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and Q_3 produces a symmetrical divide-by-twelve square wave output.

B. Divide-By-Two and Divide-By-Six Counter – No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. The $\overline{CP}_1$ input is used to obtain divide-by-three operation at the Q_1 and Q_2 outputs and divide-by-six operation at the Q_3 output.

LS93

A. 4-Bit Ripple Counter – The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the truth table.

B. 3-Bit Ripple Counter – The input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1, Q_2, and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

LS90
MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LS92 AND LS93
MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LS90
BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to Input CP_1 for BCD count.

LS92
TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

Note: Output Q_0 connected to input CP_1.

LS93
TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note: Output Q_0 connected to input CP_1.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
SN54LS90X SN54LS92X SN54LS93X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS90X SN74LS92X SN74LS93X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current MS, MR				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	$\overline{CP}_0$				20		
	$\overline{CP}_1$ (LS93)				20		
	$\overline{CP}_1$ (LS90, LS92)				20		
	MS, MR				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
	$\overline{CP}_0$, $\overline{CP}_1$ (LS93)				0.1		
	$\overline{CP}_1$ (LS90, LS92)				0.1		
I_{IL}	Input LOW Current MS, MR				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	$\overline{CP}_0$				−2.4		
	$\overline{CP}_1$ (LS93)				−1.6		
	$\overline{CP}_1$ (LS90, LS92)				−3.2		
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			9	15	mA	V_{CC} = MAX

NOTES

1. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0$ V, $C_L = 15$ pF

SYMBOL	PARAMETER	LIMITS						UNITS	
		LS90		LS92		LS93			
		MIN	MAX	MIN	MAX	MIN	MAX		
f_{MAX}	$\overline{CP}_0$ Input Count Frequency	32		32		32		MHz	Fig. 1
f_{MAX}	$\overline{CP}_1$ Input Count Frequency	16		16		16		MHz	Fig. 1
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_0 Output		16 18		16 18		16 18	ns	Fig. 1
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_1 Output		16 21		16 21		16 21	ns	
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_2 Output		32 35		16 21		32 35	ns	
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_3 Output		32 35		32 35		51 51	ns	
t_{PLH} t_{PHL}	$\overline{CP}_0$ Input to Q_3 Output		48 50		48 50		70 70	ns	
t_{PLH}	MS Input to Q_0 and Q_3 Outputs		30					ns	Fig. 3
t_{PHL}	MS Input to Q_1 and Q_2Outputs		40					ns	Fig. 2
t_{PHL}	MR Input to Any Output		40		40		40	ns	Fig. 2

AC SET-UP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS						UNITS	
		LS90		LS92		LS93			
		MIN	MAX	MIN	MAX	MIN	MAX		
t_W	$\overline{CP}_0$ Pulse Width	15		15		15		ns	Fig. 1
t_W	$\overline{CP}_1$ Pulse Width	30		30		30		ns	
t_W	MS Pulse Width	15						ns	Fig. 2, 3
t_W	MR Pulse Width	15		15		15		ns	Fig. 2
t_{rec}	Recovery Time MS to $\overline{CP}$	25						ns	Fig. 2, 3
t_{rec}	Recovery Time MR to $\overline{CP}$	25		25		25		ns	Fig. 2

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

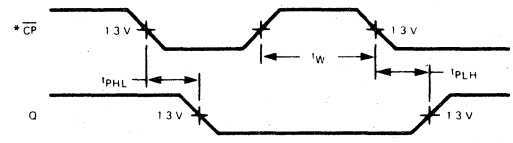


Fig. 1

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.

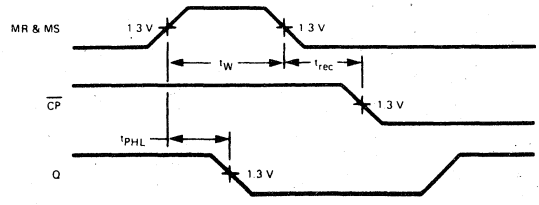


Fig. 2

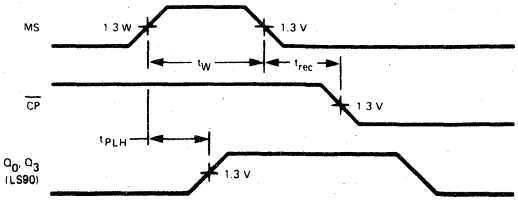


Fig. 3

SN54LS95B/SN74LS95B

4-BIT SHIFT REGISTER

DESCRIPTION — The SN54LS95B/SN74LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH to LOW transition of the appropriate clock input.

The LS95 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

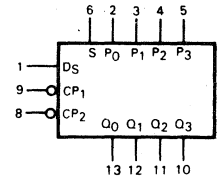
- **SYNCHRONOUS, EXPANDABLE SHIFT RIGHT**
- **SYNCHRONOUS SHIFT LEFT CAPABILITY**
- **SYNCHRONOUS PARALLEL LOAD**
- **SEPARATE SHIFT AND LOAD CLOCK INPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
S	Mode Control Input	0.5 U.L.	0.25 U.L.
D_S	Serial Data Input	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
$\overline{CP}_1$	Serial Clock (Active LOW Going Edge) Input	1.0 U.L.	0.5 U.L.
$\overline{CP}_2$	Parallel Clock (Active LOW Going Edge) Input	1.0 U.L.	0.5 U.L.
$Q_0 - Q_3$	Parallel Outputs (Note b)	10 U.L.	5(2.5) U.L.

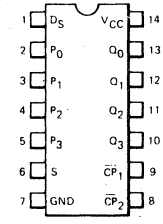
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



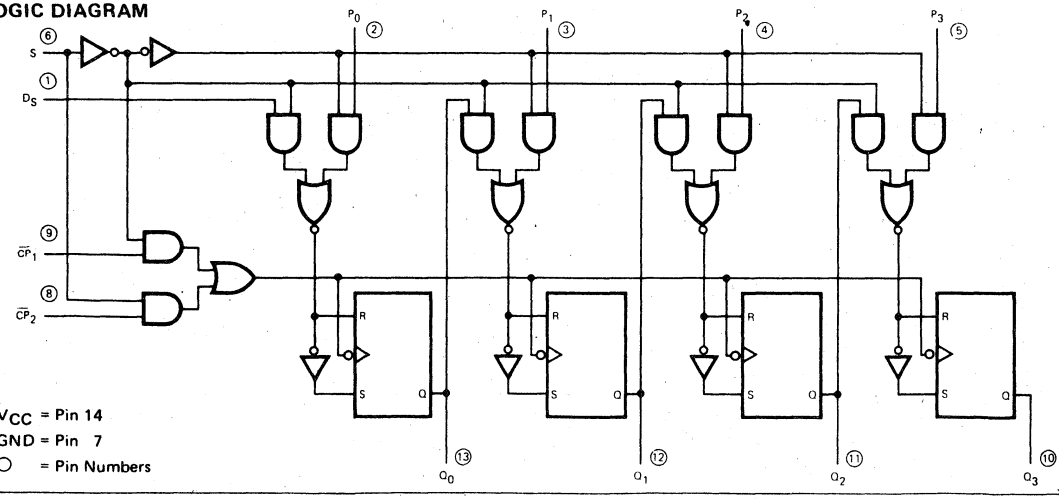
V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION – The LS95 is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial (D_S) and four Parallel ($P_0 - P_3$) Data inputs and four Parallel Data outputs ($Q_0 - Q_3$). The serial or parallel mode of operation is controlled by a Mode Control input (S) and two Clock inputs ($\overline{CP}_1$) and ($\overline{CP}_2$). The serial (right-shift) or parallel data transfers occur synchronous with the HIGH to LOW transition of the selected clock input.

When the Mode Control input (S) is HIGH, $\overline{CP}_2$ is enabled. A HIGH to LOW transition on enabled $\overline{CP}_2$ transfers parallel data from the $P_0 - P_3$ inputs to the $Q_0 - Q_3$ outputs.

When the Mode Control input (S) is LOW, $\overline{CP}_1$ is enabled. A HIGH to LOW transition on enabled $\overline{CP}_1$ transfers the data from Serial input (D_S) to Q_0 and shifts the data in Q_0 to Q_1, Q_1 to Q_2, and Q_2 to Q_3 respectively (right-shift). A left-shift is accomplished by externally connecting Q_3 to P_2, Q_2 to P_1, and Q_1 to P_0, and operating the 9LS95 in the parallel mode (S = HIGH).

For normal operation, S should only change states when both Clock inputs are LOW. However, changing S from LOW to HIGH while $\overline{CP}_2$ is HIGH, or changing S from HIGH to LOW while $\overline{CP}_1$ is HIGH and $\overline{CP}_2$ is LOW will not cause any changes on the register outputs.

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	S	$\overline{CP}_1$	$\overline{CP}_2$	D_S	P_n	Q_0	Q_1	Q_2	Q_3
Shift	L	↓	X	l	X	L	q_0	q_1	q_2
	L	↓	X	h	X	H	q_0	q_1	q_2
Parallel Load	H	X	↓	X	p_n	p_0	p_1	p_2	p_3
Mode Change	↓	L	L	X	X	No Change			
	↑	L	L	X	X	No Change			
	↓	H	L	X	X	No Change			
	↑	H	L	X	X	Undetermined			
	↓	L	H	X	X	Undetermined			
	↑	L	H	X	X	No Change			
	↓	H	H	X	X	Undetermined			
	↑	H	H	X	X	No Change			

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
l = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.
h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.
p_n = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS95BX	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS95BX	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type, W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current $\overline{CP}_1$, $\overline{CP}_2$, D_S, P_0, P_1, P_2, P_3, S				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	$\overline{CP}_1$, $\overline{CP}_2$, D_S, P_0, P_1, P_2, P_3, S				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current $\overline{CP}_1$, $\overline{CP}_2$, D_S, P_0, P_1, P_2, P_3, S				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			13	21	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Shift Frequency	30	40		MHz	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		20 18	27 27	ns	Fig. 1	

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
$t_{W(CP)}$	Clock Pulse Width	20			ns	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
$t_{s(Data)}$	Set-up Time, Data to Clock	20			ns	Fig. 1	
$t_{h(Data)}$	Hold Time, Data to Clock	10			ns	Fig. 1	
t_{sL}	Set up Time, LOW Mode Control to Clock	20			ns	Fig. 2	
t_{hL}	Hold Time, LOW Mode Control to Clock	0			ns	Fig. 2	
t_{sH}	Set-up Time, HIGH Mode Control to Clock	20			ns	Fig. 2	
t_{hH}	Hold Time, HIGH Mode Control to Clock	0			ns	Fig. 2	

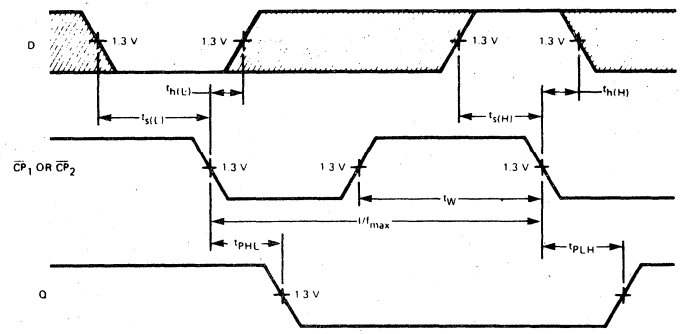
DEFINITIONS OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



*The Data Input is (D_S for $\overline{CP}_1$) or (P_n for $\overline{CP}_2$).

Fig. 1

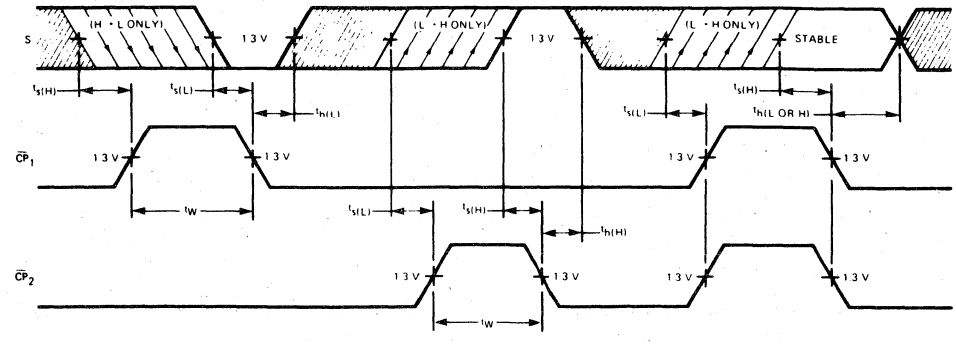


Fig. 2

Advance Information

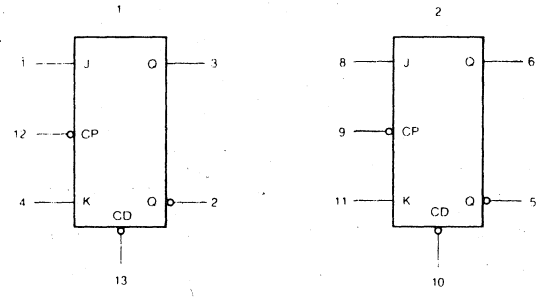
SN54LS107A/SN74LS107A

DUAL JK FLIP-FLOP

DESCRIPTION — the 54LS/74LS107A is a Dual JK Flip-Flop with individual J, K, Direct Clear and Clock Pulse inputs. Output changes are initiated by the HIGH-to-LOW transition of the clock. A LOW signal on CD input overrides the other inputs and makes the Q output LOW.

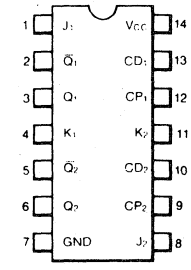
The 54LS/74LS107A is the same as the 54LS/74LS73A but has corner power pins. For electrical characteristics, truth tables and operations information, refer to the 54LS/74LS73A data sheet.

LOGIC SYMBOL



V_{CC} = 14
GND = 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS107AX	4.5 V	5.0 V	5.5 V	-55°C to +125°C
SN74LS107AX	4.75 V	5.0 V	5.25 V	0°C to +70°C

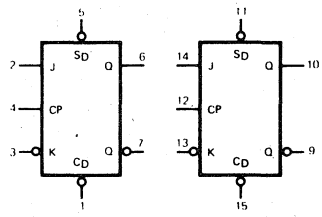
X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

This is advance information and specifications are subject to change without notice.

DUAL JK POSITIVE EDGE-TRIGGERED FLIP-FLOP

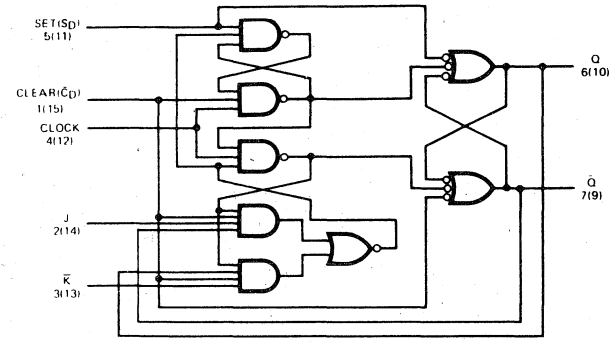
DESCRIPTION – The SN54LS109A/SN74LS109A consists of two high speed completely independent transition clocked J$\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The J$\overline{K}$ design allows operation as a D flip-flop by simply connecting the J and $\overline{K}$ pins together.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS109AX	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS109AX	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA; V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current J, K Clock, Set Clear				20 40 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	J, K Clock, Set Clear				0.1 0.2 0.4	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current J, K Clock, Set Clear				−0.4 −0.8 −1.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	8.0	mA	V_{CC} = MAX, V_{CP} = 0 V

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	$\overline{K}$	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Load "1" (Set)	H	H	h	h	H	L
Hold	H	H	l	h	q	$\overline{q}$
Toggle	H	H	h	l	$\overline{q}$	q
Load "0" (Reset)	H	H	l	l	L	H

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

AC CHARACTERISTICS: T_A = 25°C (See SN54LS73A for Waveforms)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Maximum Clock Frequency		30	45		MHz	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output			9 13	20 30	ns	Fig. 1	
t_{PLH} t_{PHL} t_{PHL}	Propagation Delay, Set or Clear to Output	CP = L CP = H		8 13 13	15 25 35	ns	Fig. 2	

AC SET-UP REQUIREMENTS: T_A = 25°C (See SN54LS73A for Waveforms)

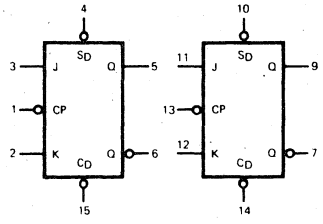
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_WCP(H)	Clock Pulse Width (HIGH)	18	12		ns	Fig. 1	V_{CC} = 5.0 V
t_W	Set or Clear Pulse Width	15	10		ns	Fig. 2	
t_s(H)	Set-up Time HIGH, Data to Clock	18	12		ns	Fig. 1	
t_h(H)	Hold Time HIGH, Data to Clock	0	−13		ns		
t_s(L)	Set-up Time LOW, Data to Clock	20	13		ns		
t_h(L)	Hold Time LOW, Data to Clock	0	−12		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

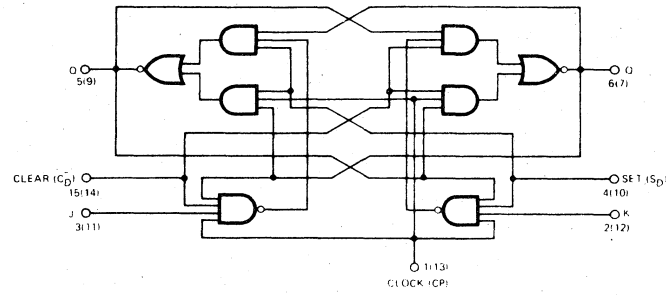
DESCRIPTION — The SN54LS112A/SN74LS112A dual JK flip-flop features individual J, K, clock, and asynchronous set and clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up and hold time are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM
(EACH FLIP-FLOP)



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS112AX	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS112AX	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA; V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current J, K Set, Clear Clock				 20 60 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	J, K Set, Clear Clock				0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current J, K Set, Clear Clock				 −0.4 −0.8 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	6.0	mA	V_{CC} = MAX, V_{CP} = 0 V

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

AC CHARACTERISTICS: $T_A = 25°C$ (See SN54LS73A for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 3	
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		11 16	20 20	ns	Fig. 3	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Set or Clear to Output		11 16	20 20	ns	Fig. 2	

AC SET-UP REQUIREMENTS: $T_A = 25°C$ (See SN54LS73A for Waveforms)

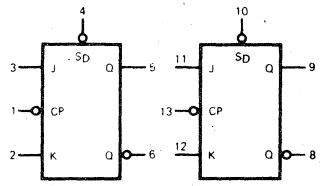
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
$t_W^{CP(H)}$	Clock Pulse Width (HIGH)	18	12		ns	Fig. 3	
$t_W^{CP(L)}$	Clock Pulse Width (LOW)	15	10		ns		
t_W	Set or Clear Pulse Width	15	10		ns	Fig. 2	
$t_s(H)$	Set-up Time HIGH, J or K to Clock	20	13		ns		V_{CC} = 5.0 V
$t_h(H)$	Hold Time HIGH, J or K to Clock	0	−10		ns	Fig. 3	
$t_s(L)$	Set-up Time LOW, J or K to Clock	15	10		ns		
$t_h(L)$	Hold Time LOW, J or K to Clock	0	−13		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

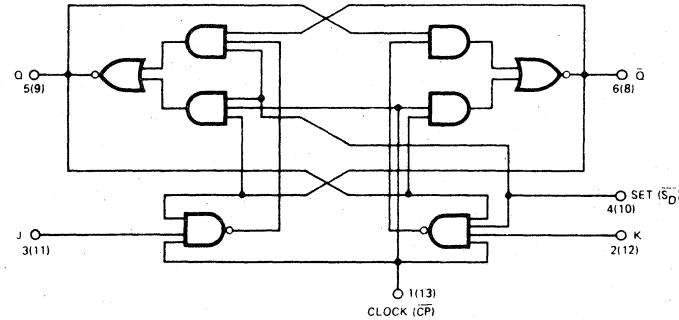
DESCRIPTION — The SN54LS113A/SN74LS113A offers individual J, K, set, and clock inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

LOGIC DIAGRAM
(EACH FLIP-FLOP)



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS113AX	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS113AX	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA; V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current J, K Set Clock				 20 60 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	J, K Set Clock				0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current J, K Set Clock				 −0.4 −0.8 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	6.0	mA	V_{CC} = MAX, V_{CP} = 0 V

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{S}_D$	J	K	Q	$\overline{Q}$
Set	L	X	X	H	L
Toggle	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	l	h	L	H
Load "1" (Set)	H	h	l	H	L
Hold	H	l	l	q	$\overline{q}$

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

AC CHARACTERISTICS: T_A = 25°C (See SN54LS73A for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 3	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		11 16	20 20	ns	Fig. 3	
t_{PLH} t_{PHL}	Propagation Delay, Set to Output		11 16	20 20	ns	Fig. 2	

AC SET-UP REQUIREMENTS: T_A = 25°C (See SN54LS73A for Waveforms)

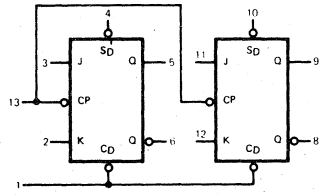
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_WCP(H)	Clock Pulse Width (HIGH)	18	12		ns	Fig. 3	V_{CC} = 5.0 V
t_WCP(L)	Clock Pulse Width (LOW)	15	10		ns		
t_W	Set Pulse Width	15	10		ns	Fig. 2	
t_s(H)	Set-up Time HIGH, J or K to Clock	20	13		ns	Fig. 3	
t_h(H)	Hold Time HIGH, J or K to Clock	0	−10		ns		
t_s(L)	Set-up Time LOW, J or K to Clock	15	10		ns		
t_h(L)	Hold Time LOW, J or K to Clock	0	−13		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

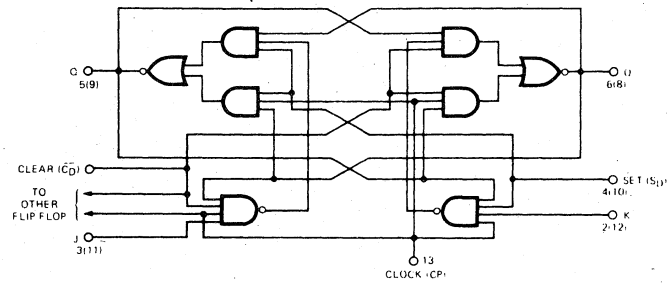
DESCRIPTION — The SN54LS114A/SN74LS114A offers common clock and common clear inputs and individual J, K, and set inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

LOGIC DIAGRAM
(EACH FLIP-FLOP)



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS114AX	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS114AX	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA; V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current J, K Set Clear Clock				 20 60 120 160	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	 J, K Set Clear Clock				 0.1 0.3 0.6 0.8	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current J, K Set Clear Clock				 −0.4 −0.8 −1.6 −1.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	6.0	mA	V_{CC} = MAX, V_{CP} = 0 V

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

AC CHARACTERISTICS: T_A = 25°C (See SN54LS73A for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 3	
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		11 16	20 20	ns	Fig. 3	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Set or Clear to Output		11 16	20 20	ns	Fig. 2	

AC SET-UP REQUIREMENTS: T_A = 25°C (See SN54LS73A for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_WCP(H)	Clock Pulse Width (HIGH)	18	12		ns	Fig. 3	
t_WCP(L)	Clock Pulse Width (LOW)	15	10		ns		
t_W	Set or Clear Pulse Width	15	10		ns	Fig. 2	
t_s(H)	Set-up Time HIGH, J or K to Clock	20	13		ns	Fig. 3	V_{CC} = 5.0 V
t_h(H)	Hold Time HIGH, J or K to Clock	0	−10		ns		
t_s(L)	Set-up Time LOW, J or K to Clock	15	10		ns		
t_h(L)	Hold Time LOW, J or K to Clock	0	−13		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

SN54LS122/SN74LS122 • SN54LS123/SN74LS123

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

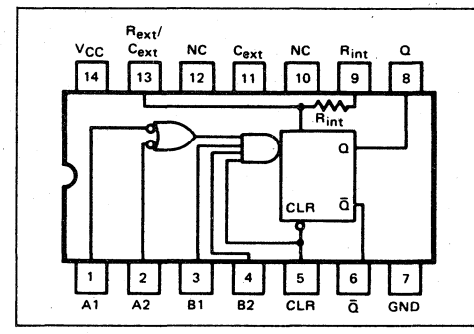
Advance Information

DESCRIPTION – These d-c triggered multivibrators feature pulse width control by three methods. The basic pulse width is programmed by selection of external resistance and capacitance values. The LS122 has an internal timing resistor that allows the circuits to be used with only an external capacitor. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear.

The LS122 and LS123 have Schmitt trigger inputs to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

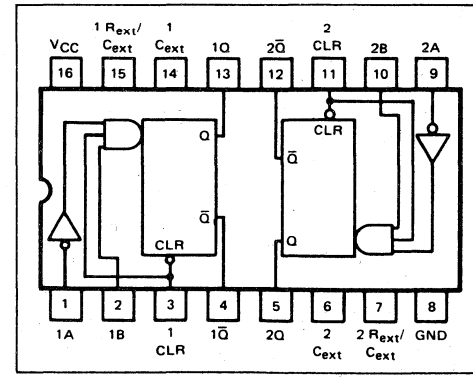
- **OVERRIDING CLEAR TERMINATES OUTPUT PULSE**
- **COMPENSATED FOR V_{CC} AND TEMPERATURE VARIATIONS**
- **D-C TRIGGERED FROM ACTIVE-HIGH OR ACTIVE-LOW GATED LOGIC INPUTS**
- **RETRIGGERABLE FOR VERY LONG OUTPUT PULSES, UP TO 100% DUTY CYCLE**
- **INTERNAL TIMING RESISTORS ON LS122**

SN54LS122, SN74LS122
(TOP VIEW) (SEE NOTES 1 THRU 4)



NC - No internal connection.

SN54LS123, SN74LS123
(TOP VIEW) (SEE NOTES 1 THRU 4)



LS122
FUNCTIONAL TABLE

INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\overline{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎
↑	L	X	H	H	⎍	⎎
↑	X	L	H	H	⎍	⎎

LS123
FUNCTIONAL TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

NOTES: 1. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
2. To use the internal timing resistor of the LS122, connect R_{int} to V_{CC}.
3. For improved pulse width accuracy connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.
4. To obtain variable pulse widths, connect an external variable resistance between R_{int}/C_{ext} and V_{CC}.

This is advance information and specifications are subject to change without notice.

SN54LS124/SN74LS124
DUAL VOLTAGE-CONTROLLED OSCILLATORS
Advance Information

DESCRIPTION – The SN54LS/74LS124 features two independent voltage-controlled oscillators (VCO) in a single package. The frequency of each VCO is established by an external component, either a capacitor or a crystal, in combination with two voltage-sensitive inputs, one for frequency range and one for frequency control. These highly stable oscillators can be set to operate at any frequency typically between 0.12 Hz and 30 MHz. The output frequency can be approximated as follows:

$$f_o = \frac{1 \times 10^{-4}}{C_{ext}}$$

where: f_o = output frequency in hertz

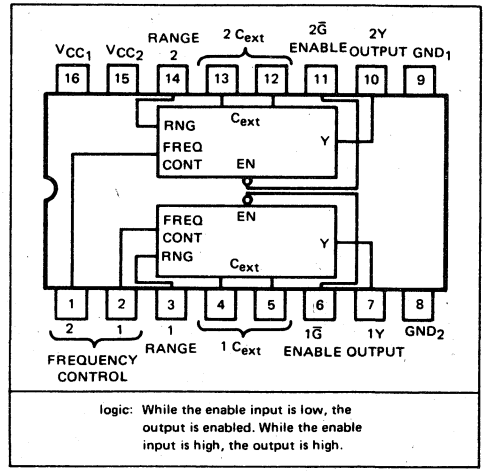
C_{ext} = external capacitance in farads.

These devices operate from a single 5-volt supply. However, a set of supply-voltage and ground pins (V_{CC1} and GND_1) are provided for the enable, synchronization-gating, and output sections, and an additional set (V_{CC2} and GND_2) is provided for the oscillator and associated frequency-control circuits so that isolation can be accomplished in the system.

The enable input starts or stops the output pulses when it is low or high, respectively. The oscillator section runs continuously even while the output is disabled. The enable input is one standard load.

The pulse synchronization-gating section ensures that the first pulse is neither clipped nor extended. Duty cycle of the square-wave output is approximately 50 percent. Operation of both VCO's in the same package is not recommended.

(TOP VIEW)



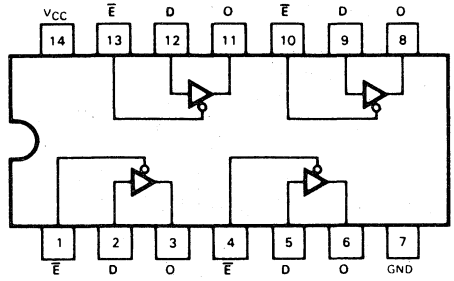
logic: While the enable input is low, the output is enabled. While the enable input is high, the output is high.

- **TWO INDEPENDENT VCO'S IN A 16-PIN PACKAGE**
- **SEPARATE SUPPLY VOLTAGE PINS FOR ISOLATION OF FREQUENCY CONTROL INPUTS AND OSCILLATORS FROM OUTPUT CIRCUITRY**
- **OUTPUT FREQUENCY SET BY ONE EXTERNAL COMPONENT:**
  - **CRYSTAL FOR HIGH-STABILITY FIXED-FREQUENCY OPERATION**
  - **CAPACITOR FOR FIXED- OR VARIABLE-FREQUENCY OPERATION**
- **HIGHLY STABLE OPERATION OVER SPECIFIED TEMPERATURE AND/OR SUPPLY VOLTAGES**

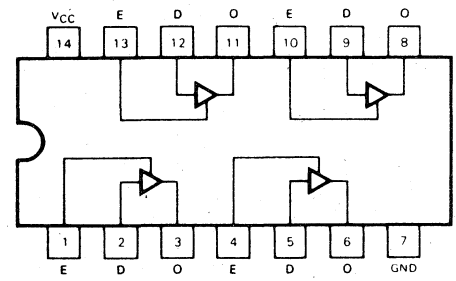
GUARANTEED FREQUENCY SPECTRUM	TYPICAL f_{max}	TYPICAL POWER DISSIPATION
1 Hz to 20 MHz	30 MHz	150 mW

This is advance information and specifications are subject to change without notice.

QUAD 3-STATE BUFFERS WITH ACTIVE HIGH ENABLES



LS125A



LS126A

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS125AX SN54LS126AX	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS125AX SN74LS126AX	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	I_{OH} = −1.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1		V	I_{OH} = −2.6 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = V_{IL}
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, V_E = V_{IL}
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−30		−130	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current, Outputs LOW	LS125A			16	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 0 V
		LS126A			20	mA	V_{CC} = MAX, V_{IN} = 0 V, V_E = 4.5 V
	Power Supply Current, Outputs Off	LS125A			20	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V
		LS126A			24	mA	V_{CC} = MAX, V_{IN} = 0 V, V_E = 0 V

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

TRUTH TABLES

LS125A

INPUTS		OUTPUT
$\overline{E}$	D	
L	L	L
L	H	H
H	X	(Z)

LS126A

INPUTS		OUTPUT
E	D	
H	L	L
H	H	H
L	X	(Z)

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
(Z) = High Impedance (off)

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output				10 16	ns	Fig. 2	V_{CC} = 5.0 V C_L = 45 pF
t_{PZH}	Output Enable Time to HIGH Level	LS125A			20	ns	Figs. 4, 5	
		LS126A			25			
t_{PZL}	Output Enable Time to LOW Level	LS125A			30	ns	Figs. 3, 5	
		LS126A			35			
t_{PLZ}	Output Disable Time from LOW Level				15	ns	Figs. 3, 5	V_{CC} = 5.0 V C_L = 5 pF R_L = 667 Ω
t_{PHZ}	Output Disable Time from HIGH Level				23	ns	Figs. 4, 5	

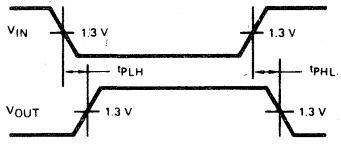


Fig. 1

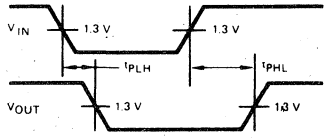


Fig. 2

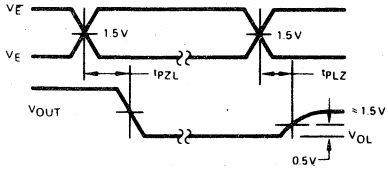


Fig. 3

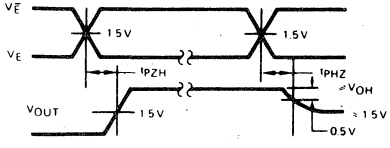
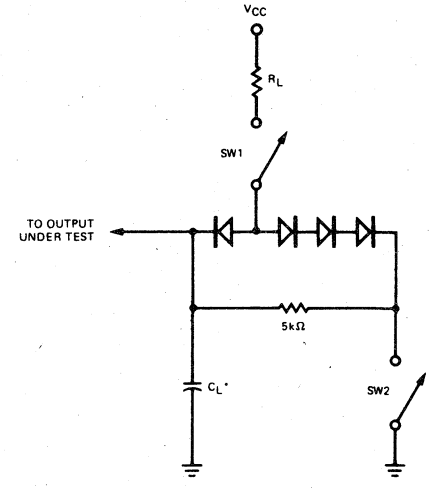


Fig. 4



SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

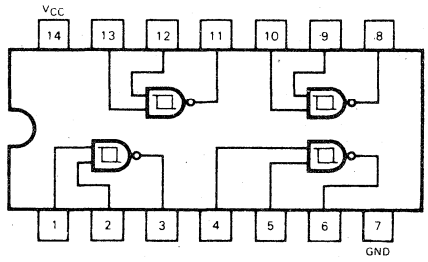
Fig. 5

QUAD 2-INPUT SCHMITT TRIGGER NAND GATE

DESCRIPTION – The SN54LS132/SN74LS132 contains four 2-Input NAND Gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional NAND Gates.

Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as one input remains at a more positive voltage than V_{T+} (MAX), the gate will respond to the transitions of the other input as shown in Figure 1.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



V_{IN} VERSUS V_{OUT}
TRANSFER FUNCTION

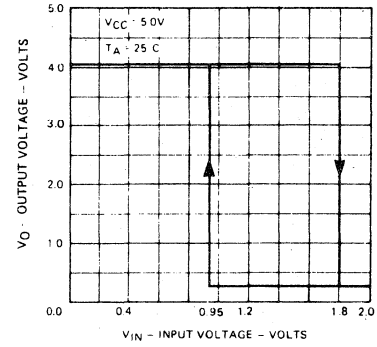


Fig. 1

THRESHOLD VOLTAGE AND HYSTERESIS
VERSUS
POWER SUPPLY VOLTAGE

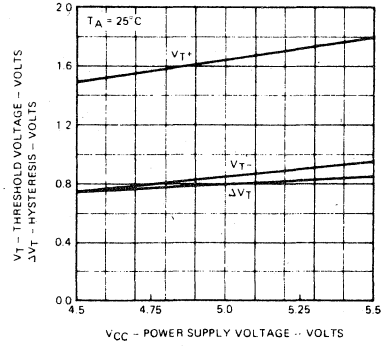


Fig. 2

THRESHOLD VOLTAGE AND HYSTERESIS
VERSUS
TEMPERATURE

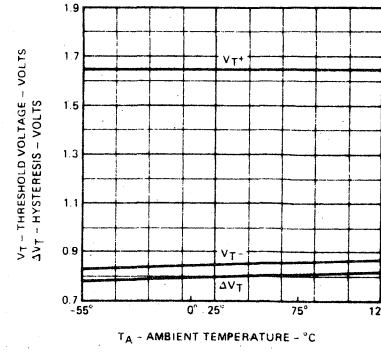


Fig. 3

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS132X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS132X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

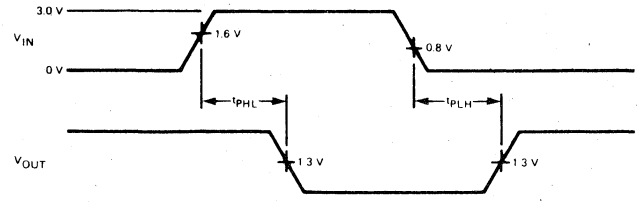
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{T+}	Positive-Going Threshold Voltage		1.5	1.8	2.0	V	V_{CC} = 5.0 V
V_{T-}	Negative-Going Threshold Voltage		0.6	0.95	1.1	V	V_{CC} = 5.0 V
$V_{T+}-V_{T-}$	Hysteresis		0.4	0.8		V	V_{CC} = 5.0 V
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{T+}	Input Current at Positive-Going Threshold			−0.14		mA	V_{CC} = 5.0 V, V_{IN} = V_{T+}
I_{T-}	Input Current at Negative-Going Threshold			−0.18		mA	V_{CC} = 5.0 V, V_{IN} = V_{T-}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			5.9	11	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			8.2	14	mA	V_{CC} = MAX, V_{IN} = 4.5 V

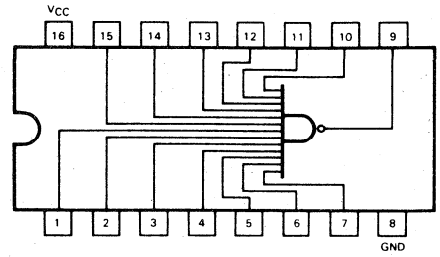
AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output			20	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output			20	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.



13-INPUT NAND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS133X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS133X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

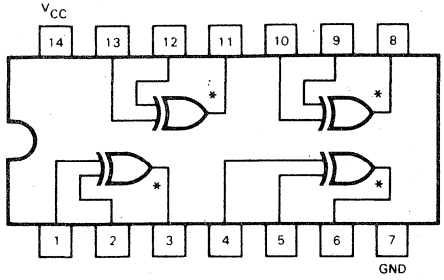
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.35	0.5	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			0.6	1.1	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		20	38	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

QUAD 2-INPUT EXCLUSIVE OR GATE



TRUTH TABLE

IN		OUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

*Open Collector Outputs

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS136X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS136X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V; V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH}
		74		0.35	0.5	V	I_{OL} = 8.0 mA; or V_{IL} per Truth Table
I_{IH}	Input HIGH Current				40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.2	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CC}	Power Supply Current			6.1	10	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, Other Input LOW			23 23	ns	V_{CC} = 5.0 V
t_{PLH} t_{PHL}	Propagation Delay, Other Input HIGH			23 23	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

SN54LS138/SN74LS138

1-OF-8 DECODER/DEMULTIPLEXER

DESCRIPTION – The LSTTL/MSI SN54LS138/SN74LS138 is a high speed 1-of-8 Decoder/Demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LS138 devices or to a 1-of-32 decoder using four LS138s and one inverter. The LS138 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

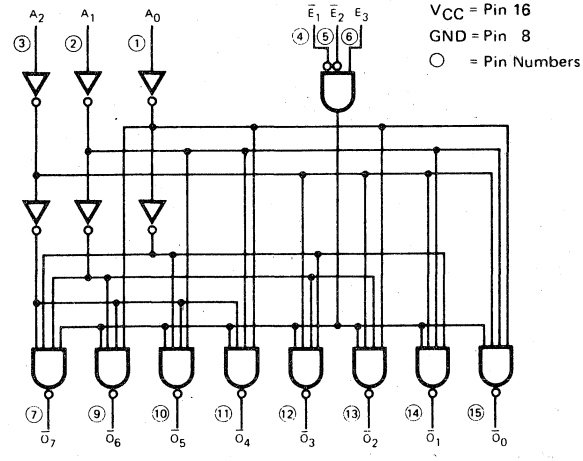
- **DEMULTIPLEXING CAPABILITY**
- **MULTIPLE INPUT ENABLE FOR EASY EXPANSION**
- **TYPICAL POWER DISSIPATION OF 32 mW**
- **ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

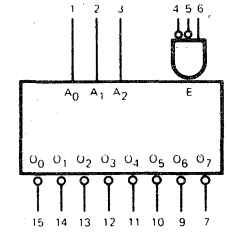
		LOADING (Note a) HIGH	LOW
$A_0 - A_2$	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_1, \overline{E}_2$	Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
E_3	Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0 - \overline{O}_7$	Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM

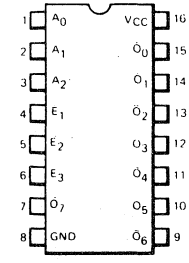


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS138 is a high speed 1-of-8 Decoder/Demultiplexer fabricated with the low power Schottky barrier diode process. The decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled provides eight mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_7$). The LS138 features three Enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four LS138s and one inverter. (See Figure a.)

The LS138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

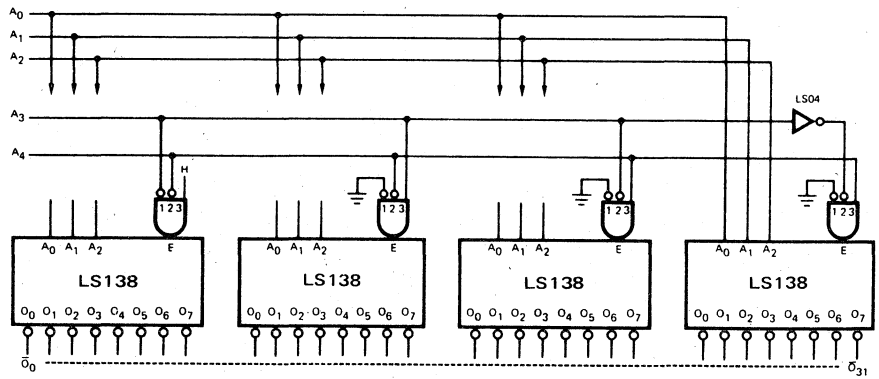


Fig. a.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +5.5 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS138X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS138X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.3	10	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay Address to Output		11 19	18 27	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E_1}$ or $\overline{E_2}$ to Output		9.0 17	15 24	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, E_3 to Output		11 20	18 28	ns	Fig. 1	

AC WAVEFORMS

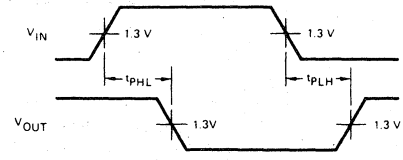


Fig. 1

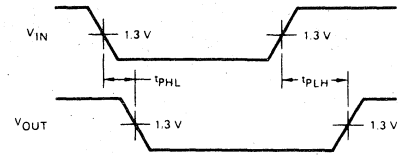


Fig. 2

SN54LS139/SN74LS139

DUAL 1-OF-4 DECODER

DESCRIPTION – The LSTTL/MSI SN54LS139/SN74LS139 is a high speed Dual 1-of-4 Decoder/Demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW outputs. Each decoder has an active LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the LS139 can be used as a function generator providing all four minterms of two variables. The LS139 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

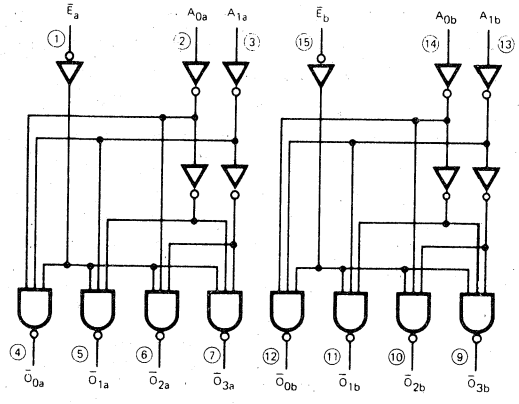
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- TWO COMPLETELY INDEPENDENT 1-OF-4 DECODERS
- ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
A_0, A_1	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0 - \overline{O}_3$	Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

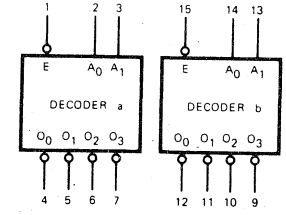
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



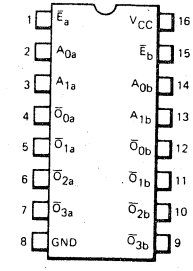
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS139 is a high speed dual 1-of-4 decoder/demultiplexer fabricated with the Schottky barrier diode process. The device has two independent decoders, each of which accept two binary weighted inputs (A_0, A_1) and provide four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). Each decoder has an active LOW Enable ($\overline{E}$). When $\overline{E}$ is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application.

Each half of the LS139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Fig. a, and thereby reducing the number of packages required in a logic network.

TRUTH TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

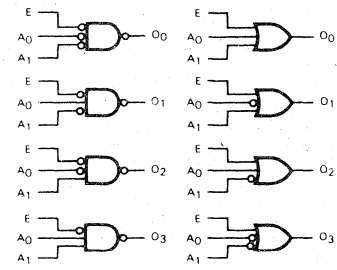


Fig. a

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs, (Output HIGH)	−0.5 V to +5.5 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS139X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS139X	4.75 V	5.0 V	5.25 V	0°C to + 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.8	11	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Address to Output		11 19	18 27	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output		9.0 17	15 24	ns	Fig. 2	

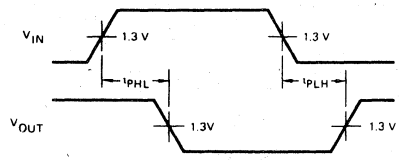


Fig. 1

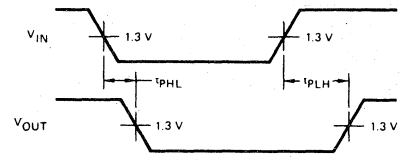


Fig. 2

Advance Information

SN54LS145/SN74LS145

1-OF-10 DECODER/DRIVER -OPEN COLLECTOR

DESCRIPTION — The 54LS/74LS145, 1-of-10 Decoder/driver, is designed to accept BCD inputs and provide appropriate outputs to drive 10-digit incandescent displays. All outputs remain off for all invalid binary input conditions. It is designed for use as indicator/relay drivers or as an open-collector logic circuit driver. Each of the high breakdown output transistors will sink up to 80 mA of current. Typical power dissipation is 35 mW. This device is fully compatible with all TTL families.

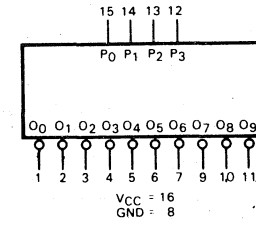
- **LOW POWER VERSION OF 54/74145**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATIBLE**

PIN NAMES

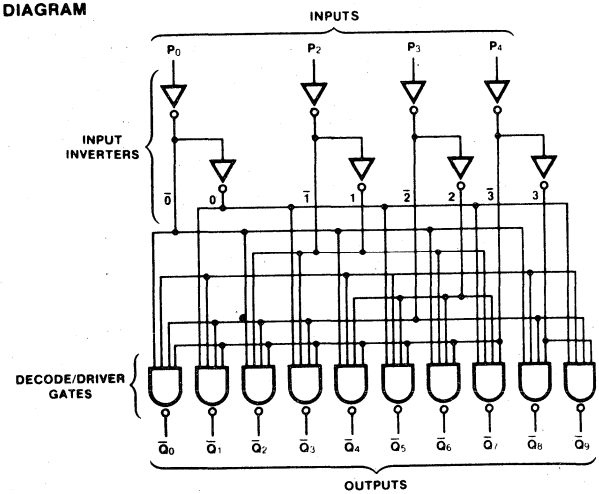
		LOADING (Note a)	
		HIGH	LOW
P_0, P_1, P_2, P_3	BCD Inputs	0.5 U.L.	0.25 U.L.
$\overline{Q}_0$ to $\overline{Q}_9$	Outputs (Note b)	Open Collector	15 (7.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges

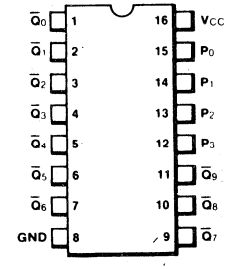
LOGIC SYMBOL



LOGIC DIAGRAM



CONNECTION DIAGRAM DIP (TOP VIEW)



TRUTH TABLE

INPUTS				OUTPUTS									
P_D	P_C	P_B	P_A	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$	$\overline{Q}_8$	$\overline{Q}_9$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS145X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS145X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
I_{OH}	Output HIGH Current				250	μA	V_{CC} = MIN, V_{OH} = 15 V	
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} or V_{IL} per Truth Table
		74		0.35	0.5		I_{OL} = 24 mA	
		54, 74			1.7		I_{OL} = 80 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{CC}	Power Supply Current			7	13	mA	V_{CC} = MAX	

NOTES:
1. Conditions for testing, not shown in the table, are chosen to guarantee operations under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading

AC CHARACTERISTICS T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PHL} t_{PLH}	Propagation Delay P_n Input to Q_n Output			50 50	ns	Figs. 1, 2	V_{CC} = 5.0 V C_L = 45 pF

AC WAVEFORMS

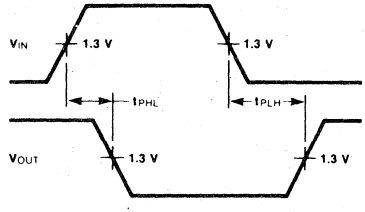


Fig.1

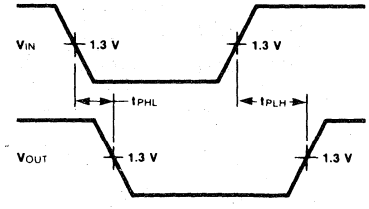


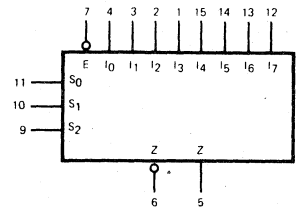
Fig. 2

SN54LS151/SN74LS151
8-INPUT MULTIPLEXER

DESCRIPTION – The TTL/MSI SN54LS151/SN74LS151 is a high speed 8-Input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The LS151 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

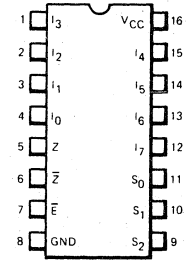
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- ON-CHIP SELECT LOGIC DECODING
- FULLY BUFFERED COMPLEMENTARY OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



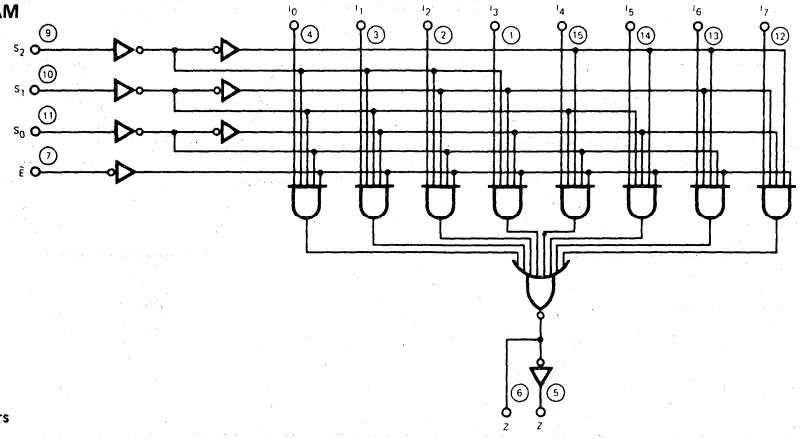
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOW
$S_0 - S_2$	Select Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_0 - I_7$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{Z}$	Complementary Multiplexer Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The LS151 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Enable input (E) is active LOW. When it is not activated, the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E} \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

The LS151 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the LS151 can provide any logic function of four variables and its negation.

TRUTH TABLE

$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS151X	4.5 V	5.0 V	5.5 V	–55°C to +125°C
SN74LS151X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.0	10	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Select to $\overline{Z}$ Output		11 23	20 32	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Z Output		30 18	41 30	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, Enable to $\overline{Z}$ Output		13 17	20 26	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, Enable to Z Output		22 18	33 27	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data to $\overline{Z}$ Output		7.0 10	12 15	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data to Z Output		18 15	26 23	ns	Fig. 2	

AC WAVEFORMS

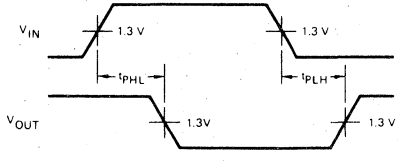


Fig. 1

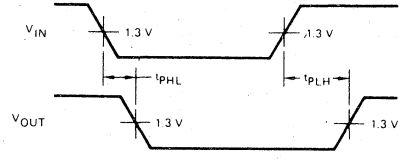


Fig. 2

SN54LS153/SN74LS153

DUAL 4-INPUT MULTIPLEXER

DESCRIPTION — The LSTTL/MSI SN54LS153/SN74LS153 is a very high speed Dual 4-Input Multiplexer with common select inputs and individual enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the LS153 can generate any two functions of three variables. The LS153 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

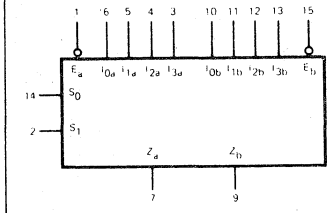
- MULTIFUNCTION CAPABILITY
- NON-INVERTING OUTPUTS
- SEPARATE ENABLE FOR EACH MULTIPLEXER
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
S_0	Common Select Input	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
I_0, I_1	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output (Note b)	10 U.L.	5 (2.5) U.L.

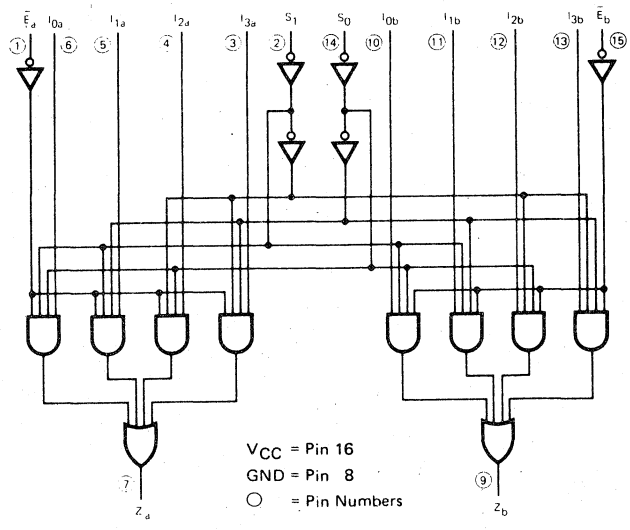
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL

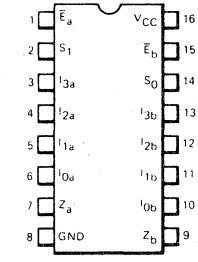


V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS153 is a Dual 4-Input Multiplexer fabricated with Low Power, Schottky barrier diode process for high speed. It can select two bits of data from up to four sources under the control of the common Select Inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW.

The LS153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select Inputs. The logic equations for the outputs are shown below.

$$Z_a = \overline{E}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$
$$Z_b = \overline{E}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

The LS153 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select Inputs. A less obvious application is a function generator. The LS153 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS153X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS153X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.2	10	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay Select to Output		20 16	29 24	ns	Fig. 2	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output		17 14	24 20	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		10 10	15 15	ns	Fig. 2	

AC WAVEFORMS

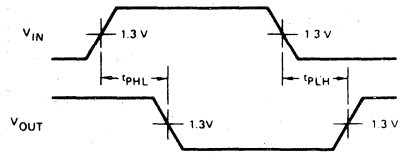


Fig. 1

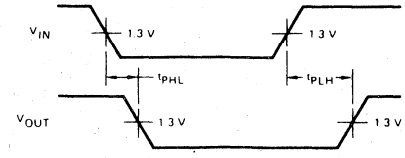


Fig. 2

SN54LS155/SN74LS155
SN54LS156/SN74LS156

DUAL 1-OF-4 DECODER/DEMULTIPLEXER
(LS156 HAS OPEN COLLECTOR OUTPUTS)

DESCRIPTION — The LSTTL/MSI SN54LS155/SN74LS155 and SN54LS156/SN74LS156 are high speed Dual 1-of-4 Decoder/Demultiplexers. These devices have two decoders with common 2-bit Address inputs and separate gated Enable inputs. Decoder "a" has an Enable gate with one active HIGH and one active LOW input. Decoder "b" has two active LOW Enable inputs. If the Enable functions are satisfied, one output of each decoder will be LOW as selected by the address inputs. The LS156 has open collector outputs for wired-OR (DOT-AND) decoding and function generator applications.

The LS155 and LS156 are fabricated with the Schottky barrier diode process for high speed and are completely compatible with all Motorola TTL families.

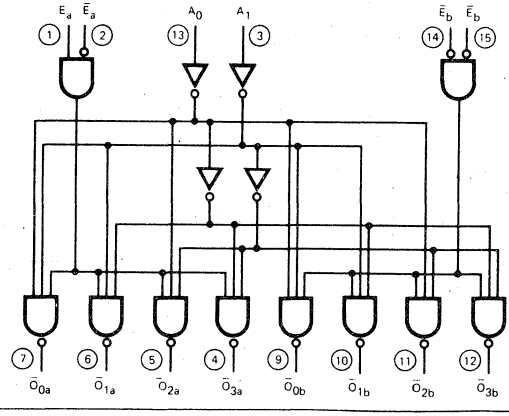
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **COMMON ADDRESS INPUTS**
- **TRUE OR COMPLEMENT DATA DEMULTIPLEXING**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
A_0, A_1	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_a$, $\overline{E}_b$	Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
E_a	Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0 - \overline{O}_3$	Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

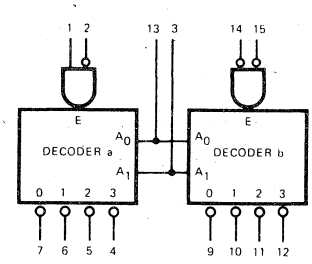
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The HIGH level drive for the LS156 must be established by an external resistor.

LOGIC DIAGRAM



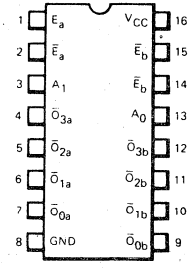
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS155 and LS156 are Dual 1-of-4 Decoder/Demultiplexers with common Address inputs and separate gated Enable inputs. When enabled, each decoder section accepts the binary weighted Address inputs (A_0, A_1) and provides four mutually exclusive active LOW outputs ($\overline{O}_0$–$\overline{O}_3$). If the Enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

Each decoder section has a 2-input enable gate. The enable gate for Decoder "a" requires one active HIGH input and one active LOW input ($E_a \cdot \overline{E}_a$). In demultiplexing applications, Decoder "a" can accept either true or complemented data by using the $\overline{E}_a$ or E_a inputs respectively. The enable gate for Decoder "b" requires two active LOW inputs ($\overline{E}_b \cdot \overline{E}_b$). The LS155 or LS156 can be used as a 1-of-8 Decoder/Demultiplexer by tying E_a to $\overline{E}_b$ and relabeling the common connection as (A_2). The other $\overline{E}_b$ and $\overline{E}_a$ are connected together to form the common enable.

The LS155 and LS156 can be used to generate all four minterms of two variables. These four minterms are useful in some applications replacing multiple gate functions as shown in Fig. a. The LS156 has the further advantage of being able to AND the minterm functions by tying outputs together. Any number of terms can be wired-AND as shown below.

$$f = (E + A_0 + A_1) \cdot (E + \overline{A}_0 + A_1) \cdot (E + A_0 + \overline{A}_1) \cdot (E + \overline{A}_0 + \overline{A}_1)$$

where $E = E_a + \overline{E}_a$; $E = E_b + E_b$

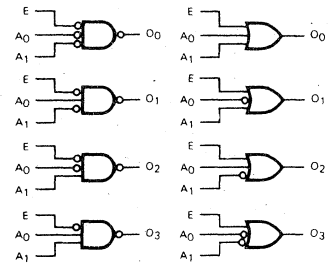


Fig. a

TRUTH TABLE

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A_0	A_1	E_a	$\overline{E}_a$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{E}_b$	$\overline{E}_b$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
SN54LS155X SN54LS156X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS155X SN74LS156X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage LS155 Only	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
I_{OH}	Output HIGH Current LS156 Only				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.1	10	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS				UNITS	TEST CONDITIONS	
		LS155		LS156				
		TYP	MAX	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay, Address to Output	11 19	18 27	18 23	28 33	ns	Fig. 1	$V_{CC} = 5.0$ V $C_L = 15$ pF $R_L = 2$ kΩ (LS156) only
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E}_a$ or $\overline{E}_b$ to Output	9.0 17	15 24	16 21	25 30	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay E_a to Output	11 20	18 28	18 24	28 34	ns	Fig. 1	

AC WAVEFORMS

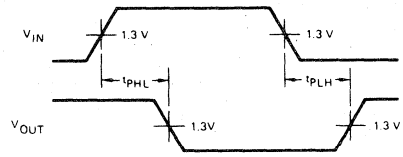


Fig. 1

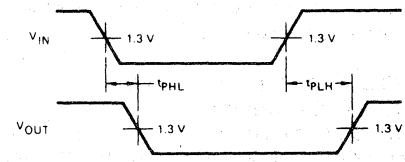


Fig. 2

SN54LS157/SN74LS157

QUAD 2-INPUT MULTIPLEXER

DESCRIPTION – The LSTTL/MSI SN54LS157/SN74LS157 is a high speed Quad 2-Input Multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The LS157 can also be used to generate any four of the 16 different functions of two variables. The LS157 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

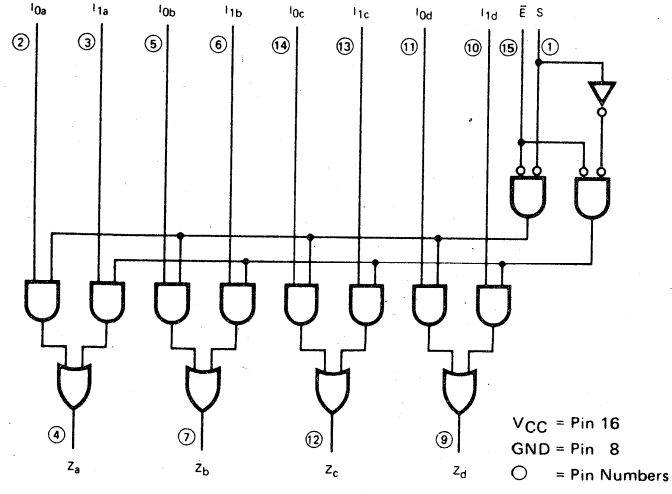
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **NON-INVERTING OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

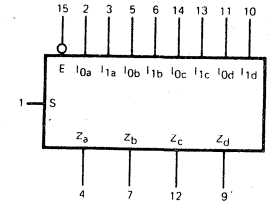
		LOADING (Note a) HIGH	LOW
S	Common Select Input	1.0 U.L.	0.5 U.L.
$\overline{E}$	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
$I_{0a} - I_{0d}$	Data Inputs from Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs from Source 1	0.5 U.L.	0.25 U.L.
$Z_a - Z_d$	Multiplexer Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM

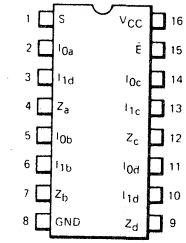


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS157 is a Quad 2-Input Multiplexer fabricated with the Schottky barrier diode process for high speed. It selects four bits of data from two sources under the control of a common Select Input (S). The Enable Input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs.

The LS157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \qquad Z_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$

$$Z_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \qquad Z_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

A common use of the LS157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select Input. A less obvious use is as a function generator. The LS157 can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS157X	4.5 V	5.0 V	5.5 V	–55°C to 125°C
SN74LS157X	4.75 V	5.0 V	5.25 V	0°C to + 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current $\overline{I_0}$, I_1 $\overline{E}$, S				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Input HIGH Current at MAX Input Voltage $\overline{I_0}$, I_1 $\overline{E}$, S				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current $\overline{I_0}$, I_1 $\overline{E}$, S				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			9.7	16	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay Select to Output			23 27	ns	Fig. 2	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output			20 21	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output			14 14	ns	Fig. 2	

AC WAVEFORMS

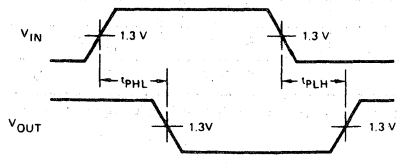


Fig. 1

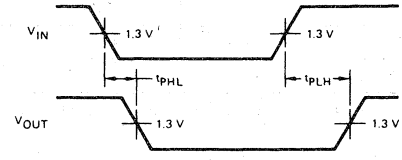


Fig. 2

SN54LS158/SN74LS158

QUAD 2-INPUT MULTIPLEXER

DESCRIPTION – The LSTTL/MSI SN54LS158/SN74LS158 is a high speed Quad 2-Input Multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The LS158 can also generate any four of the 16 different functions of two variables. The LS158 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

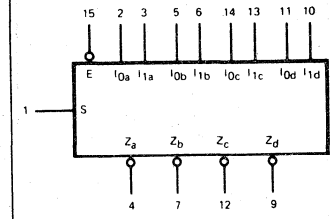
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **INVERTED OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
S	Common Select Input	1.0 U.L.	0.5 U.L.
$\overline{E}$	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
$I_{0a} - I_{0d}$	Data Inputs from Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs from Source 1	0.5 U.L.	0.25 U.L.
$\overline{Z}_a - \overline{Z}_d$	Inverted Outputs (Note b)	10 U.L.	5 (2.5) U.L.

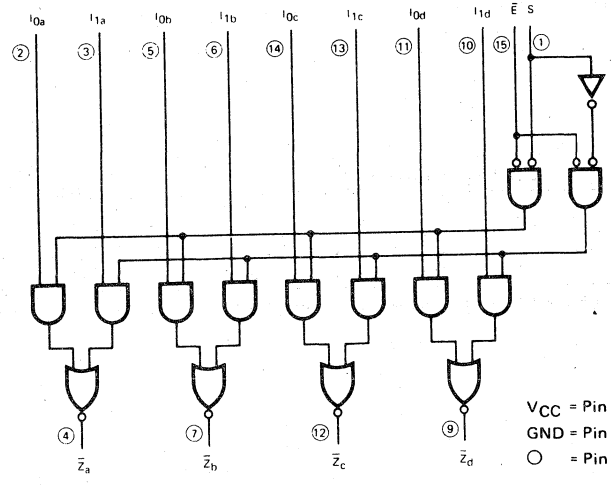
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



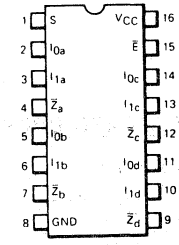
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS158 is a Quad 2-Input Multiplexer fabricated with the Schottky barrier diode process for high speed. It selects four bits of data from two sources under the control of a common Select Input (S) and presents the data in inverted form at the four outputs. The Enable Input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs ($\overline{Z}$) are forced HIGH regardless of all other inputs.

The LS158 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input.

A common use of the LS158 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select Input. A less obvious use is as a function generator. The LS158 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS158X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS158X	4.75 V	5.0 V	5.25 V	0°C to + 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		74	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current I_0, I_1 E, S				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Input HIGH Current at MAX Input Voltage I_0, I_1 E, S				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current I_0, I_1 E, S				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.8	8.0	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay Select to Output			20 24	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output			17 18	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output			12 12	ns	Fig. 1	

AC WAVEFORMS

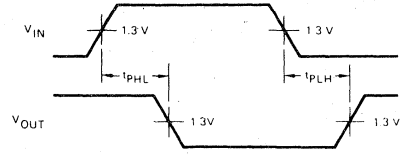


Fig. 1

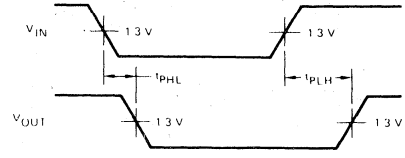


Fig. 2

SN54LS160A/SN74LS160A • SN54LS161A/SN74LS161A
SN54LS162A/SN74LS162A • SN54LS163A/SN74LS163A

BCD DECADE COUNTERS — 4-BIT BINARY COUNTERS

DESCRIPTION — The LS160A/161A/162A/163A are high-speed 4-bit synchronous counters. They are edge-triggered, synchronously presettable, and cascadable MSI building blocks for counting, memory addressing, frequency division and other applications. The LS160A and LS162A count modulo 10 (BCD). The LS161A and LS163A count modulo 16 (binary.)

The LS160A and LS161A have an asynchronous Master Reset (Clear) input that overrides, and is independent of, the clock and all other control inputs. The LS162A and LS163A have a Synchronous Reset (Clear) input that overrides all other control inputs,but is active only during the rising clock edge.

	BCD (Modulo 10)	Binary (Modulo 16)
Asynchronous Reset	LS160A	LS161A
Synchronous Reset	LS162A	LS163A

- SYNCHRONOUS COUNTING AND LOADING
- TWO COUNT ENABLE INPUTS FOR HIGH SPEED SYNCHRONOUS EXPANSION
- TERMINAL COUNT FULLY DECODED
- EDGE-TRIGGERED OPERATION
- TYPICAL COUNT RATE OF 35 MHz
- FULLY TTL AND CMOS COMPATIBLE

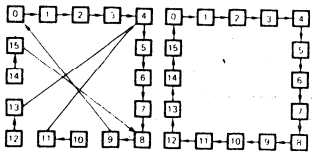
PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{PE}$	Parallel Enable (Active LOW) Input	0.6 U.L.	0.3 U.L.
P_0-P_3	Parallel Inputs	0.5 U.L.	0.25 U.L.
CEP	Count Enable Parallel Input	0.6 U.L.	0.3 U.L.
CET	Count Enable Trickle Input	1.0 U.L.	0.5 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.6 U.L.	0.3 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{SR}$	Synchronous Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_0-Q_3	Parallel Outputs (Note b)	10 U.L.	5 (2.5) U.L.
TC	Terminal Count Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commerical (74) Temperature Ranges.

STATE DIAGRAM

LS160A • LS162A LS161A • LS163A

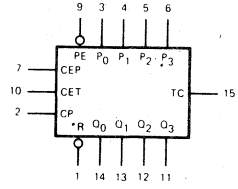


LOGIC EQUATIONS

Count Enable = CEP • CET • PE
TC for LS160A & LS162A = CET • Q_0 • $\overline{Q_1}$ • $\overline{Q_2}$ • Q_3
TC for LS161A & LS163A = CET • Q_0 • Q_1 • Q_2 • Q_3
Preset = $\overline{PE}$ • CP + (rising clock edge)
Reset = $\overline{MR}$ (LS160A & LS161A)
Reset = $\overline{SR}$ • CP + (rising clock edge) (LS162A & LS163A)

NOTE:
The LS160A and LS162A can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14, or 15, it will return to its normal sequence within two clock pulses.

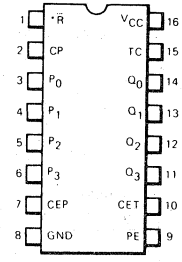
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

*MR for LS160A and LS161A
*SR for LS162A and LS163A

CONNECTION DIAGRAMS
DIP (TOP VIEW)



*MR for LS160A and LS161A
*SR for LS162A and LS163A

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS160A/161A/162A/163A are 4-bit synchronous counters with a synchronous Parallel Enable (Load) feature. These counters consist of four edge-triggered D flip-flops with the appropriate data routing networks feeding the D inputs. All changes of the Q outputs (except due to the asynchronous Master Reset in the LS160A and LS161A) occur as a result of, and synchronous with, the LOW to HIGH transition of the Clock input (CP). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

Three control inputs — Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — select the mode of operation as shown in the tables below. The Count Mode is enabled when the CEP, CET, and $\overline{PE}$ inputs are HIGH. When the $\overline{PE}$ is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW to HIGH transition of the clock. Either the CEP or CET can be used to inhibit the count sequence. With the $\overline{PE}$ held HIGH, a LOW on either the CEP or CET inputs at least one set-up time prior to the LOW to HIGH clock transition will cause the existing output states to be retained. The AND feature of the two Count Enable inputs (CET•CEP) allows synchronous cascading without external gating and without delay accumulation over any practical number of bits or digits.

The Terminal Count (TC) output is HIGH when the Count Enable Trickle (CET) input is HIGH while the counter is in its maximum count state (HLLH for the BCD counters, HHHH for the Binary counters). Note that TC is fully decoded and will, therefore, be HIGH only for one count state.

The LS160A and LS162A count modulo 10 following a binary coded decimal (BCD) sequence. They generate a TC output when the CET input is HIGH while the counter is in state 9 (HLLH). From this state they increment to state 0 (LLLL). If loaded with a code in excess of 9 they return to their legitimate sequence within two counts, as explained in the state diagram. States 10 through 15 do *not* generate a TC output.

The LS161A and LS163A count modulo 16 following a binary sequence. They generate a TC when the CET input is HIGH while the counter is in state 15 (HHHH). From this state they increment to state 0 (LLLL).

The Master Reset ($\overline{MR}$) of the LS160A and LS161A is asynchronous. When the $\overline{MR}$ is LOW, it overrides all other input conditions and sets the outputs LOW. The $\overline{MR}$ pin should never be left open. If not used, the $\overline{MR}$ pin should be tied through a resistor to V_{CC}, or to a gate output which is permanently set to a HIGH logic level.

The active LOW Synchronous Reset ($\overline{SR}$) input of the LS162A and LS163A acts as an edge-triggered control input, overriding CET, CEP and $\overline{PE}$, and resetting the four counter flip-flops on the LOW to HIGH transition of the clock. This simplifies the design from race-free logic controlled reset circuits, e.g., to reset the counter synchronously after reaching a predetermined value.

MODE SELECT TABLE

*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

*For the LS162A and LS163A only.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

*Enter Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS		SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
SN54LS160AX SN54LS162AX	SN54LS161AX SN54LS163AX	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS160AX SN74LS162AX	SN74LS161AX SN74LS163AX	4.75 V	5.0 V	5.25 V	0°C to 70°C

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current $P_0 - P_3$, $\overline{MR}$ $\overline{PE}$, CEP, CP CET, $\overline{SR}$				20 20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	$P_0 - P_3$, MR, $\overline{PE}$, CEP CP CET, $\overline{SR}$				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current $P_0 - P_3$, $\overline{MR}$, CEP, CP CET, $\overline{PE}$, $\overline{SR}$				−0.40 −0.40 −0.80	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH} I_{CCL}	Power Supply Current			18 19	31 32	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C (These parameters apply to all four devices unless otherwise noted)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Turn Off Delay CP to Q Turn On Delay CP to Q		13 18	25 27	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Turn Off Delay CP to TC Turn On Delay CP to TC		15 14	25 21	ns	Fig. 4	
t_{PLH} t_{PHL}	Turn Off Delay CET to TC Turn On Delay CET to TC		9.0 16	14 23	ns	Fig. 3	
t_{PHL}	Turn On Delay $\overline{MR}$ to Q (LS160 and LS161 Only)		18	28	ns	Fig. 2	
f_{count}	Input Count Frequency	25	35		MHz	Fig. 1	

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{rec}	Recovery Time for $\overline{MR}$ (LS160 and LS161 Only)	20			ns	Fig. 2	V_{CC} = 5.0 V
$t_{W\overline{MR}(L)}$	Master Reset Pulse Width (LS160 and LS161 Only)	15	8.0		ns	Fig. 2	
$t_{WCP(H)}$ $t_{WCP(L)}$	Clock Pulse Width (HIGH) Clock Pulse Width (LOW)	15 25	10 18		ns	Fig. 1	
t_s(H) t_s(L)	Set-Up Time (HIGH), Data to Clock Set-Up Time (LOW), Data to Clock	20 20			ns	Fig. 5	
t_h(H) t_h(L)	Hold Time (HIGH), Data to Clock Hold Time (LOW), Data to Clock	3.0 3.0					
t_s(H) t_s(L)	Set-Up Time (HIGH), $\overline{PE}$ or $\overline{SR}$ to Clock Set-Up Time (LOW), $\overline{PE}$ or $\overline{SR}$ to Clock	25 25			ns	Fig. 6	
t_h(H) t_h(L)	Hold Time (HIGH), $\overline{PE}$ or $\overline{SR}$ to Clock Hold Time (LOW), $\overline{PE}$ OR $\overline{SR}$ to Clock	0 0					
t_s(H) t_s(L)	Set-Up Time (HIGH), CE to Clock Set-Up Time (LOW), CE to Clock	25 25			ns	Fig. 7	
t_h(H) t_h(L)	Hold Time (HIGH), CE to Clock Hold Time (LOW), CE to Clock	0 0					

DEFINITION OF TERMS:

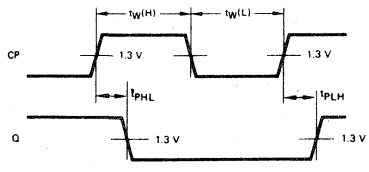
SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) – is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

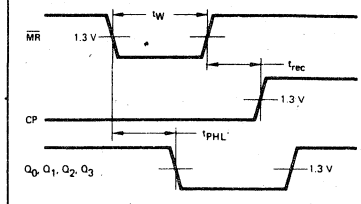
CLOCK TO OUTPUT DELAYS, COUNT FREQUENCY, AND CLOCK PULSE WIDTH.



Other Conditions:
$\overline{PE}$ = $\overline{MR}$ ($\overline{SR}$) = H
CEP = CET = H

Fig. 1

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME.



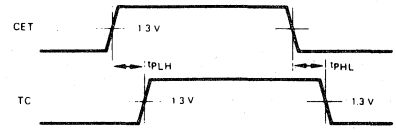
Other Conditions:
$\overline{PE}$ = L
P_0 = P_1 = P_2 = P_3 = H

Fig. 2

AC WAVEFORMS (Cont'd)

COUNT ENABLE TRICKLE INPUT TO TERMINAL COUNT OUTPUT DELAYS

The positive TC pulse occurs when the outputs are in the ($Q_0 \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet Q_3$) state for the LS160 and LS162 and the ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$) state for the LS161 and LS163.

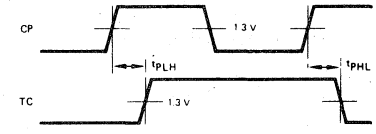


Other Conditions: CP = $\overline{PE}$ = CEP = $\overline{MR}$ = H

Fig. 3

CLOCK TO TERMINAL COUNT DELAYS.

The positive TC pulse is coincident with the output state ($Q_0 \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet Q_3$) for the LS161 and LS163 and ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$) for the LS161 and LS163.

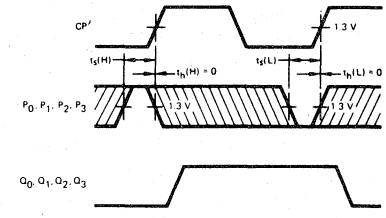


Other Conditions: $\overline{PE}$ = CEP = CET = $\overline{MR}$ = H

Fig. 4

SET-UP TIME (t_s) AND HOLD TIME (t_h) FOR PARALLEL DATA INPUTS.

The shaded areas indicate when the input is permitted to change for predictable output performance.



Other Conditions: $\overline{PE}$ = L, $\overline{MR}$ = H

Fig. 5

SET-UP TIME (t_s) AND HOLD TIME (t_h) FOR COUNT ENABLE (CEP) AND (CET) AND PARALLEL ENABLE ($\overline{PE}$) INPUTS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

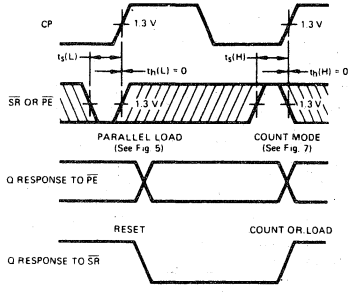
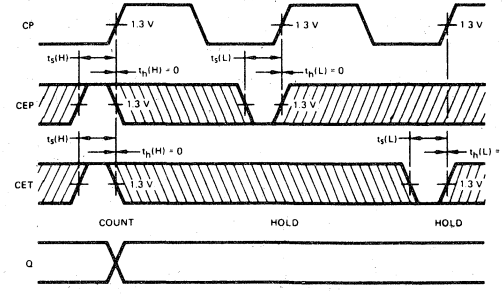


Fig. 6



Other Conditions: $\overline{PE}$ = H, $\overline{MR}$ = H

Fig. 7

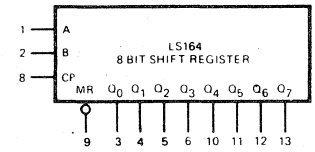
SN54LS164/SN74LS164

SERIAL-IN PARALLEL-OUT SHIFT REGISTER

DESCRIPTION — The SN54LS164/SN74LS164 is a high speed 8-Bit Serial-In Parallel-Out Shift Register. Serial data is entered through a 2-Input AND gate synchronous with the LOW to HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register setting all outputs LOW independent of the clock. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL products.

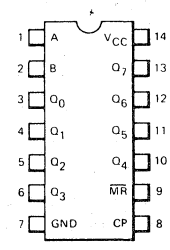
- TYPICAL SHIFT FREQUENCY OF 35 MHz
- ASYNCHRONOUS MASTER RESET
- GATED SERIAL DATA INPUT
- FULLY SYNCHRONOUS DATA TRANSFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM DIP (TOP VIEW)



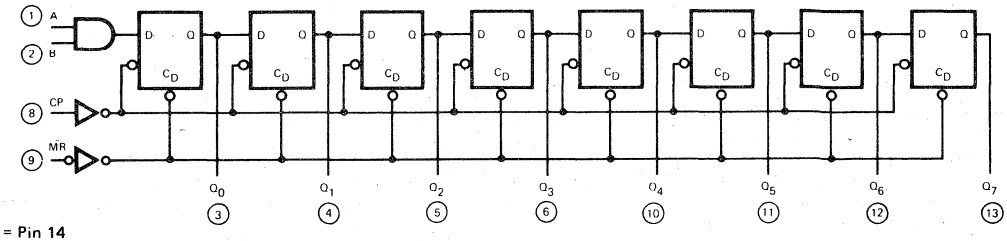
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOW
A, B	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_7$	Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7
○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The LS164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH, or both inputs connected together.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q_0 the logical AND of the two data inputs (A·B) that existed before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	A	B	Q_0	$Q_1 - Q_7$
Reset (Clear)	L	X	X	L	L – L
Shift	H	l	l	L	$q_0 - q_6$
	H	l	h	L	$q_0 - q_6$
	H	h	l	L	$q_0 - q_6$
	H	h	h	H	$q_0 - q_6$

L (l) = LOW Voltage Levels
H (h) = HIGH Voltage Levels
X = Don't Care
q_n = Lower case letters indicate the state of the referenced input or output one set-up time prior to the LOW to HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS164X	4.5 V	5.0 V	5.5 V	–55°C to +125°C
SN74LS164X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type: W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current (Note 5)			16	27	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.
4. Not more than one output should be shorted at a time.
5. I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4 V, and a momentary ground, then 4.5 V applied to clear.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Maximum Clock Frequency	25	35		MHz	Fig. 1	V_{CC} = 5 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going Clock to Outputs		17 21	27 32	ns	Fig. 1	
t_{PHL}	Propagation Delay, Negative-Going $\overline{MR}$ to Outputs		24	36	ns	Fig. 2	

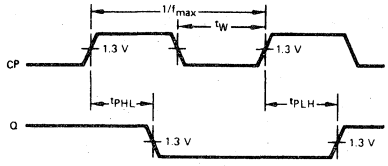
AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_s	Set-Up Time, A or B Input to Positive-Going CP	15			ns	Fig. 3	V_{CC} = 5 V, C_L = 15 pF
t_h	Hold Time, A or B Input to Positive-Going CP	5			ns	Fig. 3	
t_WCP(H)	CP Pulse Width (HIGH)	20			ns	Fig. 1	
t_WCP(L)	CP Pulse Width (LOW)	20			ns	Fig. 1	
$t_W\overline{MR}$(L)	$\overline{MR}$ Pulse Width (LOW)	20			ns	Fig. 2	
t_{rec}	Recovery Time, Positive-Going $\overline{MR}$ to Positive-Going CP	20			ns	Fig. 2	

AC WAVEFORMS

*The shaded areas indicate when the input is permitted to change for predictable output performance.

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



CONDITIONS: $\overline{MR}$ = H

Fig. 1

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME

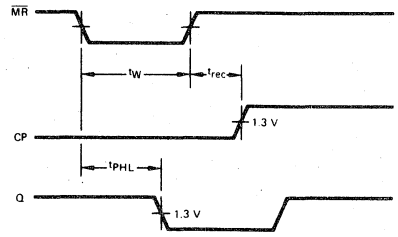


Fig. 2

DATA SET-UP AND HOLD TIMES

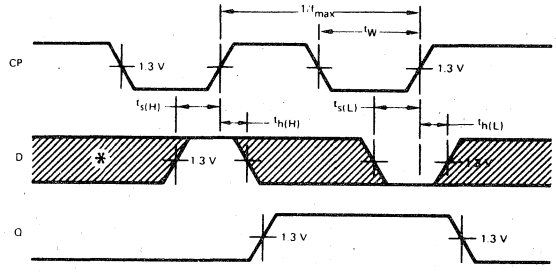


Fig. 3

SN54LS165/SN74LS165

8-BIT PARALLEL-TO-SERIAL CONVERTER

DESCRIPTION—The 54LS/74LS165 is an 8-bit parallel load or serial-in register with complementary outputs available from the last stage. Parallel inputing occurs asynchronously when the Parallel Load ($\overline{PL}$) input is LOW. With $\overline{PL}$ HIGH, serial shifting occurs on the rising edge of the clock; new data enters via the Serial Data (DS) input. The 2-input OR clock can be used to combine two independent clock sources, or one input can act as an active LOW clock enable.

PIN NAMES

		LOADING (Note a) HIGH	LOW
CP_1, CP_2	Clock (LOW-to-HIGH Going Edge) Inputs	0.5 U.L.	0.25 U.L.
$\overline{DS}$	Serial Data Input	0.5 U.L.	0.25 U.L.
$\overline{PL}$	Asynchronous Parallel Load (Active LOW) Input	1.5 U.L.	0.75 U.L.
P_0-P_7	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_7	Serial Output from Last State (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{Q}_7$	Complementary Output (Note b)	10 U.L.	5 (2.5) U.L.

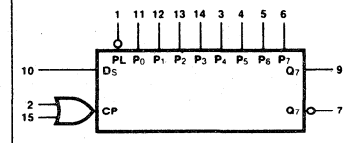
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

TRUTH TABLE

$\overline{PL}$	CP 1	CP 2	CONTENTS Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	$\overline{Q}_7$	RESPONSE
L	X	X	P_0	P_1	P_2	P_3	P_4	P_5	P_6	P_7	Parallel Entry
H	L	↓	D_S	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Right Shift
H	H	↓	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	No Change
H	↓	L	D_S	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Right Shift
H	↓	H	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	No Change

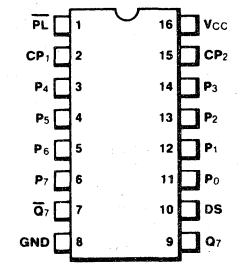
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC SYMBOL



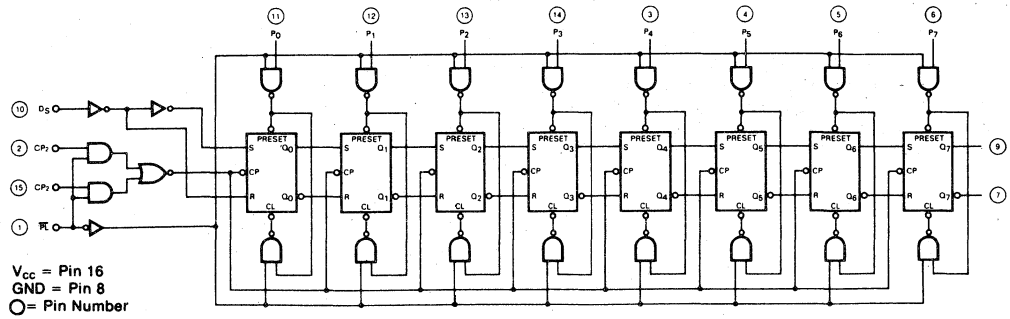
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Number

FUNCTIONAL DESCRIPTION – The 54LS/74LS165 contains eight clocked master/slave RS flip-flops connected as a shift register, with auxiliary gating to provide overriding asynchronous parallel entry. Parallel data enters when the $\overline{PL}$ signal is LOW. The parallel data can change while $\overline{PL}$ is LOW, provided that the recommended set-up and hold times are observed.

For clock operation, $\overline{PL}$ must be HIGH. The two clock inputs perform identically; one can be used as a clock inhibit by applying a HIGH signal. To avoid double clocking, however, the inhibit signal should only go HIGH while the clock is HIGH. Otherwise, the rising inhibit signal will cause the same response as a rising clock edge. The flip-flops are edge-triggered for serial operations. The serial input data can change at any time, provided only that the recommended set-up and hold times are observed, with respect to the rising edge of the clock.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS165X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS165X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5			V	I_{OH} = -400 μA V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7				
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4 mA V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5		I_{OL} = 8 mA
I_{IH}	Input HIGH Current $\overline{CP}$,DS, P_0-P_7 $\overline{PL}$				20 60	μA	V_{CC} = MAX V_{IN} = 2.7 V
	$\overline{CP}$, DS, P_0-P_7 $\overline{PL}$				0.1 0.3	mA	V_{CC} = MAX V_{IN} = 10 V
I_{IL}	Input LOW Current $\overline{CP}$, DS, P_0-P_7 $\overline{PL}$				−0.4 −1.2	mA	V_{CC} = MAX V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX V_{OUT} = 0 V
I_{CC}	Power Supply Current				36	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operations under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Maximum Input Clock Frequency	30	45		MHz	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output			30 30	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{PL}$ to Output			30 30	ns	Fig. 2	

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
T_w	CP Pulse Width	20			ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
T_w	$\overline{PL}$ Pulse Width	15			ns	Fig. 2	
T_sL	Set-Up Time LOW, Data to $\overline{PL}$	10			ns	Fig. 3	
T_hL	Hold Time LOW, Data to $\overline{PL}$	5			ns	Fig. 3	
T_sH	Set-Up Time HIGH, Data to $\overline{PL}$	10			ns	Fig. 3	
T_hH	Hold Time HIGH, Data to $\overline{PL}$	5			ns	Fig. 3	
T_sL	Set-Up Time LOW, Data to Clock	10			ns	Fig. 3	
T_hL	Hold Time LOW, Data to Clock	5			ns	Fig. 3	
T_sH	Set-Up Time HIGH, Data to Clock	10			ns	Fig. 3	
T_hH	Hold Time HIGH, Data to Clock	5			ns	Fig. 3	
T_{rec}	Recovery Time, $\overline{PL}$ to CP	15			ns	Fig. 4	

DEFINITION OF TERMS:

SET-UP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative hold time indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

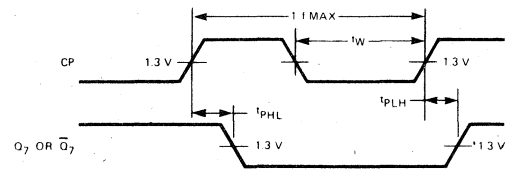


Fig. 1

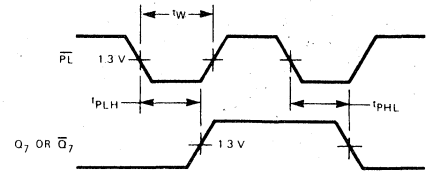


Fig. 2

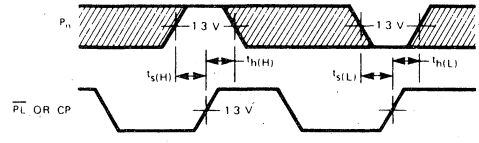


Fig. 3

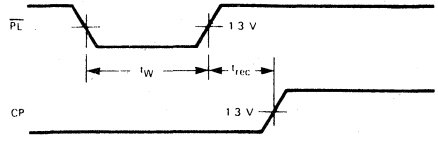


Fig. 4

SN54LS168/SN74LS168 • SN54LS169/SN74LS169

BCD DECADE MODULO 16 BINARY SYNCHRONOUS BI-DIRECTIONAL COUNTERS

DESCRIPTION – The 54LS/74LS168 and 54LS/74LS169 are fully synchronous 4-stage up/down counters featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. The 54LS/74LS168 counts in a BCD decade (8, 4, 2, 1) sequence, while the 54LS/74LS169 operates in a Modulo 16 binary sequence. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

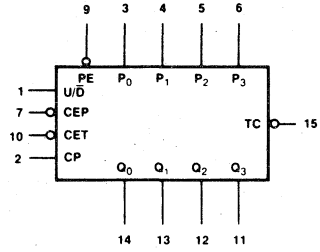
- **LOW POWER DISSIPATION 100mW TYPICAL**
- **HIGH-SPEED COUNT FREQUENCY 30 MHz TYPICAL**
- **FULLY SYNCHRONOUS OPERATION**
- **FULL CARRY LOOKAHEAD FOR EASY CASCADING**
- **SINGLE UP/DOWN CONTROL INPUT**
- **POSITIVE EDGE-TRIGGER OPERATION**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{CEP}$	Count Enable Parallel (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{CET}$	Count Enable Trickle (Active LOW) Input	1.0 U.L.	0.5 U.L.
CP	Clock Pulse (Active positive going edge) Input	0.5 U.L.	0.25 U.L.
$\overline{PE}$	Parallel Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
U/$\overline{D}$	Up-Down Count Control Input	0.5 U.L.	0.25 U.L.
P_0-P_3	Parallel Data Inputs	0.5 U.L.	0.25 U.L
Q_0-Q_3	Flip-Flop Outputs	10 U.L.	5 (2.5) U.L.
$\overline{TC}$	Terminal Count (Active LOW) Output	10 U.L.	5 (2.5) U.L.

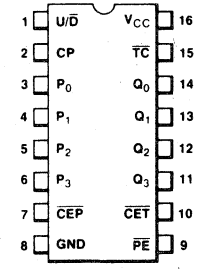
NOTES:
a. 1 TTL Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

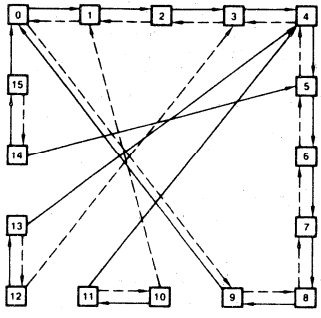
CONNECTION DIAGRAM
DIP (TOP VIEW)



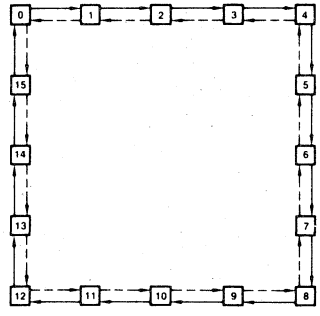
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

STATE DIAGRAMS

F54LS/74LS168
UP/DOWN DECADE COUNTER



F54LS/74LS169



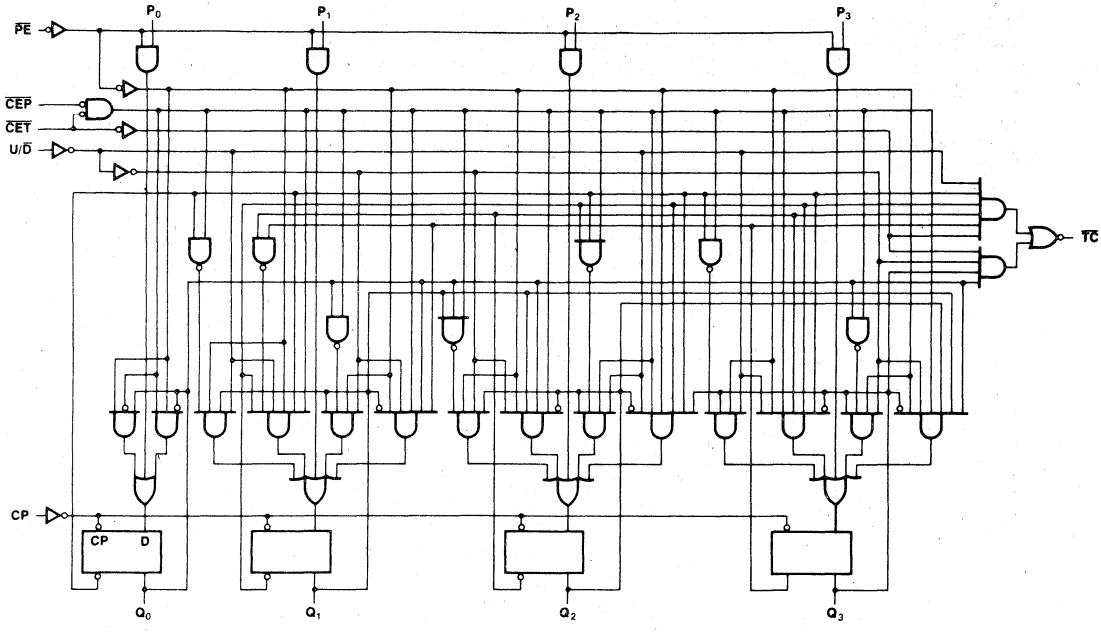
54LS/74LS168
UP: $TC = Q_0 \cdot Q_3 \cdot (U/\overline{D})$
DOWN: $TC = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (U/\overline{D})$

——→ Count Up
— — → Count Down

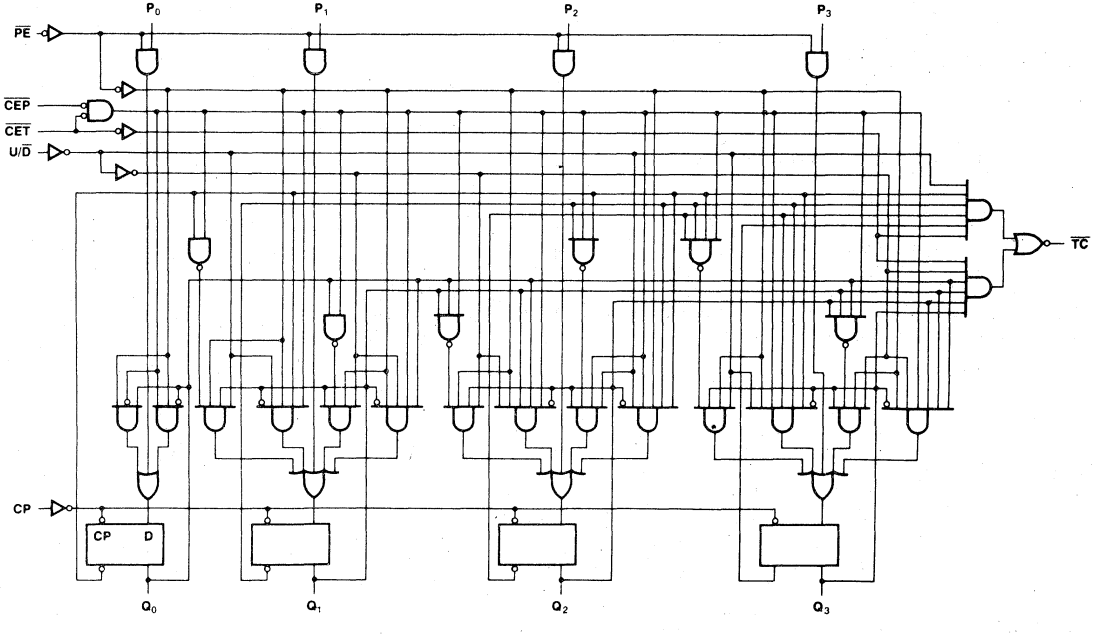
54LS/74LS169
UP: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (U/\overline{D})$
DOWN: $TC = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (U/\overline{D})$

LOGIC DIAGRAMS

54LS/74LS168



54LS/74LS169



FUNCTIONAL DESCRIPTION – The 54LS/74LS168 and 54LS/74LS169 use edge-triggered D-type flip-flops and that have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a set-up time before the rising edge of the clock and remain valid for the recommended hold time thereafter.

The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the P_0-P_3 inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW and $\overline{PE}$ must be HIGH. The U/$\overline{D}$ input then determines the direction of counting.

The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the COUNT DOWN mode or reaches 15 (9 for the 54LS/74LS168) in the COUNT UP mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ output of the 54LS/74LS168 decade counter can also be LOW in the illegal states 11, 13 and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the 54LS/74LS168 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended.

MODE SELECT TABLE

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load (Pn→Qn)
H	L	L	H	Count Up (increment)
H	L	L	L	Count Down (decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = immaterial

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS168/54LS169X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS168/74LS169X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5			
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5		I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current U/$\overline{D}$ CP, $\overline{PE}$ $\overline{CEP}$, P_0-P				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	$\overline{CET}$				40		
	U/$\overline{D}$, CP, $\overline{PE}$, $\overline{CEP}$, P_0-P_3				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
	$\overline{CET}$				0.2		
I_{IL}	Input LOW Current U/$\overline{D}$, CP, $\overline{PE}$, $\overline{CEP}$, P_0-P_3				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	$\overline{CET}$				−0.8		
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			20	34	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the table, are chosen to guarantee operations under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS : T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH}	CP to Q		15	20	ns	Fig. 1	C_L = 15 pF
t_{PHL}			15	20			
t_{PLH}	CP to $\overline{TC}$		22	30	ns	Fig. 3	
t_{PHL}			22	30			
t_{PLH}	$\overline{CET}$ to $\overline{TC}$		10	15	ns	Fig. 2	
t_{PHL}			15	20			
t_{PLH}	U/$\overline{D}$ to $\overline{TC}$		20	25	ns	Fig. 6	
t_{PHL}			20	25			
f_{MAX}	Maximum Clock Frequency	25	32		MHz	Fig. 1	

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
$t_s(L)$ $t_s(H)$	Set-up LOW, Data to CP Set-up HIGH, Data to CP	15 15	12 12		ns	Fig. 4	V_{CC} = 5.0 V
$t_h(L)$ $t_h(H)$	Hold LOW Data to CP Hold HIGH, Data to CP	5.0 5.0	0 0		ns	Fig. 4	
$t_s(L)$ $t_s(H)$	Set-up LOW, $\overline{PE}$ to CP Set-up HIGH, $\overline{PE}$ to CP	15 15	12 12		ns	Fig. 5	
$t_h(L)$ $t_h(H)$	Hold LOW, $\overline{PE}$ to CP Hold HIGH, $\overline{PE}$ to CP	5.0 5.0	0 0		ns	Fig. 5	
$t_s(L)$ $t_s(H)$	Set-up LOW, $\overline{CET}$ or $\overline{CEP}$ to CP Set-up HIGH, $\overline{CET}$ or $\overline{CEP}$ to CP	15 15	12 12		ns	Fig. 5	
$t_h(L)$ $t_h(H)$	Hold LOW, $\overline{CET}$ or $\overline{CEP}$ to CP Set-up HIGH, $\overline{CET}$ or $\overline{CEP}$ to CP	15 15	12 12		ns	Fig. 5	
$t_h(H)$ $t_h(H)$	Set-up LOW, U/$\overline{D}$ to CP Set-up HIGH, U/$\overline{D}$ to CP	25 25	20 20		ns	Fig. 6	
$t_h(L)$ $t_h(H)$	Hold LOW, U/$\overline{D}$ to CP Hold HIGH, U/$\overline{D}$ to CP	0 0	−4.0 −4.0		ns	Fig. 6	
$t_wCP(L)$ $t_wCP(H)$	Clock Pulse Width LOW Clock Pulse Width HIGH	20 10	18 5.0		ns	Fig. 1	

DEFINITION OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, COUNT FREQUENCY, AND CLOCK PULSE WIDTH.

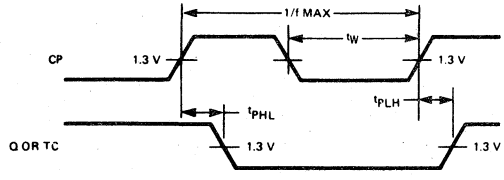


Fig. 1

COUNT ENABLE TRICKLE INPUT TO TERMINAL COUNT OUTPUT DELAYS

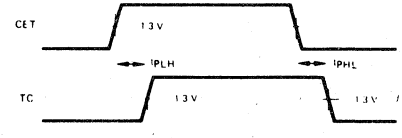


Fig. 2

CLOCK TO TERMINAL DELAYS

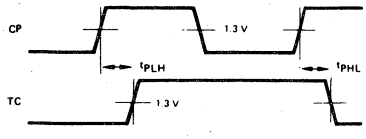


Fig. 3

SET-UP TIME (t_s) AND HOLD (t_h) FOR PARALLEL DATA INPUTS.

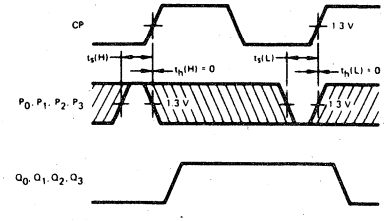
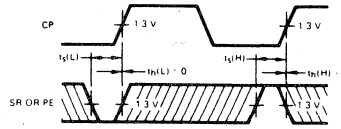
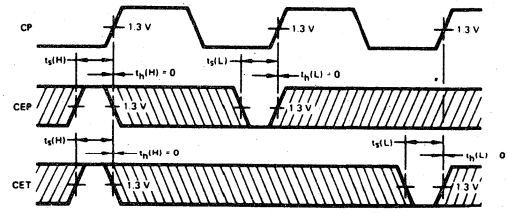


Fig. 4

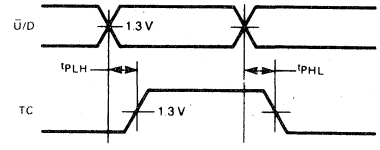


Set-up time (t_s) and hold time (t_h) for count enable (CEP) and (CET), parallel enable (PE) inputs, and up-down (U/D) control inputs.



The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 5



Up-Down input to Terminal Count Output Delays

Fig. 6

SN54LS170/SN74LS170

4×4 REGISTER FILE (O/C)

DESCRIPTION – The TTL/MSI SN54LS170/SN74LS170 is a high-speed, low-power 4 x 4 Register File organized as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

Open collector outputs make it possible to connect up to 128 outputs in a wired-AND configuration to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

The SN54LS670/SN74LS670 provides a similar function to this device but it features 3-state outputs.

- **SIMULTANEOUS READ/WRITE OPERATION**
- **EXPANDABLE TO 512 WORDS OF n-BITS**
- **TYPICAL ACCESS TIME OF 20 ns**
- **LOW LEAKAGE OPEN-COLLECTOR OUTPUTS FOR EXPANSION**
- **TYPICAL POWER DISSIPATION OF 125 mW**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
D_1-D_4	Data Inputs	0.5 U.L.	0.25 U.L.
W_A, W_B	Write Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_W$	Write Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
R_A, R_B	Read Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_R$	Read Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
Q_1-Q_4	Outputs (Note b)	Open Collector	5(2.5) U.L.

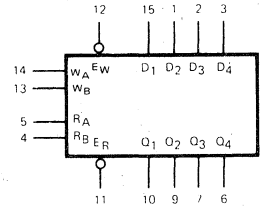
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5.0 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive must be supplied by an external resistor to V_{CC}.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

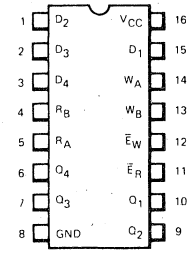
*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

LOGIC SYMBOL



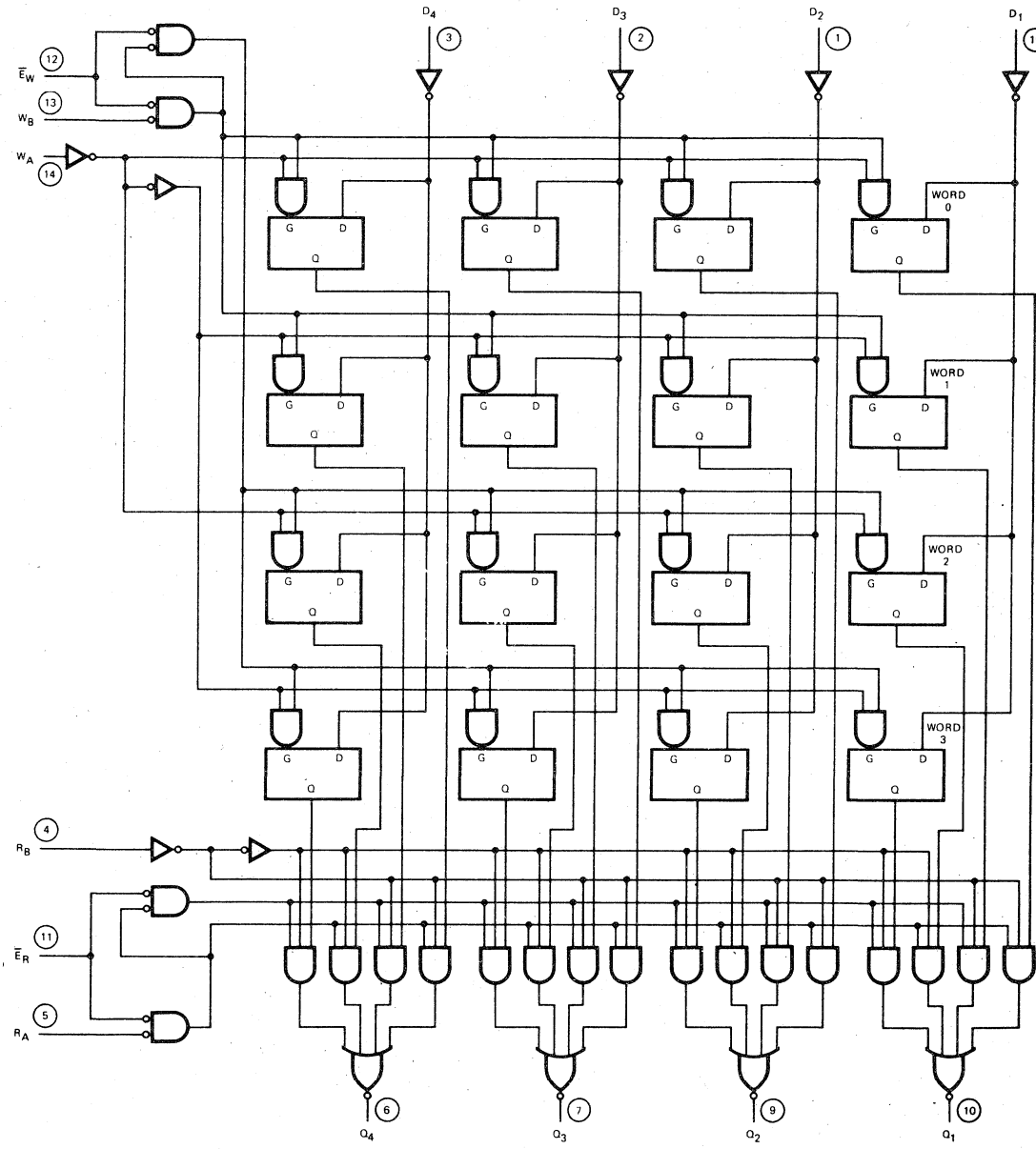
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



○ = Pin Numbers
V_{CC} = Pin 16
GND = Pin 8

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

WRITE INPUTS			WORD			
W_B	W_A	$\overline{E}_W$	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
R_B	R_A	$\overline{E}_R$	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

NOTES: A. H = high level, L = low level, X = irrelevant
B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs
C. Q_0 = the level of Q before the indicated input conditions were established
D. W0B1 = The first bit of word 0, etc

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS170X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS170X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				20	μA	V_{OH} = 5.5 V, V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current Any D, R, or W $\overline{E}_R$ or $\overline{E}_W$				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Any D, R, or W $\overline{E}_R$ or $\overline{E}_W$				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current Any D, R or W $\overline{E}_R$ or $\overline{E}_W$				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CC}	Power Supply Current (Note 4)			25	40	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
4. I_{CC} is measured under the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{E}_R$ to Q Outputs			30 30	ns	Fig. 1	V_{CC} = 5 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, R_A or R_B to Q Outputs			40 40	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{E}_W$ to Q Outputs			45 40	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs to Q Outputs			45 35	ns	Fig. 1	

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_W	Pulse Width (LOW) for $\overline{E}_W$	25			ns	V_{CC} = 5 V Fig. 3
t_sD (Note 5)	Set-Up Time, Data Inputs with Respect to Positive-Going $\overline{E}_W$	10			ns	
t_hD	Hold Time, Data Inputs with Respect to Positive-Going $\overline{E}_W$	15			ns	
t_sW (Note 7)	Set-Up Time, Write Select Inputs W_A and W_B with Respect to Negative-Going $\overline{E}_W$	15			ns	
t_hW	Hold Time, Write Select Inputs W_A and W_B with Respect to Positive-Going $\overline{E}_W$	5			ns	

NOTES:
5. The Data to Enable Set-up Time is defined as the time required for the logic level to be present at the Data input prior to the enable transition from LOW to HIGH in order for the latch to recognize and store the new data.
6. The Hold Time (t_h) is defined as the minimum time following the enable transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition.
7. The Address to Enable Set-up Time is the time before the HIGH to LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
8. The shaded areas indicate when the inputs are permitted to change for predictable output performance.

AC WAVEFORMS

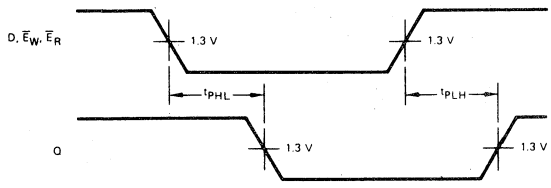


Fig. 1

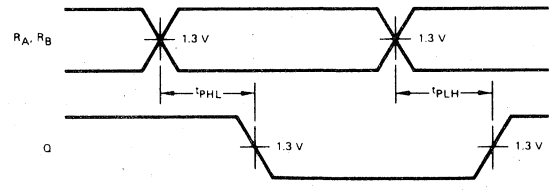


Fig. 2

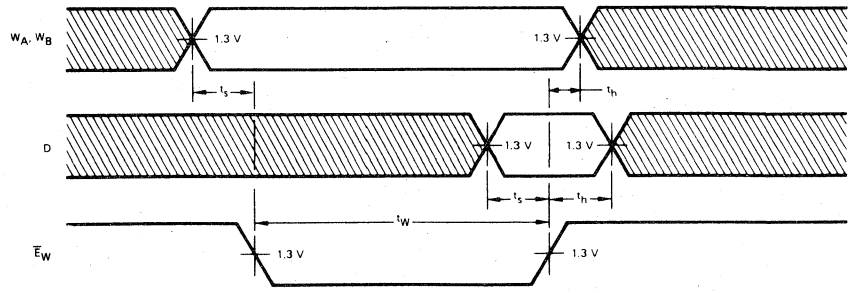


Fig. 3

SN54LS173/SN74LS173

4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUTS

DESCRIPTION — The 54LS/74LS173 is a high-speed 4-Bit Register featuring 3-state outputs for use in bus-organized systems. The clock is fully edge-triggered allowing either a load from the D inputs or a hold (retain register contents) depending on the state of the input Enable lines ($\overline{IE}_1$, $\overline{IE}_2$). A HIGH on either Output Enable line ($\overline{OE}_1$, $\overline{OE}_2$) brings the output to a high impedence state without affecting the actual register contents. A HIGH on the Master Reset (MR) input resets the Register regardless of the state of the Clock (CP), the Output Enable ($\overline{OE}_1$, $\overline{OE}_2$) or the Input Enable ($\overline{IE}_1$, $\overline{IE}_2$) lines.

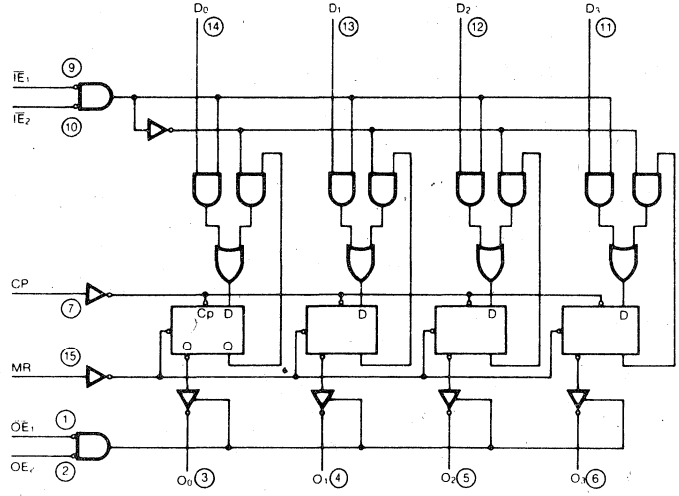
- **FULLY EDGE-TRIGGERED**
- **3-STATE OUTPUTS**
- **GATED INPUT AND OUTPUT ENABLES**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATABLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
$D_0 - D_3$	Data Inputs	0.5 U.L.	0.25 U.L.
$\overline{IE}_1$, $\overline{IE}_2$	Input Enable (Active LOW)	0.5 U.L.	0.25 U.L.
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
CP	Clock Pulse (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
MR	Master Reset Input (Active HIGH)	0.5 U.L.	0.25 U.L.
$O_0 - O_3$	Outputs (Note b)	65 (25) U.L.	5 (2.5) U.L.

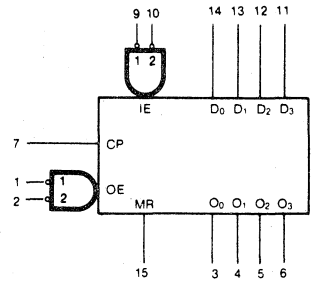
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



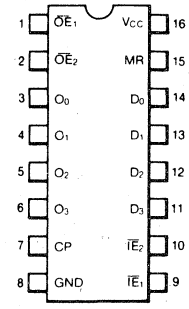
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS173X	4.5 V	5.0 V	5.5 V	-55°C to +125°C
SN74LS173X	4.75 V	5.0 V	5.25 V	0°C to+70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

TRUTH TABLE

MR	CP	$\overline{E}_1$	$\overline{E}_2$	D_n	Q_{n+1}
H	X	X	X	X	L
L	L	X	X	X	Q_n
L	↓	H	X	X	Q_n
L	↓	X	H	X	Q_n
L	↓	L	L	L	L
L	↓	L	L	H	H

When either $\overline{OE}_1$ or $\overline{OE}_2$ are HIGH, the output is in the off state (High Impedence); however this does not affect the contents or sequential operation of the register.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE unless otherwise specified

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			-0.65	-1.5	V	V_{CC} = MIN, I_{IN} = -18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	I_{OH} = -1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1		V	I_{OH} = -2.6 mA	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V, $V_{\overline{E}}$ = 2.0 V	
I_{OZL}	Output Off Current LOW				-20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				-0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{SC}	Output Short Circuit Current (Note 4)		-30		-130	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current				28	mA	V_{CC} = MAX	

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operations under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Maximum Input Clock Frequency	30	45		MHz	Fig. 1	V_{CC} = 5.0 V
t_{PLH} t_{PHL}	Propagation Delay, CP To Output		26 17	40 25	ns	Fig. 1	C_L = 15 pF
t_{PHL}	Propagation Delay, MR To Output		17	25	ns	Fig. 2	
t_{PZH}	Output Enable Time to HIGH Level		13	20	ns	Figs. 4, 5	C_L = 15 pF
t_{PZL}	Output Enable Time to LOW Level		13	20	ns	Figs. 3, 5	R_L = 2 kΩ
t_{PLZ}	Output Disable Time from LOW Level		11	16	ns	Figs. 3, 5	C_L = 5 pF
t_{PHZ}	Output Disable Time from HIGH Level		11	16	ns	Figs. 4, 5	R_L = 2 kΩ

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_w(CP)	Clock Pulse Width	17	11		ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_s(Data)	Set-up Time, Data to Clock	10	7		ns	Fig. 1	
t_h(Data)	Hold Time, Data to Clock	10	7		ns		
$t_s(\overline{IE})$	Set-up Time, $\overline{IE}$ Control to Clock	17	11		ns	Fig. 1	
$t_h(\overline{IE})$	Hold Time, $\overline{IE}$ Control to Clock	2	0		ns		
t_w(MR)	Master Reset Pulse Width	17	11		ns	Fig. 2	
t_{rec}(MR)	Recovery Time, Master Reset to Clock	15	10		ns		

AC WAVEFORMS

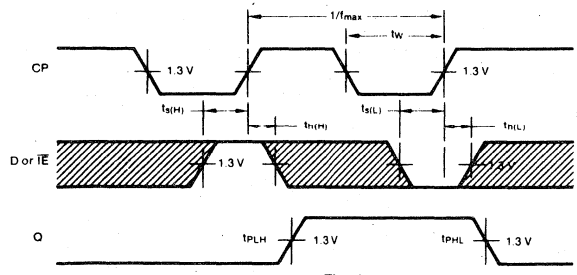


Fig. 1

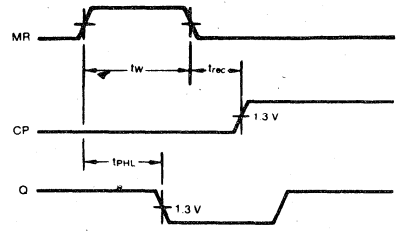


Fig. 2

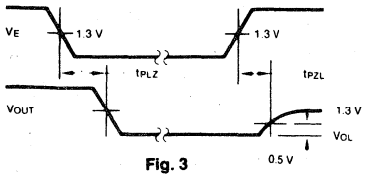


Fig. 3

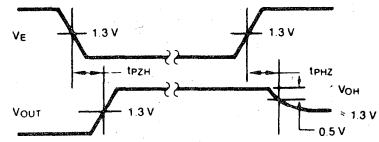
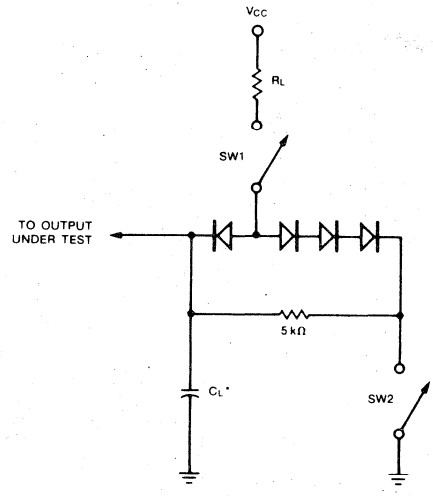


Fig. 4

AC LOAD CIRCUIT



*Includes Jig and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 5

SN54LS174/SN74LS174

HEX D FLIP-FLOP

DESCRIPTION – The LSTTL/MSI SN54LS174/SN74LS174 is a high speed Hex D Flip-Flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW to HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops. The LS174 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

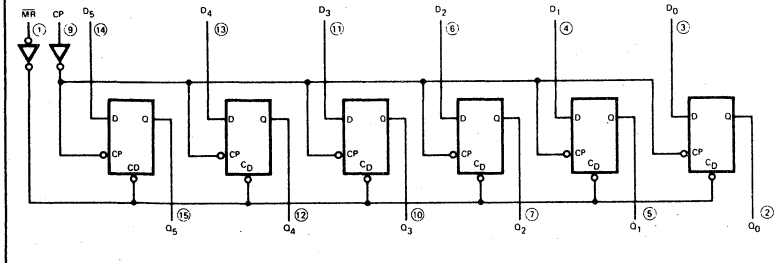
- EDGE-TRIGGERED D-TYPE INPUTS
- BUFFERED-POSITIVE EDGE-TRIGGERED CLOCK
- CLOCK TO OUTPUT DELAYS OF 14 ns
- ASYNCHRONOUS COMMON RESET
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERNATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

		LOADING (Note a) HIGH	LOW
$D_0 - D_5$	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_5$	Outputs (Note b)	10 U.L.	5 (2.5) U.L.

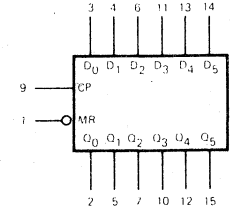
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



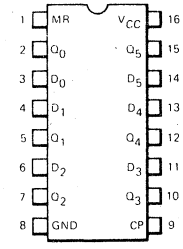
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops.

Each D input's state is transferred to the corresponding flip-flop's output following the LOW to HIGH Clock (CP) transition.

A LOW input to the Master Reset ($\overline{MR}$) will force all outputs LOW independent of Clock or Data inputs. The LS174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

TRUTH TABLE

Inputs (t = n, $\overline{MR}$ = H)	Outputs (t = n+1) Note 1
D	Q
H	H
L	L

Note 1: t = n + 1 indicates conditions after next clock.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS174X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS174X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{SC}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			16	26	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

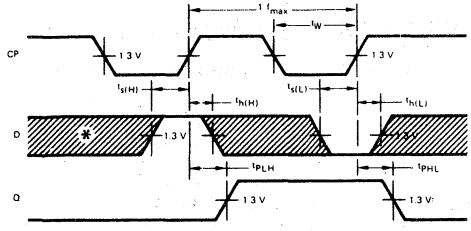
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		12 15	20 22	ns	Fig. 1
t_{PHL}	Propagation Delay, $\overline{MR}$ to Output		20	28	ns	Fig. 2
f_{MAX}	Maximum Input Clock Frequency	30	45		MHz	Fig. 1

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_WCP	Minimum Clock Pulse Width	15	10		ns	Fig. 1
t_s	Set-up Time, Data to Clock (HIGH or LOW)	10			ns	Fig. 1
t_h	Hold Time, Data to Clock (HIGH or LOW)	0			ns	Fig. 1
t_{rec}	Recovery Time for $\overline{MR}$	12	8.0		ns	Fig. 2
$t_W\overline{MR}$	Minimum $\overline{MR}$ Pulse Width	18	8.0		ns	Fig. 2

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, CLOCK PULSE WIDTH, FREQUENCY, SET-UP AND HOLD TIMES DATA TO CLOCK



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME

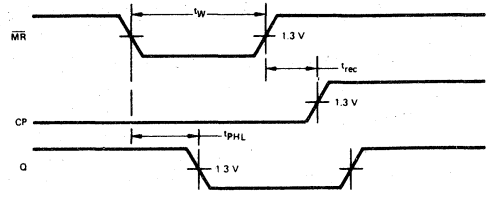


Fig. 2

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) – is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

SN54LS175/SN74LS175

QUAD D FLIP-FLOP

DESCRIPTION – The LSTTL/MSI SN54LS175/SN74LS175 is a high speed Quad D Flip-Flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW to HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

The LS175 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

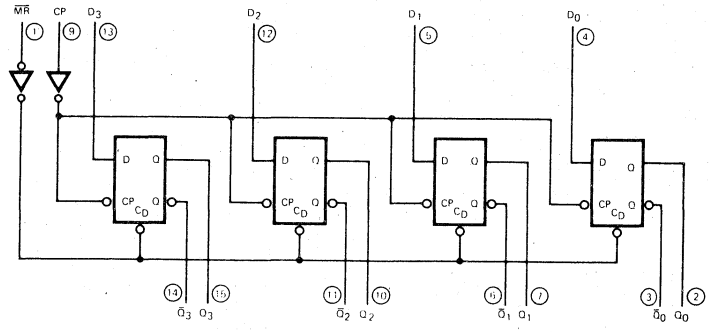
- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED-POSITIVE EDGE-TRIGGERED CLOCK**
- **CLOCK TO OUTPUT DELAYS OF 14 ns**
- **ASYNCHRONOUS COMMON RESET**
- **TRUE AND COMPLEMENT OUTPUT**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$D_0 - D_3$	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	True Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q}_0 - \overline{Q}_3$	Complemented Outputs (Note b)	10 U.L.	5(2.5) U.L.

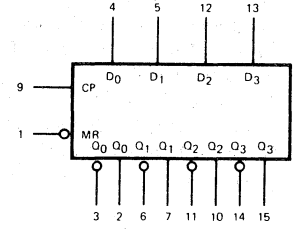
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



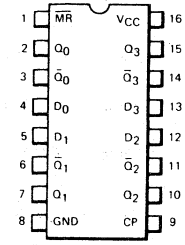
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW to HIGH Clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs.

The LS175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

TRUTH TABLE

Inputs (t = n, $\overline{MR}$ = H)	Outputs (t = n+1) Note 1	
D	Q	$\overline{Q}$
L	L	H
H	H	L

Note 1: t = n + 1 indicates conditions after next clock.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS175X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS175X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{SC}	Output Short Circuit Current (Note 4)		−15		100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			11	18	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

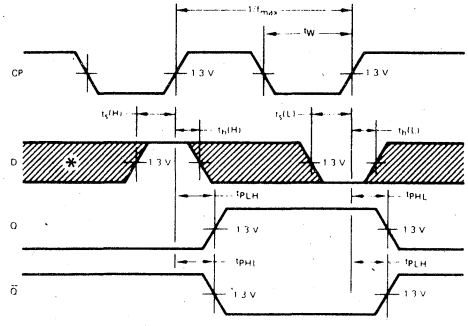
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		12 15	20 22	ns	Fig. 1
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q Output		20	28	ns	Fig. 2
t_{PLH}	Propagation Delay, $\overline{MR}$ to $\overline{Q}$ Output		16	24	ns	Fig. 2
f_{MAX}	Maximum Input Clock Frequency	30	45		MHz	Fig. 1

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_WCP	Minimum Clock Pulse Width	15	10		ns	Fig. 1
t_s	Set-up Time, Data to Clock (HIGH or LOW)	10			ns	Fig. 1
t_h	Hold Time, Data to Clock (HIGH or LOW)	0			ns	Fig. 1
t_{rec}	Recovery Time for $\overline{MR}$	12	8.0		ns	Fig. 2
$t_W\overline{MR}$	Minimum $\overline{MR}$ Pulse Width	18	8.0		ns	Fig. 2

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, CLOCK PULSE WIDTH, FREQUENCY, SET-UP AND HOLD TIMES DATA TO CLOCK



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME

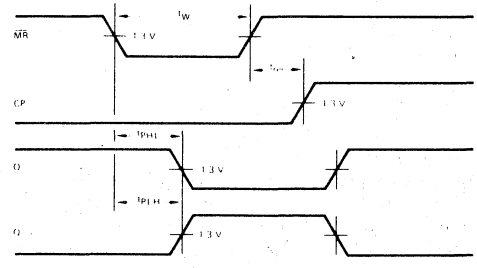


Fig. 2

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) – is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

SN54LS181/SN74LS181

4-BIT ARITHMETIC LOGIC UNIT

DESCRIPTION – The SN54LS181/SN74LS181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic, operations on two variables and a variety of arithmetic operations.

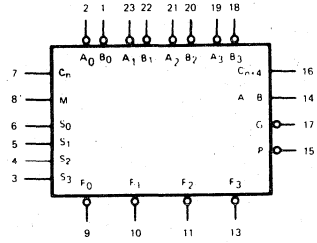
- **PROVIDES 16 ARITHMETIC OPERATIONS**
  ADD, SUBTRACT, COMPARE, DOUBLE, PLUS TWELVE OTHER ARITHMETIC OPERATIONS
- **PROVIDES ALL 16 LOGIC OPERATIONS OF TWO VARIABLES**
  EXCLUSIVE–OR, COMPARE, AND, NAND, OR, NOR, PLUS TEN OTHER LOGIC OPERATIONS
- **FULL LOOKAHEAD FOR HIGH SPEED ARITHMETIC OPERATION ON LONG WORDS**
- **INPUT CLAMP DIODES**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$\overline{A}_0$–$\overline{A}_3$, $\overline{B}_0$–$\overline{B}_3$	Operand (Active LOW) Inputs	1.5 U.L.	0.75 U.L.
S_0–S_3	Function – Select Inputs	2.0 U.L.	1.0 U.L.
M	Mode Control Input	0.5 U.L.	0.25 U.L.
C_n	Carry Input	2.5 U.L.	1.25 U.L.
$\overline{F}_0$–$\overline{F}_3$	Function (Active LOW) Outputs	10 U.L.	5 (2.5) U.L.
A = B	Comparator Output	Open Collector	5 (2.5) U.L.
$\overline{G}$	Carry Generator (Active LOW) Output	10 U.L.	10 U.L.
$\overline{P}$	Carry Propagate (Active LOW) Output	10 U.L.	5 U.L.
C_{n+4}	Carry Output	10 U.L.	5 (2.5) U.L.

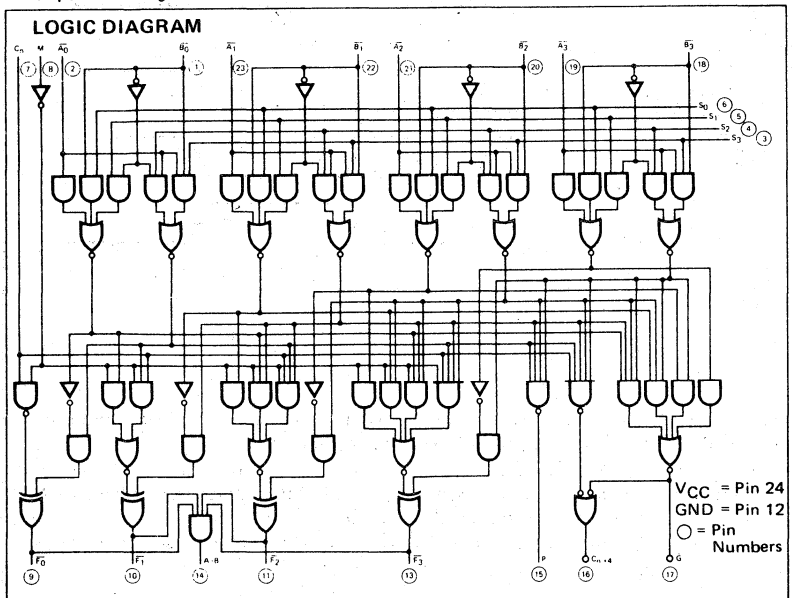
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



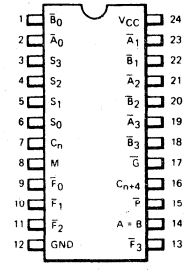
V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12
○ = Pin Numbers

CONNECTION DIAGRAMS
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

FUNCTIONAL DESCRIPTION – The SN54LS181/SN74LS181 is a 4-bit high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select Inputs ($S_0 \ldots S_3$) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

When the Mode Control Input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, the LS181 can be used in a simple ripple carry mode by connecting the Carry Output (C_{n+4}) signal to the Carry Input (C_n) of the next unit. For high speed operation the LS181 is used in conjunction with the 9342 or 93S42 carry lookahead circuit. One carry lookahead package is required for each group of four LS181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the LS181 goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A = B output is open collector and can be wired-AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, the LS181 can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

FUNCTION TABLE

MODE SELECT INPUTS	ACTIVE LOW INPUTS & OUTPUTS		ACTIVE HIGH INPUTS & OUTPUTS	
S_3 S_2 S_1 S_0	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = L)	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = H)
L L L L	$\overline{A}$	A minus 1	$\overline{A}$	A
L L L H	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A + B
L L H L	$\overline{A+B}$	$A\overline{B}$ minus 1	$A\overline{B}$	A + $\overline{B}$
L L H H	Logical 1	minus 1	Logical 0	minus 1
L H L L	$\overline{A+B}$	A plus (A + $\overline{B}$)	$\overline{AB}$	A plus $A\overline{B}$
L H L H	$\overline{B}$	AB plus (A + $\overline{B}$)	$\overline{B}$	(A + B) plus $A\overline{B}$
L H H L	$\overline{A \oplus B}$	A minus B minus 1	A ⊕ B	A minus B minus 1
L H H H	A + $\overline{B}$	A + $\overline{B}$	$A\overline{B}$	AB minus 1
H L L L	$A\overline{B}$	A plus (A + B)	$\overline{A}$ + B	A plus AB
H L L H	A ⊕ B	A plus B	$\overline{A \oplus B}$	A plus B
H L H L	B	$A\overline{B}$ plus (A + B)	B	(A + $\overline{B}$) plus AB
H L H H	A + B	A + B	AB	AB minus 1
H H L L	Logical 0	A plus A*	Logical 1	A plus A*
H H L H	$A\overline{B}$	AB plus A	A + $\overline{B}$	(A + B) plus A
H H H L	AB	$A\overline{B}$ plus A	A + B	(A + $\overline{B}$) plus A
H H H H	A	A	A	A minus 1

L = LOW Voltage Level

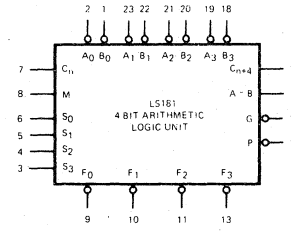
H = HIGH Voltage Level

*Each bit is shifted to the next more significant position

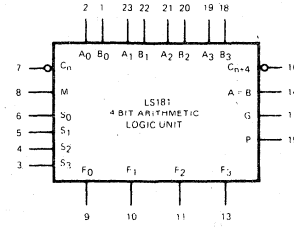
**Arithmetic operations expressed in 2s complement notation

LOGIC SYMBOLS

ACTIVE LOW OPERANDS



ACTIVE HIGH OPERANDS



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
SN54LS181X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS181X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
	Any Output except A=B	74	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{OH}	Output HIGH Current A=B Output Only				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V
V_{OL}	Output LOW Voltage Except $\overline{G}$ and $\overline{P}$	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
	Output LOW Voltage Output $\overline{G}$			0.47	0.7	V	I_{OL} = 16 mA; V_{IL} per Truth Table
	Output LOW Voltage Output $\overline{P}$	54		0.35	0.6	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
		74		0.35	0.7		
I_{IH}	Input HIGH Current Mode Input				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	$\overline{A}$ and $\overline{B}$ Inputs				60		
	S Inputs				80		
	Carry Inputs				100		
	Mode Input				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
	$\overline{A}$ and $\overline{B}$ Inputs				0.3		
	S Inputs				0.4		
	Carry Inputs				0.5		
I_{IL}	Input LOW Current Mode Input				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	$\overline{A}$ and $\overline{B}$ Inputs				−1.2		
	S Inputs				−1.6		
	Carry Inputs				−2.0		
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current Condition A (Note 5)	54		20	32	mA	V_{CC} = MAX
		74		20	34		
	Power Supply Current Condition B (Note 5)	54		21	35		
		74		21	37		

NOTES:
1. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.
5. With outputs open, I_{CC} is measured for the following conditions:
   A. S0 through S3, M, and A inputs are at 4.5 V, all other inputs are grounded.
   B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V, Pin 12 = GND

SYMBOL	PARAMETER	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, (C_n to C_{n+4})		27 20	ns	M = 0 V, (Sum or Diff Mode) See Fig. 4 and Tables I and II
t_{PLH} t_{PHL}	(C_n to $\overline{F}$ Outputs)		26 20	ns	M = 0 V, (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{G}$ Output)		29 23	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{G}$ Output)		32 26	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{P}$ Output)		30 30	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{P}$ Output)		30 33	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to any $\overline{F}$ Output)		32 20	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to any $\overline{F}$ Output)		32 23	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{F}$ Outputs)		33 29	ns	M = 4.5 V (Logic Mode) See Fig. 4 and Table III
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to C_{n+4} Output)		38 38	ns	M = 0 V, S_0 = S_3 = 4.5 V, S_1 = S_2 = 0 V (Sum Mode) See Fig. 6 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to C_{n+4} Output)		41 41	ns	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode)
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to A = B Output)		50 62	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V, R_L = 2 kΩ (Diff Mode) See Fig. 5 and Table II

AC WAVEFORMS

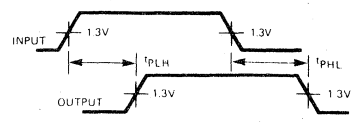


Fig. 4

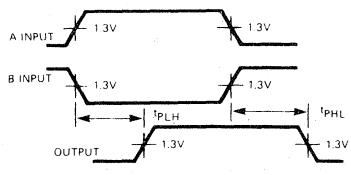


Fig. 5

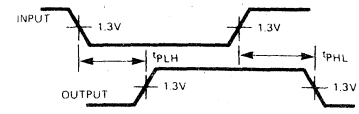


Fig. 6

SUM MODE TEST TABLE I

FUNCTION INPUTS: $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = M = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_i + 1$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_i + 1$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or $C_n + 4$

DIFF MODE TEST TABLE II

FUNCTION INPUTS: $S_1 = S_2 = 4.5$ V, $S_0 = S_3 = M = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_i + 1$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_i + 1$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	$C_n + 4$

LOGIC MODE TEST TABLE III

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$	$S_1 = S_2 = M = 4.5$ V $S_0 = S_3 = 0$ V
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$	$S_1 = S_2 = M = 4.5$ V $S_0 = S_3 = 0$ V

Advance Information

SN54LS182/SN74LS182

CARRY LOOKAHEAD GENERATOR

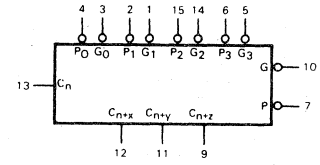
DESCRIPTION — The 54LS/74LS182 is a high-speed Carry Lookahead Generator. It is generally used with the 54LS/74LS181 4-Bit Arithmetic Logic Unit to provide high speed lookahead over word lengths of more than four bits. The carry lookahead generator is fully compatible with all members of the Motorola TTL Family.

- **PROVIDES CARRY LOOKAHEAD ACROSS A GROUP OF FOUR ALUs**
- **MULTI-LEVEL LOOKAHEAD FOR HIGH-SPEED ARITHMETIC OPERATION OVER LONG WORD LENGTHS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATIBLE**

PIN NAMES		LOADING (Note a) HIGH	LOW
C_n	Carry Input	0.5 U.L.	0.25 U.L.
$\overline{G}_0$, $\overline{G}_2$	Carry Generate (Active LOW) Inputs	3.5 U.L.	1.75 U.L.
$\overline{G}_1$	Carry Generate (Active LOW) Input	4.0 U.L.	2.0 U.L.
$\overline{G}_3$	Carry Generate (Active LOW) Input	2.0 U.L.	1.0 U.L.
$\overline{P}_0$, $\overline{P}_1$	Carry Propagate (Active LOW) Inputs	2.0 U.L.	1.0 U.L.
$\overline{P}_2$	Carry Propagate (Active LOW) Input	1.5 U.L.	0.75 U.L.
$\overline{P}_3$	Carry Propagate (Active LOW) Input	1.0 U.L.	0.5 U.L.
C_{n+x}, C_{n+y}, C_{n+z}	Carry Outputs (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{G}$	Carry Generate (Active LOW) Output (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{P}$	Carry Propagate (Active LOW) Output (Note b)	10 U.L.	5 (2.5) U.L.

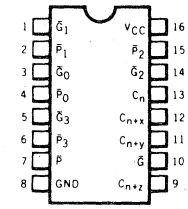
NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH 1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



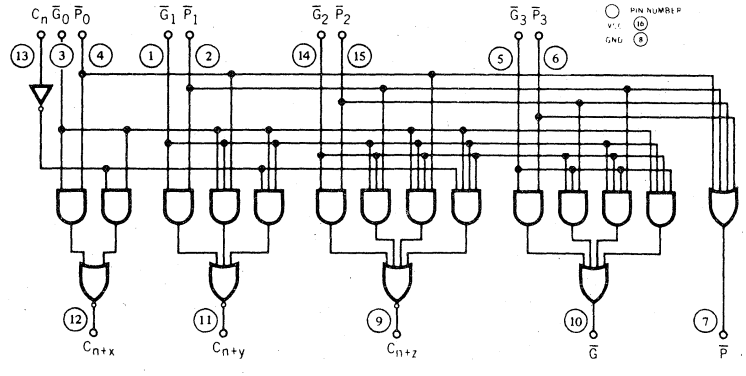
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



This is advance information and specifications are subject to change without notice.

FUNCTIONAL DESCRIPTION—The 54LS/74LS182, carry lookahead generator accepts up to four pairs of active LOW Carry Propagate ($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$) and Carry Generate ($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$, $\overline{G}_3$) signals and an active HIGH Carry Input (C_n) and provides anticipated active HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The 54LS/74LS182 also has active LOW Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs which may be used for further levels of lookahead.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 = P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_2G_0 + P_2P_1P_0C_n$$
$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$
$$\overline{P} = \overline{P_3P_2P_1P_0}$$

Also, the 54LS/74LS182 can also be used with binary ALUs in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry lookahead generator are identical in both cases.

TRUTH TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS182X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS182X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN	I_{IN} = −18 mA
V_{OH}	Output HIGH voltage	54	2.5			V	I_{OH} = -400 μA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7					
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5		I_{OL} = 8 mA	
I_{IH}	C_n				20 μA		V_{IN} = 2.7 V V_{CC} = MAX	
	$\overline{G}_0$, $\overline{G}_2$				140 μA			
	$\overline{G}_3$, $\overline{P}_0$, $\overline{P}_1$				80 μA			
	$\overline{P}_2$				60 μA			
	$\overline{P}_3$				40 μA			
	$\overline{G}_1$				160 μA			
	C_n				.100 μA		V_{IN} = 10 V V_{CC} = MAX	
	$\overline{G}_0$, $\overline{G}_2$				.700 μA			
	$\overline{G}_3$, $\overline{P}_0$, $\overline{P}_1$				.400 μA			
	$\overline{P}_2$				.300 μA			
	$\overline{P}_3$				.200 μA			
	$\overline{G}_1$				.800 μA			
I_{IL}	C_n				−0.4 mA		V_{IN} = 0.4 V V_{CC} = MAX	
	$\overline{G}_0$, $\overline{G}_2$				−2.8 mA			
	$\overline{G}_3$, $\overline{P}_0$, $\overline{P}_1$				−1.6 mA			
	$\overline{P}_2$				−1.2 mA			
	$\overline{P}_3$				−0.8 mA			
	$\overline{G}_1$				−3.2 mA			
I_{OS}	Output Short-Circuit Current (Note 4)		−20		−100	mA	V_{CC} = MAX V_{OUT} = 0 V	
I_{CCH} I_{CCL}	Power Supply Current				12 16	mA	V_{CC} = MAX	

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operations under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and max loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V, C_L = 15 pF, RL = 2 kΩ

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	(C_n to C_{n+x}, C_{n+y}, C_{n+z})		13 16		ns	$\overline{P}_0 = \overline{P}_1 = \overline{P}_2$ = Gnd, $\overline{G}_0 = \overline{G}_1 = \overline{G}_2$ = 4.5 V Fig. 1
t_{PLH} t_{PHL}	($\overline{P}_0$, $\overline{P}_1$, or $\overline{P}_2$ to C_{n+x}, C_{n+y}, or C_{n+z})		9 12.5		ns	$\overline{P}_x$ = Gnd (If not under test), $C_n = \overline{G}_0 = \overline{G}_1 = \overline{G}_2$ = 4.5 V, Fig. 2
t_{PLH} t_{PHL}	($\overline{G}_0$, $\overline{G}_1$ or $\overline{G}_2$ to C_{n+x}, C_{n+y}, or C_{n+z})		9 12.5		ns	$\overline{G}_x$ = 4.5 V (If not under test), $C_n = \overline{P}_0 = \overline{P}_1 = \overline{P}_2$ = Gnd, Fig. 2
t_{PLH} t_{PHL}	($\overline{P}_1$, $\overline{P}_2$ or $\overline{P}_3$ to $\overline{G}$ or $\overline{P}$)		9 12.5		ns	$\overline{P}_x$ = Gnd (If not under test), $\overline{G}_0 = \overline{G}_1 = \overline{G}_2 = \overline{G}_3 = C_n$ = 4.5 V, Fig. 1
t_{PLH} t_{PHL}	($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$ or $\overline{G}_3$ to $\overline{G}$)		26 8		ns	$\overline{G}_x$ = 4.5 V (If not under test), $\overline{P}_1 = \overline{P}_2 = \overline{P}_3$ = Gnd, Fig. 1
t_{PLH} t_{PHL}	($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$ or $\overline{P}_3$ to $\overline{P}$)		20 8.5		ns	$\overline{P}_x$ = Gnd (If not under test), Fig. 1

AC WAVEFORMS

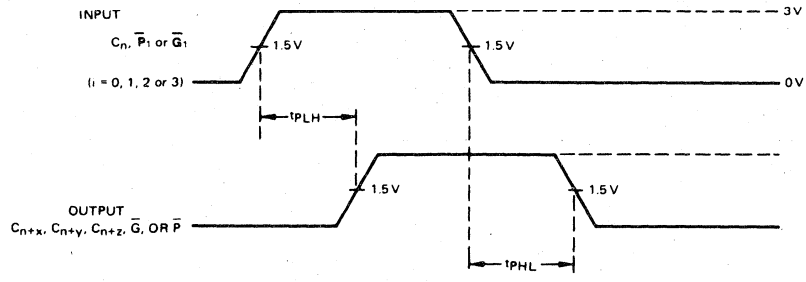


Fig.1

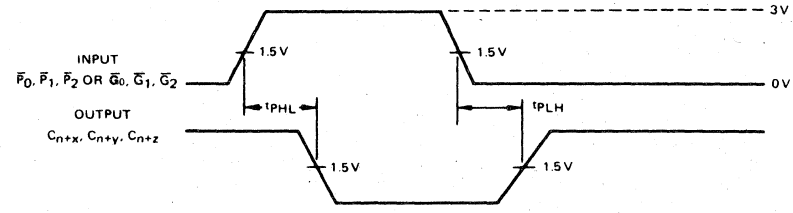


Fig. 2

Advance Information

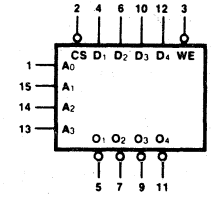
SN54LS189/SN74LS189

64-BIT RANDOM ACCESS MEMORY WITH 3-STATE OUTPUTS

DESCRIPTION – The 54LS/74LS189 is a high-speed, low-power 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-state and are in the high-impedance state whenever the Chip Select (CS) input is HIGH. The outputs are active only in the Read mode and the output data is the complement of the stored data.

- **3-STATE OUTPUTS FOR DATA BUS APPLICATIONS**
- **BUFFERED INPUTS MINIMIZE LOADING**
- **ADDRESS DECODING ON-CHIP**
- **DIODE CLAMPED INPUTS MINIMIZE RINGING**
- **LOW POWER SCHOTTKY DESIGN MINIMIZES POWER CONSUMPTION**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

AN	Address Input
$\overline{CS}$	Chip Select (active LOW) Input
D_n	Data Input
$\overline{O_n}$	Data (inverted) Output
$\overline{WE}$	Write Enable (active LOW) Input

FUNCTION TABLE

INPUTS $\overline{CS}$	INPUTS $\overline{WE}$	OPERATION	CONDITION OF OUTPUTS
L	H	Write	HIGH Impedance
L	H	Read	Complement of Stored Data
H	X	Inhibit	HIGH Impedance

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

This is advance information and specifications are subject to change without notice.

SN54LS190/ SN74LS190
PRESETTABLE BCD/DECADE UP/DOWN COUNTERS

SN54LS191/ SN74LS191
PRESETTABLE 4-BIT BINARY UP/DOWN COUNTERS

DESCRIPTION – The SN54LS190/SN74LS190 is a synchronous UP/DOWN BCD Decade (8421) Counter and the SN54LS191/SN74LS191 is a synchronous UP/DOWN Modulo-16 Binary Counter. State changes of the counters are synchronous with the LOW-to-HIGH transition of the Clock Pulse input.

An asynchronous Parallel Load ($\overline{PL}$) input overrides counting and loads the data present on the P_n inputs into the flip-flops, which makes it possible to use the circuits as programmable counters. A Count Enable ($\overline{CE}$) input serves as the carry/borrow input in multi-stage counters. An Up/Down Count Control ($\overline{U}/D$) input determines whether a circuit counts up or down. A Terminal Count (TC) output and a Ripple Clock ($\overline{RC}$) output provide overflow/underflow indication and make possible a variety of methods for generating carry/borrow signals in multi-stage counter applications.

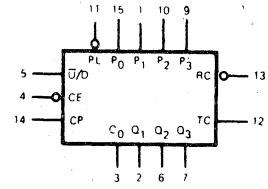
- **LOW POWER . . . 90 mW TYPICAL DISSIPATION**
- **HIGH SPEED . . . 35 MHz TYPICAL COUNT FREQUENCY**
- **SYNCHRONOUS COUNTING**
- **ASYNCHRONOUS PARALLEL LOAD**
- **INDIVIDUAL PRESET INPUTS**
- **COUNT ENABLE AND UP/DOWN CONTROL INPUTS**
- **CASCADABLE**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{CE}$	Count Enable (Active LOW) Input	1.5 U.L.	0.7 U.L.
CP	Clock Pulse (Active HIGH going edge) Input	0.5 U.L.	0.25 U.L.
$\overline{U}/D$	Up/Down Count Control Input	0.5 U.L.	0.25 U.L.
$\overline{PL}$	Parallel Load Control (Active LOW) Input	0.5 U.L.	0.25 U.L.
P_n	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_n	Flip-Flop Outputs (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{RC}$	Ripple Clock Output (Note b)	10 U.L.	5 (2.5) U.L.
TC	Terminal Count Output (Note b)	10 U.L.	5 (2.5) U.L.

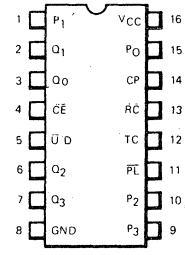
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



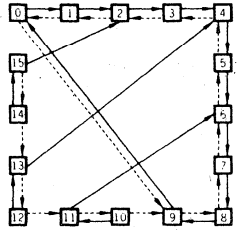
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

STATE DIAGRAMS



190

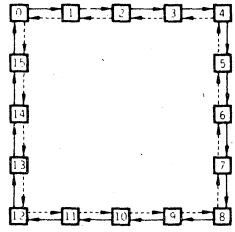
LS190

UP: $TC = Q_0 \cdot Q_3 \cdot (\overline{U}/D)$
DOWN: $TC = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot (\overline{U}/D)$

LS191

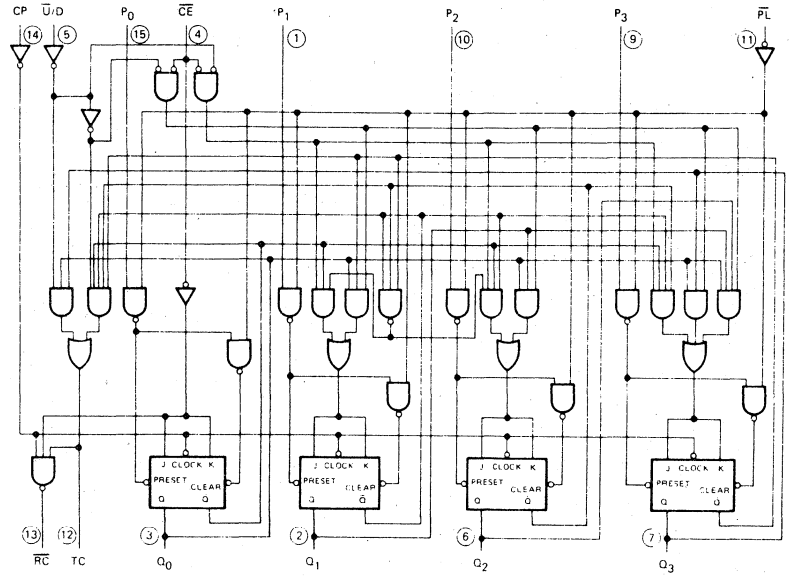
UP: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (\overline{U}/D)$
DOWN: $TC = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot (\overline{U}/D)$

Count Up ——
Count Down ------

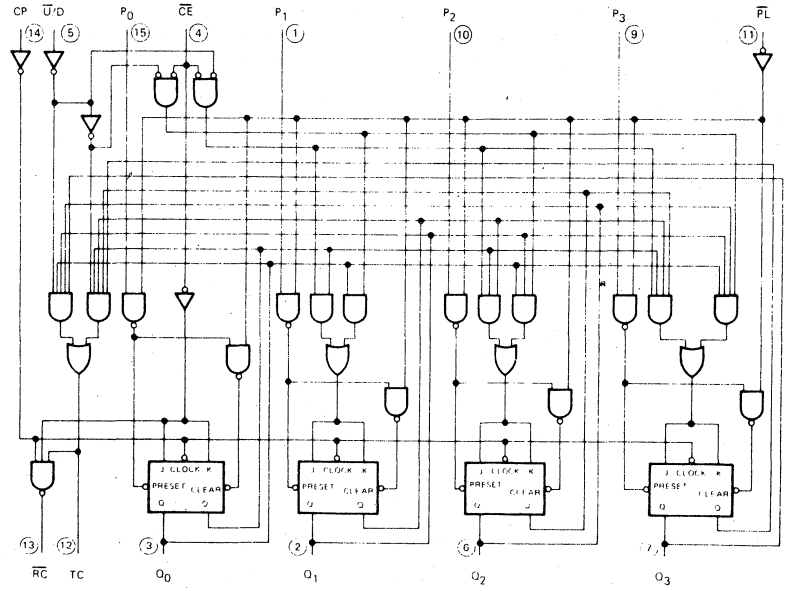


191

LOGIC DIAGRAMS



DECADE COUNTER
LS190



BINARY COUNTER
LS191

V_{CC} = Pin 16
GND = Pin 8
◯ = Pin Numbers

FUNCTIONAL DESCRIPTION – The LS190 is a synchronous Up/Down BCD Decade Counter and the LS191 is a synchronous Up/Down 4-Bit Binary Counter. The operating modes of the LS190 decade counter and the LS191 binary counter are identical, with the only difference being the count sequences as noted in the state diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Data inputs (P_0–P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}$/D input signal, as indicated in the Mode Select Table. When counting is to be enabled, the $\overline{CE}$ signal can be made LOW when the clock is in either state. However, when counting is to be inhibited, the LOW-to-HIGH $\overline{CE}$ transition must occur only while the clock is HIGH. Similarly, the $\overline{U}$/D signal should only be changed when either $\overline{CE}$ or the clock is HIGH.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches maximum (9 for the LS190, 15 for the LS191) in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, the $\overline{RC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multi-stage counters, as indicated in Figures a and b. In Figure a, each $\overline{RC}$ output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse, as indicated in the $\overline{RC}$ Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure b. All clock inputs are driven in parallel and the $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{RC}$ output of any package goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure c avoids ripple delays and their associated restrictions. The $\overline{CE}$ input signal for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures a and b doesn't apply, because the TC output of a given stage is not affected by its own $\overline{CE}$.

MODE SELECT TABLE

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	⎍	Count Up
H	L	H	⎍	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

RC TRUTH TABLE

INPUTS			$\overline{RC}$
$\overline{CE}$	TC*	CP	OUTPUT
L	H	⎍⎍	⎍⎍
H	X	X	H
X	L	X	H

*TC is generated internally

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
⎍ = LOW-to-HIGH Clock Transition
⎍⎍ = LOW Pulse

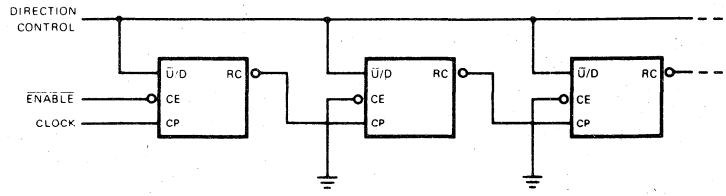


Fig. a) n-stage counter using ripple clock.

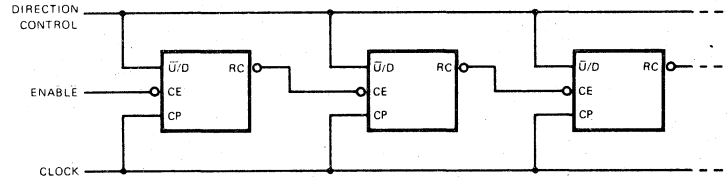


Fig. b) Synchronous n-stage counter using ripple carry/borrow.

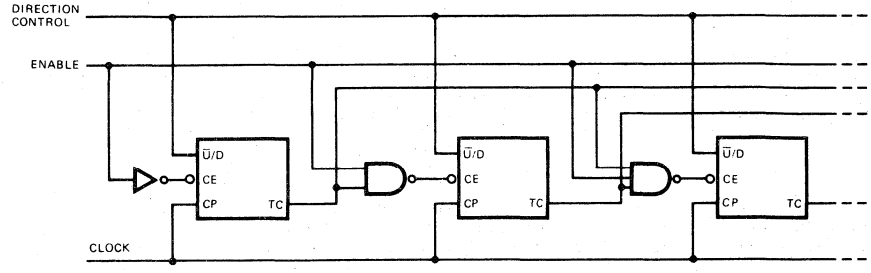


Fig. c) Synchronous n-stage counter with parallel gated carry/borrow.

• **ABSOLUTE MAXIMUM RATINGS** (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to+5.5V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
SN54LS190X SN54LS191X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS190X SN74LS191X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current P_n, $\overline{PL}$, CP, $\overline{U}/D$				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	$\overline{CE}$				60		
	P_n, $\overline{PL}$, CP, $\overline{U}/D$				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
	$\overline{CE}$				0.3		
I_{IL}	Input LOW Current P_n, $\overline{PL}$, CP, $\overline{U}/D$				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	$\overline{CE}$				−1.2		
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			20	35	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.
5. The Set-Up Time "t_s(H)" and Hold Time "t_h(L)" between the Count Enable ($\overline{CE}$) and the Clock (CP) indicate that the LOW-to-HIGH transition of the $\overline{CE}$ must occur only while the Clock is HIGH for conventional operation.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Max. Input Count Frequency	25	35		MHz	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, CP Input to Q Outputs			24 36	ns	Fig. 1	
t_{PLH} t_{PHL}	CP Input to $\overline{RC}$ Output			20 24	ns	Fig. 2	
t_{PLH} t_{PHL}	CP Input to TC Output			42 52	ns	Fig. 1	
t_{PLH}* t_{PHL}*	$\overline{U}$/D Input to $\overline{RC}$ Output			45 45	ns	Fig. 7	
t_{PLH} t_{PHL}	$\overline{U}$/D Input to TC Output			33 33	ns		
t_{PLH} t_{PHL}	$P_0 - P_3$ Inputs to $Q_0 - Q_3$ Outputs			22 50	ns	Fig. 3	
t_{PLH} t_{PHL}	$\overline{PL}$ Input to Any Output			33 50	ns	Fig. 4	
t_{PLH}* t_{PHL}	$\overline{CE}$ Input to $\overline{RC}$ Output			33 33	ns	Fig. 2	

*It is possible to get these timing relationships, but they should not occur during normal operation since the CP would be HIGH.

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_W	CP Pulse Width	20			ns	Fig. 1	V_{CC} = 5.0 V
t_W	$\overline{PL}$ Pulse Width	35			ns	Fig. 4	
t_sL	Set-Up Time LOW, Data to $\overline{PL}$	20			ns	Fig. 6	
t_hL	Hold Time LOW, Data to $\overline{PL}$	0			ns		
t_sH	Set-Up Time HIGH, Data to $\overline{PL}$	20			ns		
t_hH	Hold Time HIGH, Data to $\overline{PL}$	0			ns		
t_{rec}	Recovery Time, $\overline{PL}$ to CP	20			ns	Fig. 5	
t_sL	Set-Up Time LOW, $\overline{CE}$ to Clock	20			ns	Fig. 8	
t_hL	Hold Time LOW, $\overline{CE}$ to Clock	0			ns		

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

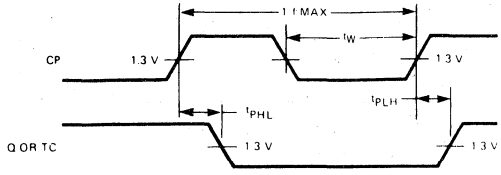


Fig. 1

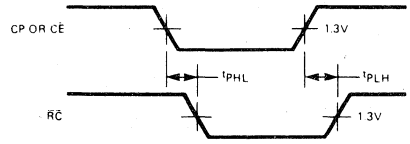
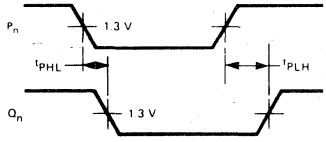


Fig. 2



NOTE: $\overline{PL}$ = LOW

Fig. 3

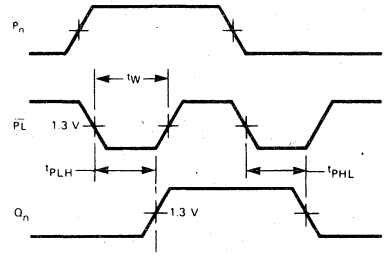


Fig. 4

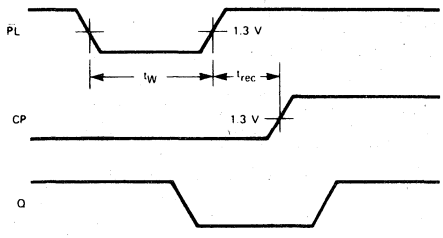
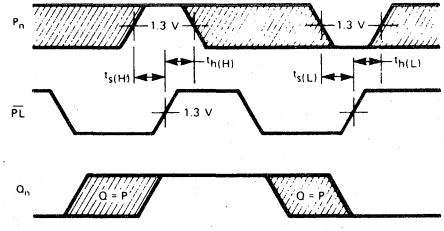


Fig. 5



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 6

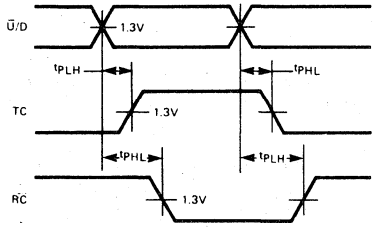


Fig. 7

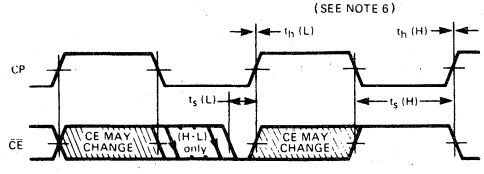


Fig. 8

SN54LS192/ SN74LS192

PRESETTABLE BCD/DECADE UP/DOWN COUNTER

SN54LS193/ SN74LS193

PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

DESCRIPTION — The SN54LS192/SN74LS192 is an UP/DOWN BCD Decade (8421) Counter and the SN54LS193/SN74LS193 is an UP/DOWN MODULO-16 Binary Counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

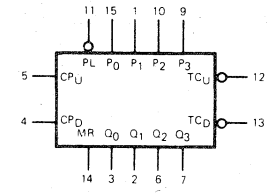
- **LOW POWER . . . . 95 mW TYPICAL DISSIPATION**
- **HIGH SPEED . . . 40 MHz TYPICAL COUNT FREQUENCY**
- **SYNCHRONOUS COUNTING**
- **ASYNCHRONOUS MASTER RESET AND PARALLEL LOAD**
- **INDIVIDUAL PRESET INPUTS**
- **CASCADING CIRCUITRY INTERNALLY PROVIDED**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
CP_U	Count Up Clock Pulse Input	0.5 U.L.	0.25 U.L.
CP_D	Count Down Clock Pulse Input	0.5 U.L.	0.25 U.L.
MR	Asynchronous Master Reset (Clear) Input	0.5 U.L.	0.25 U.L.
$\overline{PL}$	Asynchronous Parallel Load (Active LOW) Input	0.5 U.L.	0.25 U.L.
P_n	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_n	Flip-Flop Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Note b)	10 U.L.	5(2.5) U.L.
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Note b)	10 U.L.	5(2.5) U.L.

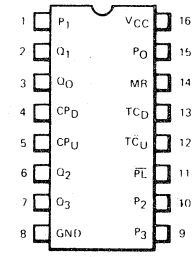
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for MILITARY (54) and 5 U.L. for COMMERCIAL (74) Temperature Ranges.

LOGIC SYMBOL



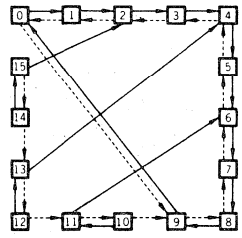
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

STATE DIAGRAMS



LS192

LS192 LOGIC EQUATIONS FOR TERMINAL COUNT

$\overline{TC}_U = Q_0 \cdot Q_3 \cdot \overline{CP_U}$

$\overline{TC}_D = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{CP_D}$

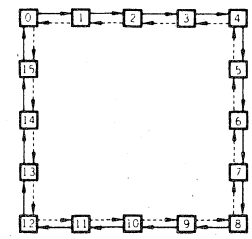
LS193 LOGIC EQUATIONS FOR TERMINAL COUNT

$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP_U}$

$\overline{TC}_D = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{CP_D}$

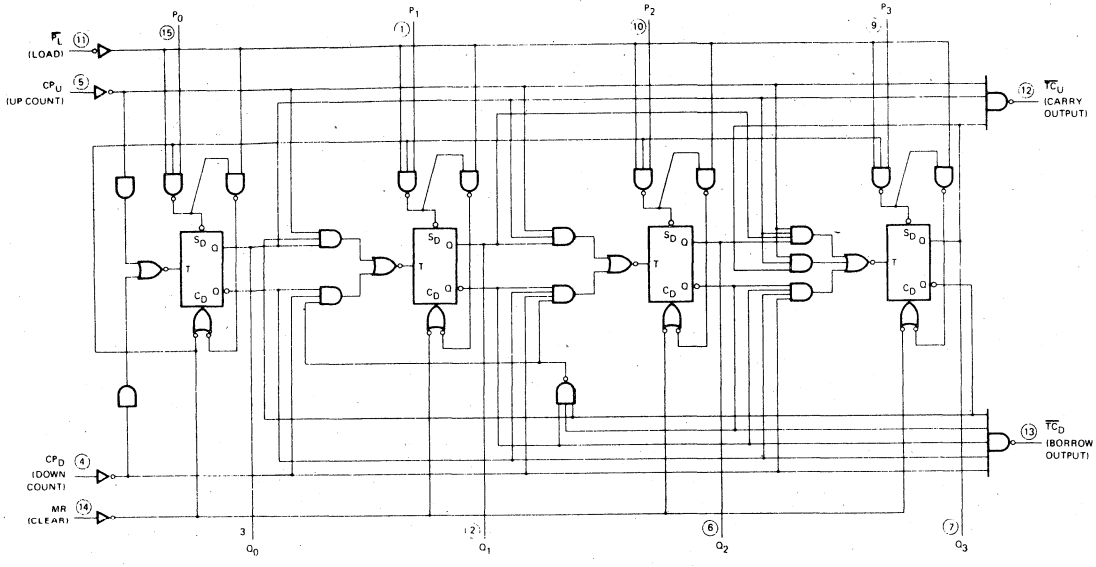
COUNT UP ——

COUNT DOWN ------

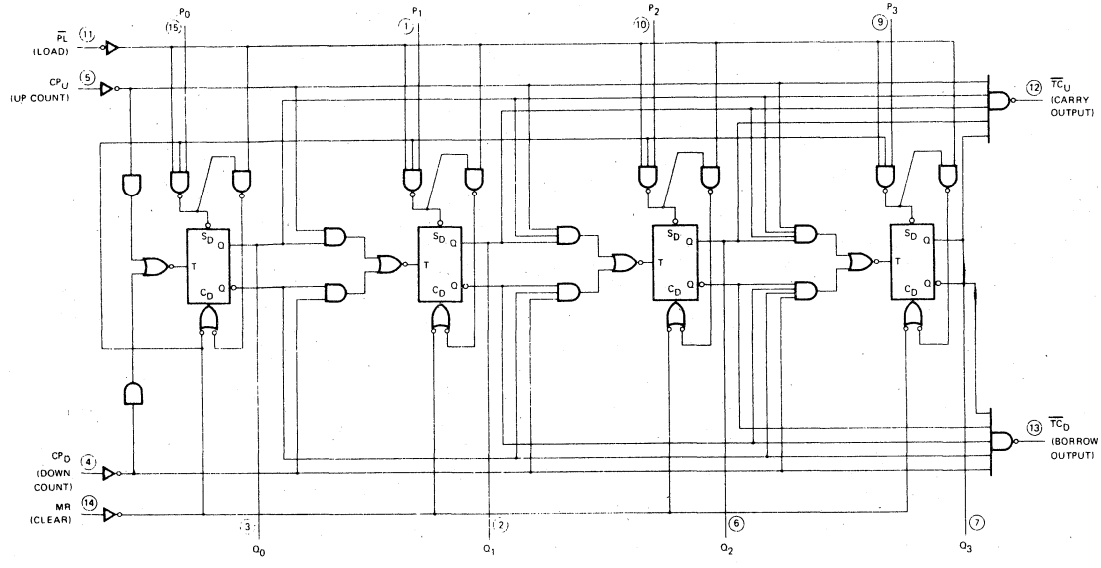


LS193

LOGIC DIAGRAMS



LS192



LS193

V_{CC} = Pin 16
GND = Pin 8
◯ = Pin Number

FUNCTIONAL DESCRIPTION – The LS192 and LS193 are Asynchronously Presettable Decade and 4-Bit Binary Synchronous UP/DOWN (Reversable) Counters. The operating modes of the LS192 decade counter and the LS193 binary counter are identical, with the only difference being the count sequences as noted in the State Diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the LS192, 15 for the LS193), the next HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the TC outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data inputs (P_0, P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

MODE SELECT TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asnyn.)
L	H	H	H	No Change
L	H	⎍	H	Count Up
L	H	H	⎍	Count Down

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
⎍ = LOW-to-HIGH Clock Transition

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5V to +7.0 V
* Input Voltage (dc)	–0.5 V to 15 V
* Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

* Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS192X SN54LS193X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS192X SN74LS193X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA; V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			19	34	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, now shown in the table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS	
		LS192			LS193					
		MIN	TYP	MAX	MIN	TYP	MAX			
f_{MAX}	Max Input Count Frequency	30	40		30	40		MHz	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	CP_U Input to $\overline{TC}_U$ Output		10 14	16 21		10 14	16 21	ns	Fig. 2	
t_{PLH} t_{PHL}	CP_D Input to $\overline{TC}_D$ Output		10 15	16 22		10 15	16 22	ns		
t_{PLH} t_{PHL}	CP_U or CP_D to Q_n Outputs		22 18	31 28		22 18	31 28	ns		
t_{PLH} t_{PHL}	$P_0 - P_3$ Inputs $Q_0 - Q_3$ Outputs							ns	Fig. 3	
t_{PLH} t_{PHL}	$\overline{PL}$ Input to Any Output		23 17	32 25		23 17	32 25	ns	Fig. 4	
t_{PHL}	MR Input to Any Output		17	25		17	25	ns	Fig. 7	

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS	
		LS192			LS193					
		MIN	TYP	MAX	MIN	TYP	MAX			
t_W	CP_U Pulse Width	17			17			ns	Fig. 1	V_{CC} = 5.0 V
t_W	CP_D Pulse Width	17			17			ns		
t_W	$\overline{PL}$ Pulse Width	15			15			ns	Fig. 4	
t_W	MR Pulse Width	15			15			ns	Fig. 7	
t_sL	Set-up Time LOW, Data to $\overline{PL}$	10			10			ns	Fig. 6	
t_hL	Hold Time LOW, Data to $\overline{PL}$	0			0			ns		
t_sH	Set-up Time HIGH, Data to $\overline{PL}$	10			10			ns		
t_hH	Hold Time HIGH, Data to $\overline{PL}$	0			0			ns		
t_{rec}	Recovery Time, $\overline{PL}$ to CP	3			3			ns	Fig. 5	
t_{rec}	Recovery Time, MR to CP	3			3			ns		

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the $\overline{PL}$ transistion from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the $\overline{PL}$ transistion from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the $\overline{PL}$ transistion from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

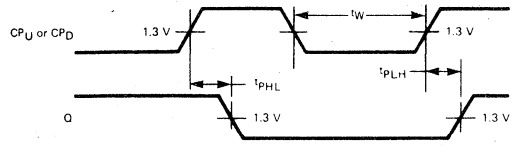


Fig. 1

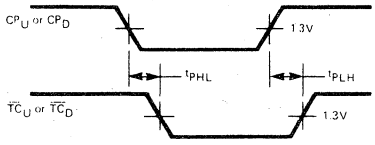
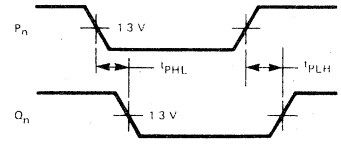


Fig. 2



NOTE: $\overline{PL}$ = LOW

Fig. 3

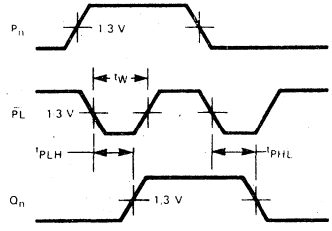


Fig. 4

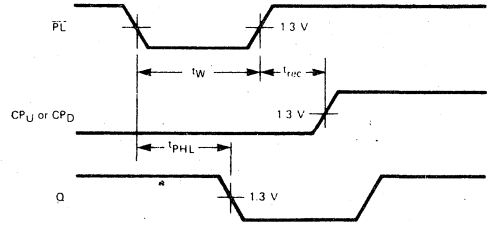
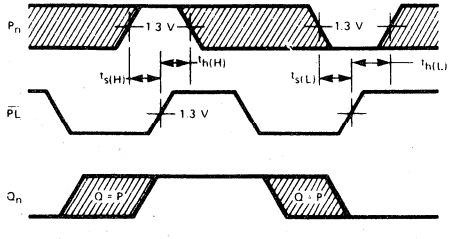


Fig. 5



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 6

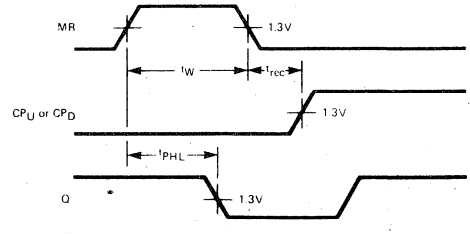


Fig. 7

SN54LS194A/SN74LS194A

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

DESCRIPTION – The SN54LS194A/SN74LS194A is a High Speed 4-Bit Bidirectional Universal Shift Register. As a high speed multifunctional sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The LS194A is similar in operation to the LS195A Universal Shift Register, with added features of shift left without external connections and hold (do nothing) modes of operation. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL families.

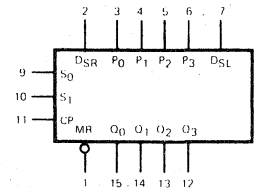
- TYPICAL SHIFT FREQUENCY OF 40 MHz
- ASYNCHRONOUS MASTER RESET
- HOLD (DO NOTHING) MODE
- FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

		LOADING (Note a) HIGH	LOW
S_0, S_1	Mode Control Inputs	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
D_{SR}	Serial (Shift Right) Data Input	0.5 U.L.	0.25 U.L.
D_{SL}	Serial (Shift Left) Data Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	Parallel Outputs (Note b)	10 U.L.	5(2.5) U.L.

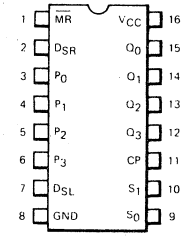
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL

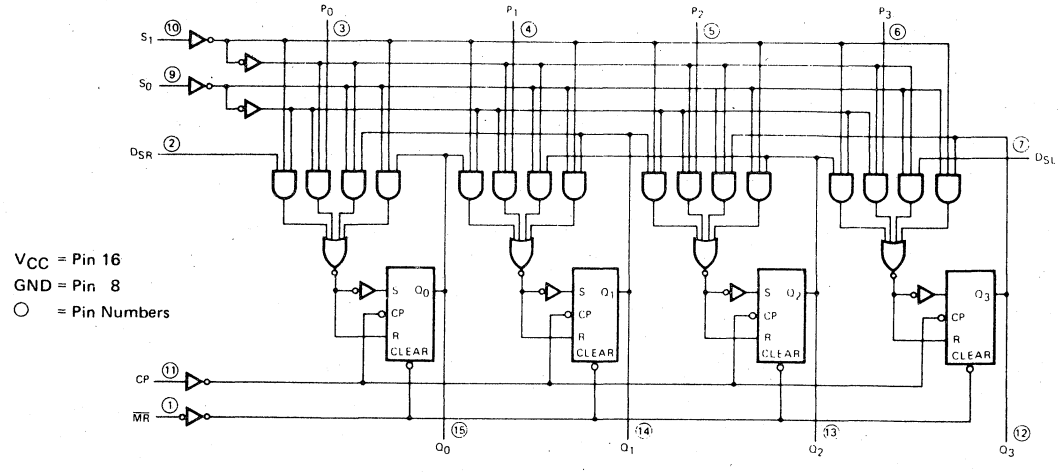


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The Logic Diagram and Truth Table indicate the functional characteristics of the LS194A 4-Bit Bidirectional Shift Register. The LS194A is similar in operation to the Motorola LS195A Universal Shift Register when used in serial or parallel data register transfers. Some of the common features of the two devices are described below:

1. All data and mode control inputs are edge-triggered, responding only to the LOW to HIGH transition of the Clock (CP). The only timing restriction, therefore, is that the mode control and selected data inputs must be stable one set-up time prior to the positive transition of the clock pulse.

2. The register is fully synchronous, with all operations taking place in less than 15 ns (typical) making the device especially useful for implementing very high speed CPUs, or the memory buffer registers.

3. The four parallel data inputs (P_0, P_1, P_2, P_3) are D-type inputs. When both S_0 and S_1 are HIGH, the data appearing on P_0, P_1, P_2, and P_3 inputs is transferred to the Q_0, Q_1, Q_2, and Q_3 outputs respectively following the next LOW to HIGH transition of the clock.

4. The asynchronous Master Reset ($\overline{MR}$), when LOW, overrides all other input conditions and forces the Q outputs LOW.

Special logic features of the LS194A design which increase the range of application are described below:

1. Two mode control inputs (S_0, S_1) determine the synchronous operation of the device. As shown in the Mode Selection Table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.) or right to left (shift left, $Q_3 \rightarrow Q_2$, etc.), or parallel data can be entered loading all four bits of the register simultaneously. When both S_0 and S_1 are LOW, the existing data is retained in a "do nothing" mode without restricting the HIGH to LOW clock transition.

2. D-type serial data inputs (D_{SR}, D_{SL}) are provided on both the first and last stages to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS						OUTPUTS			
	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	P_n	Q_0	Q_1	Q_2	Q_3
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	H	h	l	X	l	X	q_1	q_2	q_3	L
	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift Right	H	l	h	l	X	X	L	q_0	q_1	q_2
	H	l	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	H	h	h	X	X	p_n	p_0	p_1	p_2	p_3

L = LOW Voltage Level
H= HIGH Voltage Level
X = Don't Care
l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition
h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS194AX	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS194AX	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type, W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			15	23	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Shift Frequency	30	40		MHz	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} / t_{PHL}	Propagation Delay, Clock to Output			21 / 24	ns	Fig. 1	
t_{PHL}	Propagation Delay, $\overline{MR}$ to Output			26	ns	Fig. 2	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_W(CP)	Clock Pulse Width	18	12		ns	Fig. 1	V_{CC} = 5.0 V
t_s(Data)	Set-up Time, Data to Clock	16			ns	Fig. 3	
t_h(Data)	Hold Time, Data to Clock	0			ns		
t_s(S)	Set-up Time, Mode Control to Clock	20			ns	Fig. 4	
t_h(S)	Hold Time, Mode Control to Clock	0			ns		
t_W(MR)	Master Reset Pulse Width	12			ns	Fig. 2	
t_{rec}(MR)	Recovery Time Master Reset to Clock	18	12		ns		

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

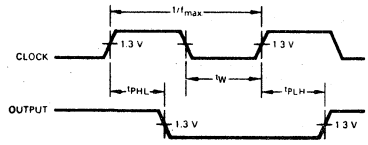
HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) – is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

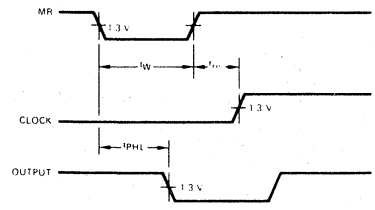
CLOCK TO OUTPUT DELAYS CLOCK PULSE WIDTH AND f_{max}



OTHER CONDITIONS: S_1 = L, $\overline{MR}$ = H, S_0 = H

Fig. 1

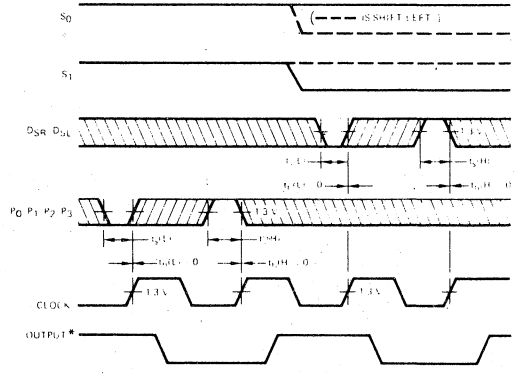
MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



OTHER CONDITIONS: S_0, S_1 = H
$P_0 = P_1 = P_2 = P_3$ = H

Fig. 2

SET-UP (t_s) AND HOLD (t_h) TIME FOR SERIAL DATA (D_{SR}, D_{SL}) AND PARALLEL DATA (P_0, P_1, P_2, P_3)

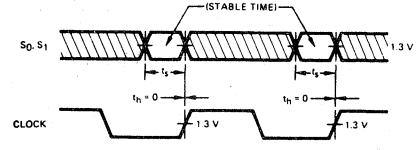


OTHER CONDITIONS: $\overline{MR}$ = H

*D_{SR} set-up time affects Q_0 only
D_{SL} set-up time affects Q_3 only

Fig. 3

SET-UP (t_s) AND HOLD (t_h) TIME FOR S INPUT



OTHER CONDITIONS: $\overline{MR}$ = H

Fig. 4

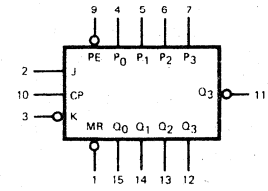
SN54LS195A/SN74LS195A

UNIVERSAL 4-BIT SHIFT REGISTER

DESCRIPTION — The SN54LS195A/SN74LS195A is a high speed 4-Bit Shift Register offering typical shift frequencies of 50 MHz. It is useful for a wide variety of register and counting applications. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL products.

- TYPICAL SHIFT RIGHT FREQUENCY OF 50 MHz
- ASYNCHRONOUS MASTER RESET
- J, $\overline{K}$ INPUTS TO FIRST STAGE
- FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

LOGIC SYMBOL



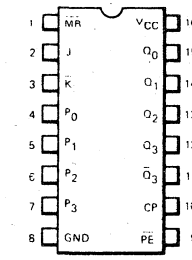
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{PE}$	Parallel Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
J	First Stage J (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{K}$	First Stage K (Active LOW) Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	Parallel Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q}_3$	Complementary Last Stage Output (Note b)	10 U.L.	5(2.5) U.L.

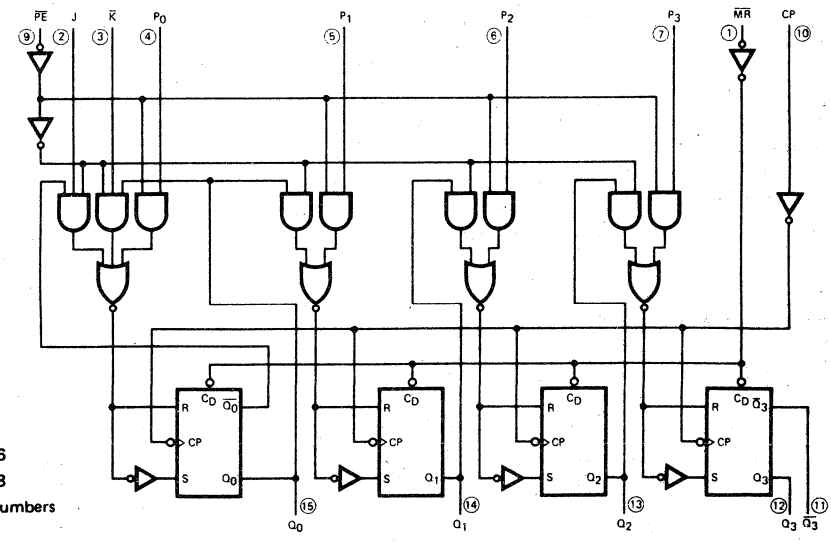
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The Logic Diagram and Truth Table indicate the functional characteristics of the LS195A 4-Bit Shift Register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The LS195A has two primary modes of operation, shift right ($Q_0 \rightarrow Q_1$) and parallel load which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. When the PE input is HIGH, serial data enters the first flip-flop Q_0 via the J and $\overline{K}$ inputs and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW to HIGH clock transition. The $\overline{JK}$ inputs provide the flexibility of the JK type input for special applications, and the simple D type input for general applications by tying the two pins together. When the $\overline{PE}$ input is LOW, the LS195A appears as four common clocked D flip-flops. The data on the parallel inputs P_0, P_1, P_2, P_3 is transferred to the respective Q_0, Q_1, Q_2, Q_3 outputs following the LOW to HIGH clock transition. Shift left operations ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n outputs to the P_{n-1} inputs and holding the $\overline{PE}$ input LOW.

All serial and parallel data transfers are synchronous, occurring after each LOW to HIGH clock transition. Since the LS195A utilizes edge-triggering, there is no restriction on the activity of the J, $\overline{K}$, P_n and $\overline{PE}$ inputs for logic operation – except for the set-up and release time requirements.

A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

MODE SELECT – TRUTH TABLE

OPERATING MODES	INPUTS					OUTPUTS				
	$\overline{MR}$	$\overline{PE}$	J	$\overline{K}$	P_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Asynchronous Reset	L	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, Reset First Stage	H	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, Toggle First Stage	H	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, Retain First Stage	H	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel Load	H	l	X	X	P_n	P_0	P_1	P_2	P_3	$\overline{P}_3$

L = LOW voltage levels
H = HIGH voltage levels
X = Don't Care
l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition.
h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition.
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS195AX	4.5 V	5.0 V	5.5 V	–55°C to +125°C
SN74LS195AX	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type, W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			0.65	1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			14	21	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Shift Frequency	30	40		MHz	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		16 17	21 24	ns	Fig. 1	
t_{PHL}	Propagation Delay, MR to Output		17	26	ns	Fig. 3	

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
$t_{W(CP)}$	Clock Pulse Width	16	7		ns	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
$t_{s(Data)}$	Set-up Time, Data to Clock	15	11		ns	Fig. 2	
$t_{h(Data)}$	Hold Time, Data to Clock	0	−3		ns		
$t_{s(\overline{PE})}$	Set-up Time, $\overline{PE}$ Control to Clock	25	18		ns	Fig. 4	
$t_{h(\overline{PE})}$	Hold Time, $\overline{PE}$ Control to Clock	0	−7		ns		
$t_{W(\overline{MR})}$	Master Reset Pulse Width	12	8		ns	Fig. 3	
$t_{rec(\overline{MR})}$	Recovery Time Master Reset to Clock	20	3		ns		

SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

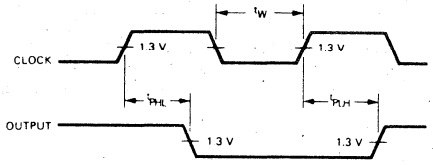
HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

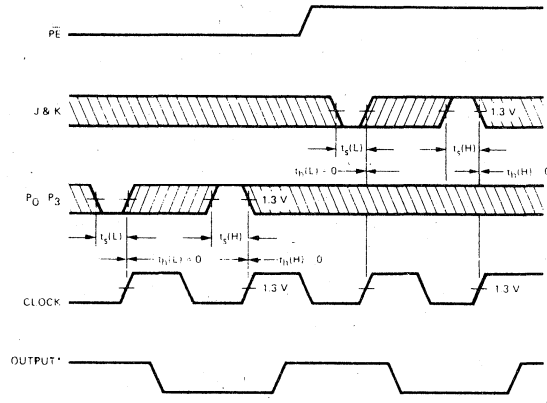
CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



CONDITIONS: J = $\overline{PE}$ = $\overline{MR}$ = H
$\overline{K}$ = L

Fig. 1

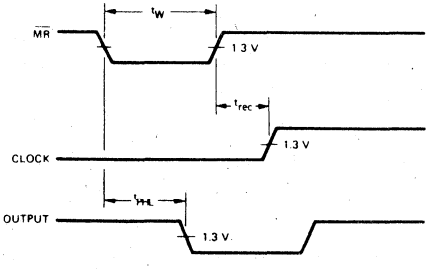
SET-UP (t_s) AND HOLD (t_h) TIME FOR SERIAL DATA (J & $\overline{K}$) AND PARALLEL DATA (P_0, P_1, P_2, P_3)



CONDITIONS: $\overline{MR}$ = H
*J and $\overline{K}$ set-up time affects Q_0 only

Fig. 2

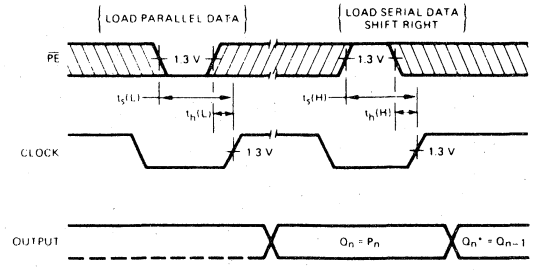
MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



CONDITIONS: $\overline{PE}$ = L
P_0 = P_1 = P_2 = P_3 = H

Fig. 3

SET-UP (t_s) AND HOLD (t_h) TIME FOR $\overline{PE}$ INPUT



CONDITIONS: $\overline{MR}$ = H
*Q_0 state will be determined by J and $\overline{K}$ inputs

Fig. 4

SN54LS196/SN74LS196
SN54LS197/SN74LS197

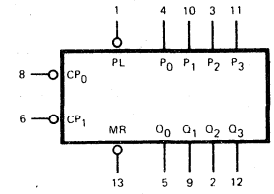
4-STAGE PRESETTABLE RIPPLE COUNTERS

DESCRIPTION – The SN54LS196/SN74LS196 decade counter is partitioned into divide-by-two and divide-by-five sections which can be combined to count either in BCD (8,4,2,1) sequence or in a bi-quinary mode producing a 50% duty cycle output. The SN54LS197/SN74LS197 contains divide-by-two and divide-by-eight sections which can be combined to form a modulo-16 binary counter. Low Power Schottky technology is used to achieve typical count rates of 70 MHz and power dissipation of only 80 mW.

Both circuit types have a Master Reset ($\overline{MR}$) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input ($\overline{PL}$) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs (P_n) into the flip-flops. This preset feature makes the circuits usable as programmable counters. The circuits can also be used as 4-bit latches, loading data from the Parallel Data inputs when $\overline{PL}$ is LOW and storing the data when $\overline{PL}$ is HIGH.

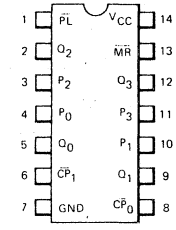
- LOW POWER CONSUMPTION – TYPICALLY 80 mW
- HIGH COUNTING RATES – TYPICALLY 70 MHz
- CHOICE OF COUNTING MODES – BCD, BI-QUINARY, BINARY
- ASYNCHRONOUS PRESETTABLE
- ASYNCHRONOUS MASTER RESET
- EASY MULTISTAGE CASCADING
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)

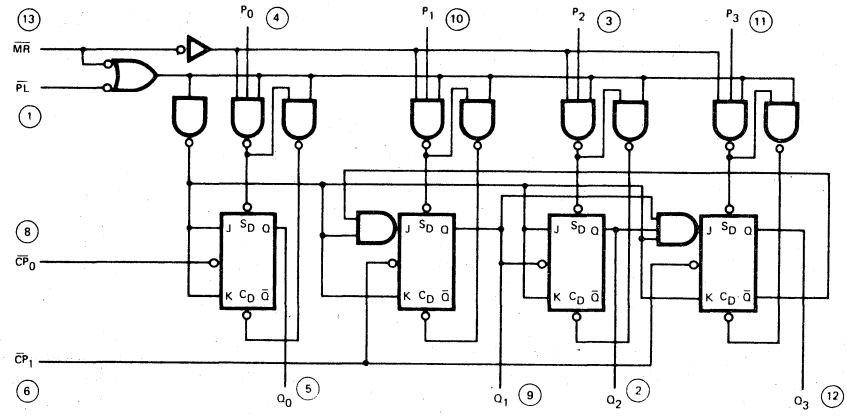


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

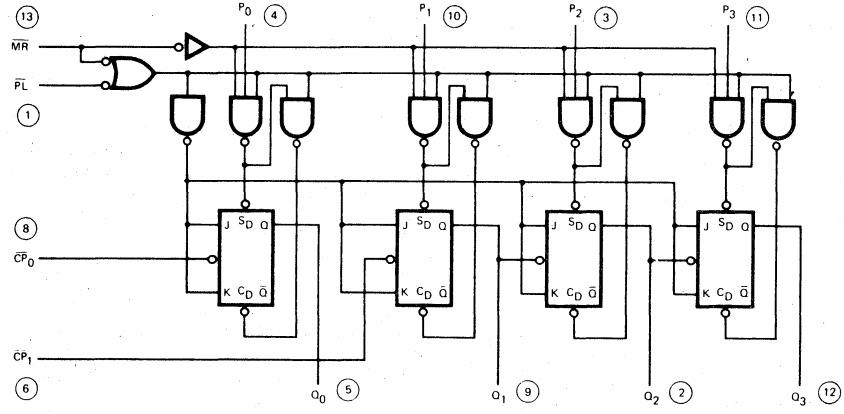
PIN NAMES		LOADING (Note a)	
		HIGH	LOW
$\overline{CP}_0$	Clock (Active LOW Going Edge) Input to Divide-by-Two Section	1.0 U.L.	1.5 U.L.
$\overline{CP}_1$	Clock (Active LOW Going Edge) Input to Divide-by-Five Section	2.0 U.L.	1.75 U.L.
$\overline{CP}_1$	Clock (Active LOW Going Edge) Input to Divide-by-Eight Section	1.0 U.L.	1.0 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	1.0 U.L.	0.5 U.L.
$\overline{PL}$	Parallel Load (Active LOW) Input	0.5 U.L.	0.25 U.L.
P_0-P_3	Data Inputs	0.5 U.L.	0.25 U.L.
Q_0-Q_3	Outputs (Notes b, c)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.
c. In addition to loading shown, Q_0 can also drive $\overline{CP}_1$.

LOGIC DIAGRAM



LS196



LS197

V_{CC} = Pin 14
GND = Pin 7
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — The LS196 and LS197 are asynchronously presettable decade and binary ripple counters. The LS196 Decade Counter is partitioned into divide-by-two and divide-by-five sections while the LS197 is partitioned into divide-by-two and divide-by-eight sections, with all sections having a separate Clock input. In the counting modes, state changes are initiated by the HIGH to LOW transition of the clock signals. State changes of the Q outputs, however, do not occur simultaneously because of the internal ripple delays. When using external logic to decode the Q outputs, designers should bear in mind that the unequal delays can lead to decoding spikes and thus a decoded signal should not be used as a clock or strobe. The $\overline{CP_0}$ input serves the Q_0 flip-flop in both circuit types while the $\overline{CP_1}$ input serves the divide-by-five or divide-by-eight section. The Q_0 output is designed and specified to drive the rated fan-out plus the $\overline{CP_1}$ input. With the input frequency connected to $\overline{CP_0}$ and Q_0 driving $\overline{CP_1}$, the LS197 forms a straightforward module-16 counter, with Q_0 the least significant output and Q3 the most significant output.

The LS196 Decade Counter can be connected up to operate in two different count sequences, as indicated in the tables of Figure 2. With the input frequency connected to $\overline{CP_0}$ and with Q_0 driving $\overline{CP_1}$, the circuit counts in the BCD (8, 4, 2, 1) sequence. With the input frequency connected to $\overline{CP_1}$ and Q_3 driving $\overline{CP_0}$, Q_0 becomes the low frequency output and has a 50% duty cycle waveform. Note that the maximum counting rate is reduced in the latter (bi-quinary) configuration because of the interstage gating delay within the divide-by-five section.

The LS196 and LS197 have an asynchronous active LOW Master Reset input (MR) which overrides all other inputs and forces all outputs LOW. The counters are also asynchronously presettable. A LOW on the Parallel Load input (PL) overrides the clock inputs and loads the data from Parallel Data ($P_0 - P_3$) inputs into the flip-flops. While PL is LOW, the counters act as transparent latches and any change in the P_n inputs will be reflected in the outputs.

Figure 2: LS196 COUNT SEQUENCES

DECADE (NOTE 1)					BI-QUINARY (NOTE 2)				
COUNT	Q_3	Q_2	Q_1	Q_0	COUNT	Q_0	Q_3	Q_2	Q_1
0	L	L	L	L	0	L	L	L	L
1	L	L	L	H	1	L	L	L	H
2	L	L	H	L	2	L	L	H	L
3	L	L	H	H	3	L	L	H	H
4	L	H	L	L	4	L	H	L	L
5	L	H	L	H	5	H	L	L	L
6	L	H	H	L	6	H	L	L	H
7	L	H	H	H	7	H	L	H	L
8	H	L	L	L	8	H	L	H	H
9	H	L	L	H	9	H	H	L	L

NOTES:
1. Signal applied to CP_0, Q_0 connected to CP_1.
2. Signal applied to CP_1, Q_3 connected to CP_0.

MODE SELECT TABLE

INPUTS			RESPONSE
$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	
L	X	X	Reset (Clear)
H	L	X	Parallel Load
H	H	⌐	Count

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
⌐ = HIGH to Low Clock Transition

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
SN54LS196X SN54LS197X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS196X SN74LS197X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		74	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current $\overline{PL}$, P_0, P_1, P_2, P_3 $\overline{MR}$, $\overline{CP_0}$, $\overline{CP_1}$ (LS197) $\overline{CP_1}$ (LS196)				20 40 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	$\overline{PL}$, P_0, P_1, P_2, P_3 $\overline{MR}$, $\overline{CP_0}$, $\overline{CP_1}$ (LS197) $\overline{CP_1}$ (LS196)				0.1 0.2 0.4	mA	V_{CC} = MAX, V_{IN} = 10 V V_{CC} = MAX, V_{IN} = 5.5 V V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current $\overline{PL}$, P_0, P_1, P_2, P_3 $\overline{MR}$ $\overline{CP_0}$ $\overline{CP_1}$ (LS196) $\overline{CP_1}$ (LS197)				−0.4 −0.8 −2.4 −2.8 −1.3	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			12	20	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS	
		LS196			LS197					
		MIN	TYP	MAX	MIN	TYP	MAX			
f_{max}	Input Count Frequency	45	60		50	75		MHz	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	$\overline{CP_0}$ Input to Q_0 Output		8.0 8.0	12 12		8.0 8.0	12 12	ns	Fig. 1	
t_{PLH} t_{PHL}	$\overline{CP_1}$ Input to Q_1 Output		9.0 9.0	14 14		9.0 9.0	14 14	ns		
t_{PLH} t_{PHL}	$\overline{CP_1}$ Input to Q_2 Output		23 21	34 32		26 23	36 34	ns		
t_{PLH} t_{PHL}	$\overline{CP_1}$ Input to Q_3 Output		12 12	18 18		35 38	50 55	ns		
t_{PLH} t_{PHL}	P_0, P_1, P_2, P_3 Inputs Q_0, Q_1, Q_2, Q_3 Outputs		10 24	15 35		10 24	15 35	ns	Fig. 2	
t_{PLH} t_{PHL}	$\overline{PL}$ Input to Any Output		15 24	24 35		15 24	24 35	ns	Fig. 3	
t_{PHL}	$\overline{MR}$ Input to Any Output		26	37		26	37	ns	Fig. 4	

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS	
		LS196			LS197					
		MIN	TYP	MAX	MIN	TYP	MAX			
t_W	$\overline{CP_0}$ Pulse Width	12			10			ns	Fig. 1	V_{CC} = 5.0 V
t_W	$\overline{CP_1}$ Pulse Width	24			20			ns		
t_W	$\overline{PL}$ Pulse Width	18			18			ns	Fig. 3	
t_W	$\overline{MR}$ Pulse Width	12			12			ns	Fig. 4	
t_sL	Set-up Time LOW Data to $\overline{PL}$	12			12			ns	Fig. 5	
t_hL	Hold Time LOW Data to $\overline{PL}$	6.0			6.0			ns		
t_sH	Set-up Time HIGH Data to $\overline{PL}$	8.0			8.0			ns		
t_hH	Hold Time HIGH Data to $\overline{PL}$	0			0			ns		
t_{rec}	Recovery Time $\overline{PL}$ to $\overline{CP}$	16			16			ns	Fig. 4	
t_{rec}	Recovery Time $\overline{MR}$ to $\overline{CP}$	18			18			ns		

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

RECOVERY TIME (t_{rec}) – is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH to LOW in order to recognize and transfer LOW Data to the Q outputs.

AC WAVEFORMS

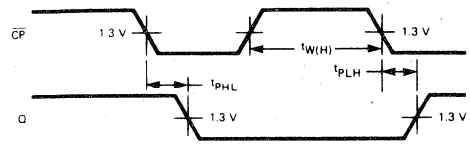
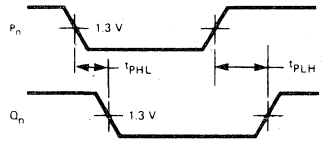


Fig. 1



NOTE: $\overline{PL}$ = LOW

Fig. 2

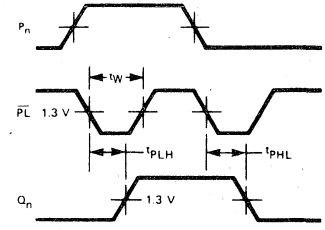


Fig. 3

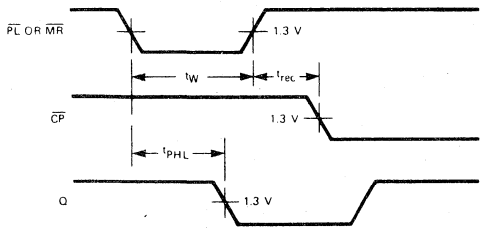
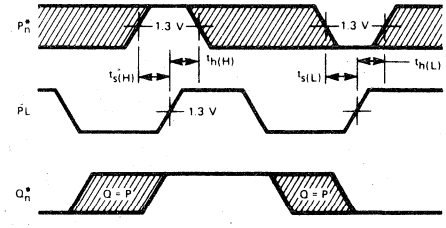


Fig. 4



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 5

SN54LS221/SN74LS221

DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

Advance Information

DESCRIPTION – Each multivibrator of the LS221 features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a voltage level and is not related to the transition time of the input pulse. Schmitt-trigger input circuitry for B input allows jitter-free triggering for inputs as slow as 1 volt/second, providing the circuit with excellent noise immunity. A high immunity to V_{CC} noise is also provided by internal latching circuitry.

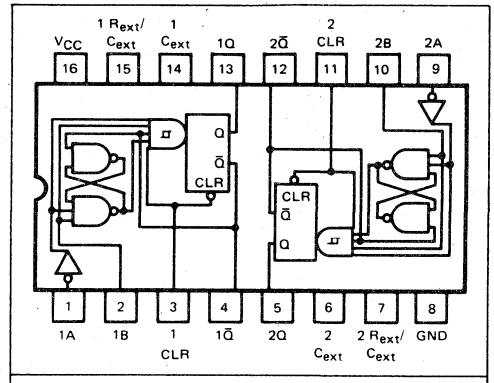
Once triggered, the outputs are independent of further transitions of the inputs and are a function of the timing components. The output pulses can be terminated by the overriding clear. Input pulse width may be of any duration relative to the output pulse width. Output pulse width may be varied from 35 nanoseconds to a maximum of 70 s by choosing appropriate timing components. With R_{ext} = 2 kΩ and C_{ext} = 0, a typical output pulse of 30 nanoseconds is achieved. Output rise and fall times are independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for greater than six decades of timing capacitance (10 pF to 10 μF), and greater than one decade of timing resistance (2 to 70 kΩ for the SN54LS221, and 2 to 100 kΩ for the SN74LS221). Pulse width is defined by the relationship: $t_{w(out)} = C_{ext}R_{ext}$ in2 ≈0.7 $C_{ext}R_{ext}$. If pulse cutoff is not critical, capacitance up to 1000 μF and resistance as low as 1.4 kΩ may be used. The range of jitter-free pulse widths is extended if V_{CC} is 5 V and 25°C temperature.

- **SN54LS221 and SN74LS221 IS A DUAL HIGHLY STABLE ONE-SHOT**
- **OVERRIDING CLEAR TERMINATES OUTPUT PULSE**
- **PIN OUT IS IDENTICAL TO SN54LS/74LS123**

(TOP VIEW)



positive logic: Low input to clear resets Q low and Q̄ high regardless of d-c levels at A or B inputs.

FUNCTION TABLE

(EACH MONOSTABLE)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

TYPE	TYPICAL POWER DISSIPATION	MAXIMUM OUTPUT PULSE LENGTH
SN54LS221	23 mW	49 s
SN74LS221	23 mW	70 s

This is advance information and specifications are subject to change without notice.

SN54LS240/SN74LS240 • SN54LS241/SN74LS241 • SN54LS244/SN74LS244

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

DESCRIPTION—The 54LS/74LS240, 241 and 244 are Octal Buffers and Line Drivers designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved PC board density.

- HYSTERESIS AT INPUTS TO IMPROVE NOISE MARGINS
- 3-STATE OUTPUTS DRIVE BUS LINES OR BUFFER MEMORY ADDRESS REGISTERS
- OUTPUTS SINK 40 mA AT V_{OL} = 0.5 V
- 10 mA SOURCE CURRENT
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

TRUTH TABLES

54LS/74LS240

INPUTS		OUTPUT
$\overline{E}_1, \overline{E}_2$	D	
L	L	H
L	H	L
H	X	(Z)

54LS/74LS244

INPUTS		OUTPUT
$\overline{E}_1, \overline{E}_2$	D	
L	L	L
L	H	H
H	X	(Z)
H	X	(Z)

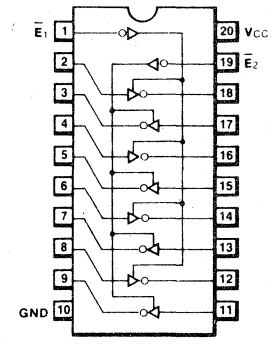
54LS/74LS241

INPUTS		OUTPUT	INPUTS		OUTPUT
$\overline{E}_1$	D		E_2	D	
L	L	L	H	L	L
L	H	H	H	H	H
H	X	(Z)	L	X	(Z)
H	X	(X)	L	X	(Z)

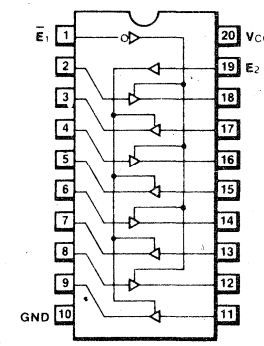
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance

LOGIC AND CONNECTION DIAGRAMS
DIP (TOP VIEW)

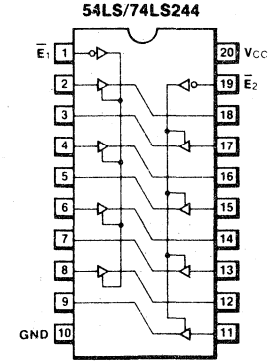
54LS/74LS240



54LS/74LS241



54LS/74LS244



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS240X, SN54LS244X SN54LS241X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS240X, SN74LS244X SN74LS241X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGES (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	I_{OH} = −12 mA	V_{CC} = MIN, V_{IN} = V_{IH}
		74	2.4	3.1			I_{OH} = −15 mA	or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} = V_{IH}
		74		0.35	0.5	V	I_{OL} = 24 mA	or V_{IL} per Truth Table
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2.0 V	
I_{OZL}	Input Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, V_E = 2.0 V	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)		−50		−225	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current	LS240		29	50	mA	V_{CC} = MAX, V_{IN} = 0 V, V_E = 4.5 V	
		LS241, LS244		32	54			

NOTES:
1. For conditions shown as MIN or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay, Data to Output 54LS/74LS240			14 18	ns	Fig. 2	C_L = 45 pF
t_{PLH} t_{PHL}	Propagation Delay, Data to Output 54LS/74LS241, 54LS/74LS244			18 18	ns	Fig. 1	C_L = 45 pF
t_{PZH}	Output Enable Time to HIGH Level			23	ns	Figs. 4, 5	C_L = 45 pF R_L = 667 Ω
t_{PZL}	Output Enable Time to LOW Level			30	ns	Figs. 3, 5	
t_{PLZ}	Output Disable Time from LOW Level			25	ns	Figs. 3, 5	C_L = 5.0 pF R_L = 667 Ω
t_{PHZ}	Output Disable Time from HIGH Level			18	ns	Figs. 4, 5	

AC WAVEFORMS

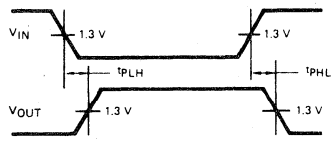


Fig.1

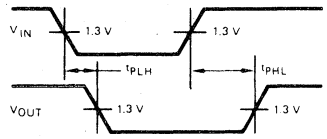


Fig. 2

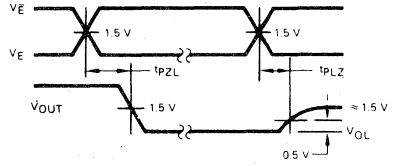


Fig. 3

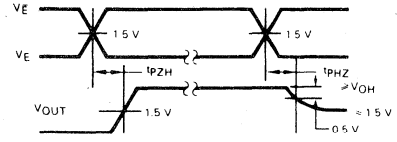
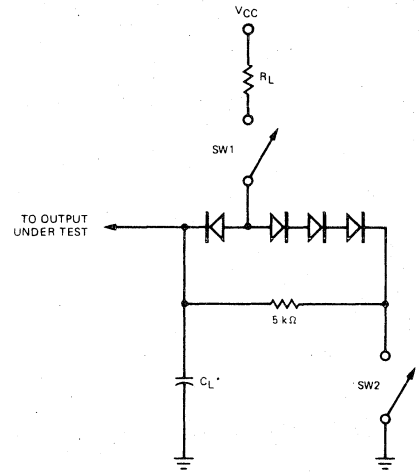


Fig. 4



SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 5

SN54LS242/SN74LS242 • SN54LS243/SN74LS243

QUAD BUS TRANSCEIVER

DESCRIPTION—The 54LS/74LS242 and 54LS/74LS243 are Quad Bus Transmitters/Receivers designed for 4-line asynchronous 2-way data communications between data buses.

- HYSTERESIS AT INPUTS TO IMPROVE NOISE IMMUNITY
- 2-WAY ASYNCHRONOUS DATA BUS COMMUNICATION
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

TRUTH TABLES

54LS/74LS242

INPUTS		OUTPUT	INPUTS		OUTPUT
$\overline{E}_1$	D		E_2	D	
L	L	H	L	X	(Z)
L	H	L	L	X	(Z)
H	X	(Z)	H	L	H
H	X	(Z)	H	H	L

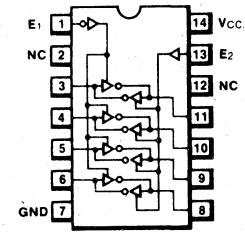
54LS/74LS243

INPUTS		OUTPUT	INPUTS		OUTPUT
$\overline{E}_1$	D		E_2	D	
L	L	L	L	X	(Z)
L	H	H	L	X	(Z)
H	X	(Z)	H	L	L
H	X	(Z)	H	H	H

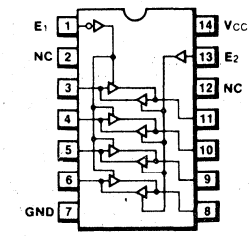
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedence

LOGIC AND CONNECTION DIAGRAMS
DIP (TOP VIEW)

54LS/74LS242



54LS/74LS243



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS242X SN54LS243X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS242X SN74LS243X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGES (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	I_{OH} = −12 mA	V_{CC} = MIN, V_{IN} = V_{IH}
		74	2.4	3.1			I_{OH} = −15 mA	or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} = V_{IH}
		74		0.35	0.5	V	I_{OL} = 24 mA	or V_{IL} per Truth Table
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2.0 V	
I_{OZL}	Input Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, V_E = 2.0 V	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)		−50		−225	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current	LS242		29	50	mA	V_{CC} = MAX, V_{IN} = 0 V, V_E = 4.5 V	
		LS243		32	54			

NOTES:
1. For conditions shown as MIN or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output 54LS/74LS242			14 18	ns	Fig. 2	C_L = 45 pF
t_{PLH} t_{PHL}	Propagation Delay, Data to Output 54LS/74LS243			18 18	ns	Fig. 1	C_L = 45 pF
t_{PZH}	Output Enable Time to HIGH Level			23	ns	Figs. 4, 5	C_L = 45 pF
t_{PZL}	Output Enable Time to LOW Level			30	ns	Figs. 3, 5	R_L = 667 Ω
t_{PLZ}	Output Disable Time from LOW Level			25	ns	Figs. 3, 5	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level			18	ns	Figs. 4, 5	R_L = 667 Ω

AC WAVEFORMS

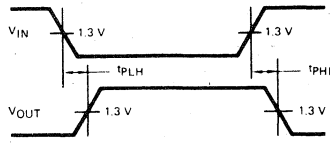


Fig.1

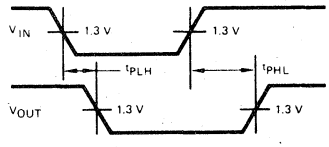


Fig. 2

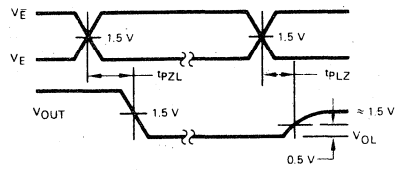


Fig. 3

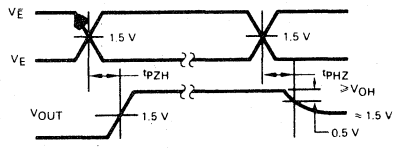
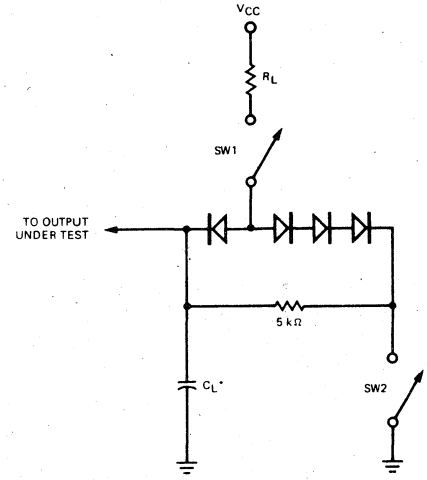


Fig. 4



SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 5

Advance Information

SN54LS245/SN74LS245

OCTAL BUS TRANSCEIVER

DESCRIPTION—The 54LS/74LS245 is an Octal Bus Transmitter/Receiver designed for 8-line asynchronous 2-way data communication between data buses. Direction Input (DR) controls transmission of Data from bus A to bus B or bus B to bus A depending upon its logic level. The Enable input ($\overline{E}$) can be used to isolate the buses.

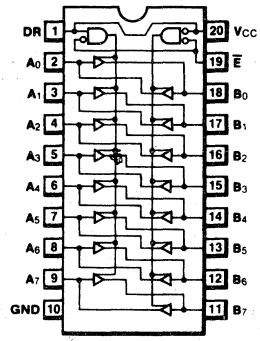
- **HYSTERESIS INPUTS TO IMPROVE NOISE IMMUNITY**
- **2-WAY ASYNCHRONOUS DATA BUS COMMUNICATION**
- **INPUT DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

TRUTH TABLE

INPUTS		OUTPUT
$\overline{E}$	DR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS245X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS245X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

This is advance information and specifications are subject to change without notice.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Output LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{CD}	Input Clamp Diode Voltage				−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4				I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4				I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	54, 74			0.4	V	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74			0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2.0 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, V_E = 2.0 V	
I_{IH}	Input HIGH Current				20 0.1	μA mA	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 10V	
I_{IL}	Input LOW Current				−0.2	mA	V_{CC} = MAX, V_{IN} = 0.4V	
I_{OS}	Output Short Circuit Current (Note 3)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current	Total, Output HIGH			60	mA	V_{CC} = MAX, Outputs Open	
		Total, Output LOW			85			
		Total at HIGH-Z			75			

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V (See Chapter 1 for Waveforms)

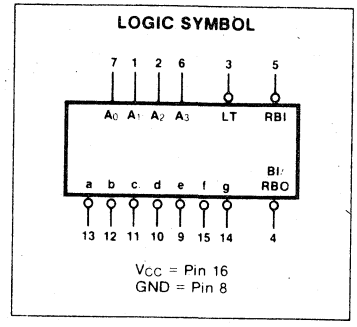
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output			18 18	ns	Figs. 1, 2	C_L = 45 pF
t_{PZH}	Output Enable Time to HIGH Level			25	ns	Figs. 4, 5	C_L = 45 pF
t_{PZL}	Output Enable Time to LOW Level			30	ns	Figs. 3, 5	R_L = 667 Ω
t_{PLZ}	Output Disable Time from LOW Level			25	ns	Figs. 3, 5	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level			18	ns	Figs. 4, 5	R_L = 667 Ω

SN54LS247/SN74LS247

BCD TO 7-SEGMENT DECODER/DRIVER

Advance Information

DESCRIPTION — The 54LS/74LS247 has active LOW open-collector outputs guaranteed to sink 12 mA (MILITARY) or 24 mA (COMMERICAL). It has the same electrical characteristics and pin connections as the 54LS/74LS47. The only difference is that the 54LS/74LS247 will light the top bar (segment a) for numeral 6 and the bottom bar (segment d) for numeral 9.

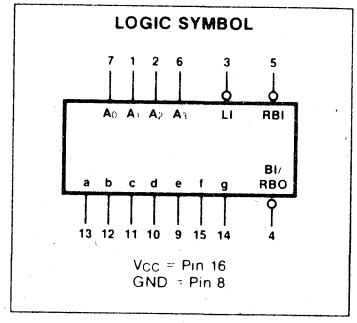


SN54LS248/SN74LS248

BCD TO 7-SEGMENT DECODER

Advance Information

DESCRIPTION —The 54LS/74LS248 has active HIGH outputs with internal 2 kΩ pullup resistors. It has the same electrical characteristics and pin connections as the 54LS/74LS48. The only difference is that the 54LS/74LS248 will light the top bar (segment a) for numeral 6 and the bottom bar (segment d) for numeral 9.

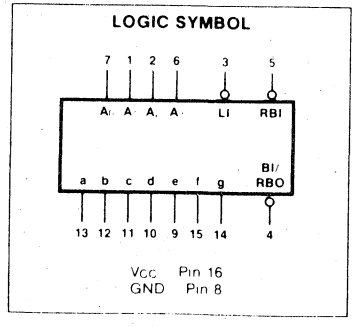


SN54LS249/SN74LS249

BCD TO 7-SEGMENT DECODER

Advance Information

DESCRIPTION — The 54LS/74LS249 has active HIGH open-collector outputs and is the 16-pin version of the 14 pin 54LS/74LS49. The 54LS/74LS249 incorporates the Lamp Test and BI/RBO inputs that are omitted in the 54LS/74LS49. Additionally, the 54LS/74LS249 will light the top bar (segment a) for numeral 6 and the bottom bar (segment d) for numeral 9.



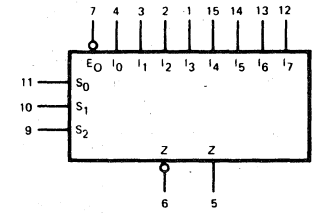
SN54LS251/SN74LS251

8-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION – The TTL/MSI SN54LS251/SN74LS251 is a high speed 8-Input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The LS251 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

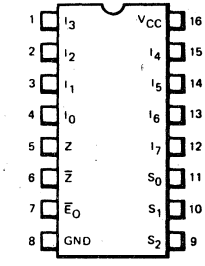
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **INVERTING AND NON-INVERTING 3-STATE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



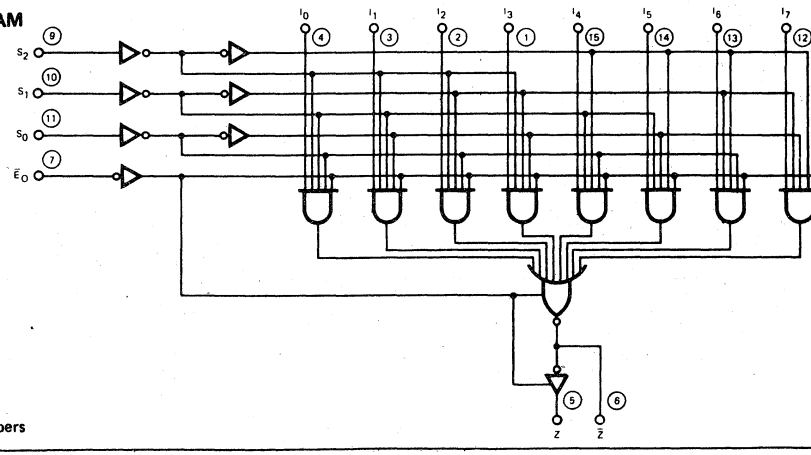
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOW
$S_0 - S_2$	Select Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_O$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_0 - I_7$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output (Note b)	65 (25) U.L.	5 (2.5) U.L.
$\overline{Z}$	Complementary Multiplexer Output (Note b)	65 (25) U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — The LS251 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Output Enable input ($\overline{E}_O$) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{E}O \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

When the Output Enable is HIGH, both outputs are in the high impedance (high Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltages.

TRUTH TABLE

$\overline{E}_0$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	(Z)	(Z)
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High Impedance (Off)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS251X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS251X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	I_{OH} = −1.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1		V	I_{OH} = −2.6 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V, $V_{\overline{E}}$ = 2.0 V
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{SC}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current, Outputs LOW			6.1	10	mA	V_{CC} = MAX, V_{IN} = 4.5 V, $V_{\overline{E}}$ = 0 V
	Power Supply Current, Outputs Off			7.1	12	mA	V_{CC} = MAX, V_{IN} = 4.5 V, $V_{\overline{E}}$ = 4.5 V

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Select to $\overline{Z}$ Output		11 23	20 33	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Z Output		30 18	45 30	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, Data to $\overline{Z}$ Output		7.0 10	12 15	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data to Z Output		18 15	27 23	ns	Fig. 2	
t_{PZH}	Output Enable Time to HIGH Level		12	20	ns	Figs. 4, 5	C_L = 15 pF R_L = 2 kΩ
t_{PZL}	Output Enable Time to LOW Level		17	25	ns	Figs. 3, 5	
t_{PLZ}	Output Disable Time from LOW Level		12	20	ns	Figs. 3, 5	C_L = 5 pF R_L = 2 kΩ
t_{PHZ}	Output Disable Time from HIGH Level		17	25	ns	Figs. 4, 5	

3-STATE AC WAVEFORMS

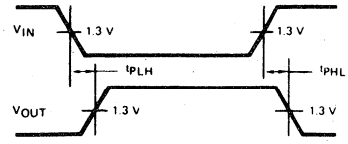


Fig. 1

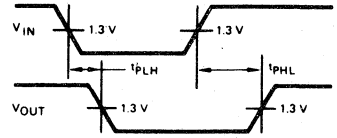


Fig. 2

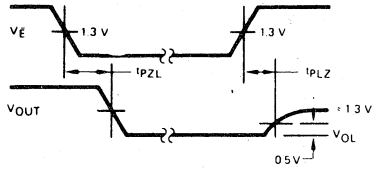


Fig. 3

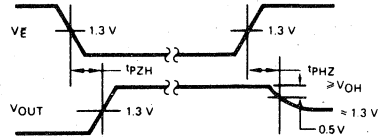
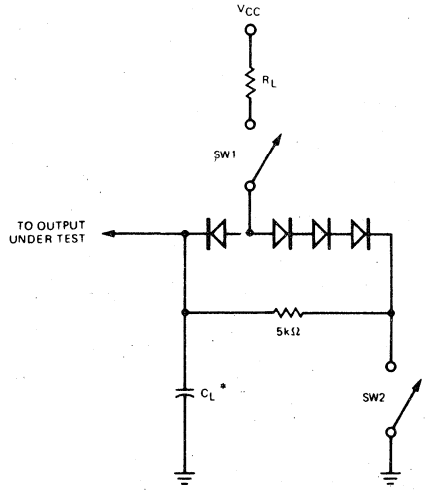


Fig. 4

AC LOAD CIRCUIT



*Includes Jig and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 5

SN54LS253/SN74LS253

DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

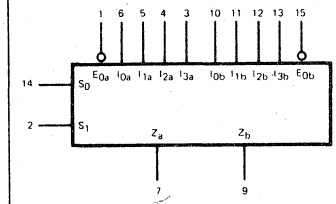
DESCRIPTION — The LSTTL/MSI SN54LS253/SN74LS253 is a Dual 4-Input Multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable (E_O) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **NON-INVERTING 3-STATE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES		LOADING (Note a) HIGH	LOW
S_0, S_1	Common Select Inputs	0.5 U.L.	0.25 U.L.
Multiplexer A			
$\overline{E}_{0a}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{3a}$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z_a	Multiplexer Output (Note b)	65(25) U.L.	5(2.5) U.L.
Multiplexer B			
$\overline{E}_{0b}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_{0b} - I_{3b}$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z_b	Multiplexer Output (Note b)	65(25) U.L.	5(2.5) U.L.

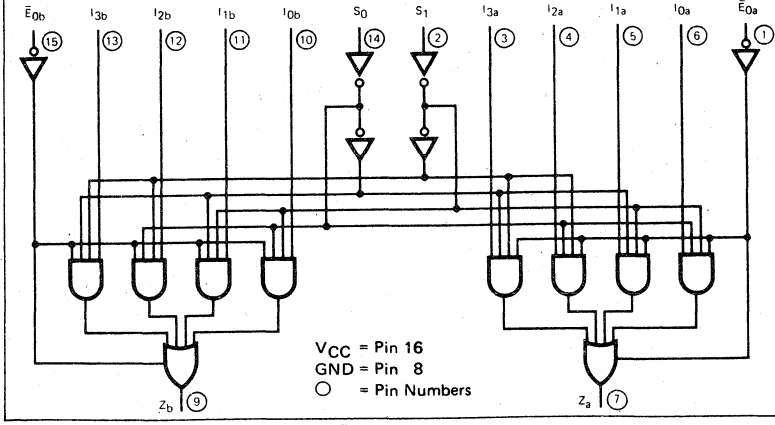
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military and 65 U.L. for Commercial Temperature Ranges.

LOGIC SYMBOL



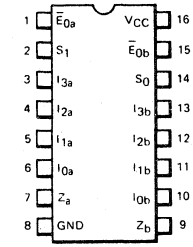
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS253 contains two identical 4-Input Multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{E}_{0a}$, $\overline{E}_{0b}$) inputs which when HIGH, forces the outputs to a high impedance (high Z) state.

The LS253 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{E}_{0a} \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$
$$Z_b = \overline{E}_{0b} \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{E}_0$	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH Level
L = LOW Level
X = Irrelevant
(Z) = High Impedance (off)
Address inputs S_0 and S_1 are common to both sections.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS253X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS253X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type: W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	I_{OH} = −1.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1			I_{OH} = −2.6 mA
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V, $V_{\overline{E}}$ = 2.0 V
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{SC}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current, Outputs LOW			7.0	12	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 0 V
	Power Supply Current, Outputs Off			8.5	14		V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C (See SN54LS251 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		10 10	15 15	ns	Fig. 1	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		20 16	29 24	ns	Fig. 1	C_L = 15 pF
t_{PZH}	Output Enable Time to HIGH Level		12	18	ns	Figs. 4, 5	C_L = 15 pF, R_L = 2 kΩ
t_{PZL}	Output Enable Time to LOW Level		11	18	ns	Figs. 3, 5	
t_{PLZ}	Output Disable Time from LOW Level		22	32	ns	Figs. 3, 5	C_L = 5 pF, R_L = 2 kΩ
t_{PHZ}	Output Disable Time from HIGH Level		11	18	ns	Figs. 4, 5	

SN54LS256/SN74LS256
DUAL 4-BIT ADDRESSABLE LATCH

DESCRIPTION – The 54LS/74LS256 is a Dual 4-Bit Addressable Latch with common control inputs; these include two Address inputs (A_0, A_1), an active LOW Enable input (E) and an active LOW Clear input (C). Each latch has a Data input (D) and four outputs (Q_0-Q_3).

When the Enable ($\overline{E}$) is HIGH and the Clear input ($\overline{C}$) is LOW, all outputs (Q_0-Q_3) are LOW. Dual 4-channel demultiplexing occurs when the $\overline{C}$ and $\overline{E}$ are both LOW. When $\overline{C}$ is HIGH and $\overline{E}$ is LOW, the selected output (Q_0-Q_3), determined by the Address inputs, follows D. When the $\overline{E}$ goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ($\overline{E}$=LOW, $\overline{C}$=HIGH), changing more than one bit of the Address (A_0, A_1) could impose a transient wrong address. Therefore, this should be done only while in the memory mode ($\overline{E}$=$\overline{C}$=HIGH).

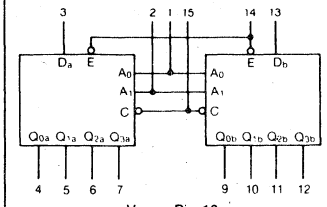
- **SERIAL-TO-PARALLEL CAPABILITY**
- **OUTPUT FROM EACH STORAGE BIT AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **EASILY EXPANDABLE**
- **ACTIVE LOW COMMON CLEAR**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATABLE**

PIN NAMES

		LOADING (Note a) HIGH	LOADING (Note a) LOW
A_0, A_1	Address Inputs	0.5 U.L.	0.25 U.L.
D_a, D_b	Data Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable Input (Active LOW)	1.0 U.L.	0.5 U.L.
$\overline{C}$	Clear Input (Active LOW)	0.5 U.L.	0.25 U.L.
Q_{0a}-Q_{3a}, Q_{0b}-Q_{3b}	Parallel Latch Outputs (Note b)	10 U.L.	5 (2.5) U.L.

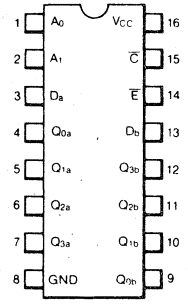
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



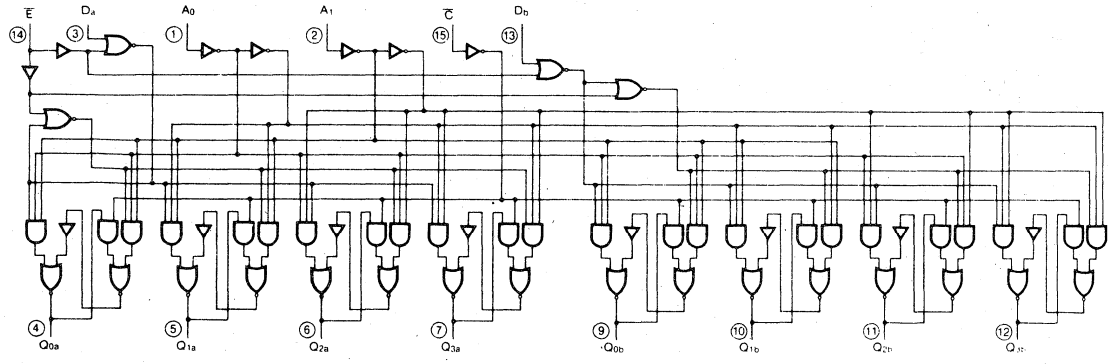
VCC = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



VCC = Pin 16
GND = Pin 8
○ = Pin Numbers

TRUTH TABLE

$\overline{C}$	$\overline{E}$	D	A_0	A_1	Q_0	Q_1	Q_2	Q_3	MODE
L	H	X	X	X	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	H	L	L	L	
L	L	L	H	L	L	L	L	L	
L	L	H	H	L	L	H	L	L	
L	L	L	L	H	L	L	L	L	
L	L	H	L	H	L	L	H	L	
L	L	L	H	H	L	L	L	L	
L	L	H	H	H	L	L	L	H	
H	H	X	X	X	Q_{N-1}	Q_{N-1}	Q_{N-1}	Q_{N-1}	Memory
H	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1}	Addressable
H	L	H	L	L	H	Q_{N-1}	Q_{N-1}	Q_{N-1}	Latch
H	L	L	H	L	Q_{N-1}	L	Q_{N-1}	Q_{N-1}	
H	L	H	H	L	Q_{N-1}	H	Q_{N-1}	Q_{N-1}	
H	L	L	L	H	Q_{N-1}	Q_{N-1}	L	Q_{N-1}	
H	L	H	L	H	Q_{N-1}	Q_{N-1}	H	Q_{N-1}	
H	L	L	H	H	Q_{N-1}	Q_{N-1}	Q_{N-1}	L	
H	L	H	H	H	Q_{N-1}	Q_{N-1}	Q_{N-1}	H	

H = High Voltage Level
L = LOW Voltage Level
X = Immaterial

MODE SELECTION

$\overline{E}$	$\overline{C}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Dual 4-Channel Demultiplexer
H	L	Clear

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS256X	4.5 V	5.0 V	5.5 V	-55° C to +125° C
SN74LS256X	4.75 V	5.0 V	5.25 V	0° C to +70° C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1			
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA V_{CC} = MIN, V_{IN} = V_{IH} I_{OL} = 8.0 mA or V_{IL} per Truth Table
		74		0.35	0.5		
V_{IH}	Input HIGH Level		2.0			V	Guaranteed Input Logical HIGH Voltage for All Inputs
V_{IL}	Input LOW Level	54			0.7	V	Guaranteed Input Logical LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage				−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{IL}	Input LOW Current A_0, A_1, $\overline{C}$, D_a, D_b E				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{IH}	Input HIGH Current A_0, A_1, $\overline{C}$, D_a, D_b E				20 40	μA	V_{CC} = MAX, V_{IN} = 2.4 V
I_{IH}	Input HIGH Current A_0, A_1, $\overline{C}$, D_a, D_b E				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			20	25	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operations under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and MAX loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25° C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn-Off Delay, Enable to Output		20	27	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn-On Delay, Enable to Output		16	24	ns	Fig. 1
t_{PLH}	Turn-Off Delay, Data to Output		20	30	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn-On Delay, Data to Output		13	20	ns	Fig. 2
t_{PLH}	Turn-Off Delay, Address to Output		20	30	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn-On Delay, Address to Output		14	20	ns	Fig. 3
t_{PHL}	Turn-On Delay, Clear to Output		12	18	ns	V_{CC} = 5.0 V, C_L = 15 pF Fig. 5

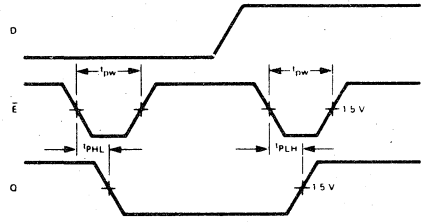
AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_s (H)	Set-up Time HIGH, Data to Enable	20	13		ns	$V_{CC} = 5.0$ V Fig. 4
t_h (H)	Hold Time HIGH, Data to Enable	0	-7.0		ns	
t_s (L)	Set-up Time LOW, Data to Enable	15	7.0		ns	
t_h (L)	Hold Time LOW, Data to Enable	0	10		ns	
t_s (A-$\overline{E}$)	Set-up Time, Address to Enable (Note 5)	0	-7.0		ns	$V_{CC} = 5.0$ V Fig. 6
t_{pw} ($\overline{E}$)	Enable Pulse Width	17	12		ns	$V_{CC} = 5.0$ V Fig. 1

NOTES:
5. The Address to Enable Set-up Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
6. The shaded areas indicate when the inputs are permitted to change for predictable output performance.

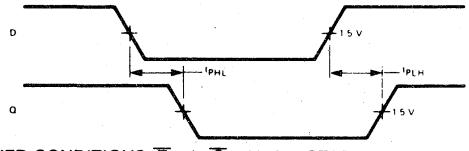
AC WAVEFORMS

Fig. 1 TURN-ON AND TURN-OFF DELAYS, ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



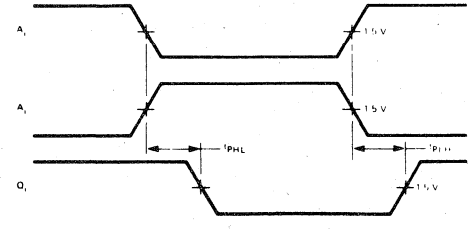
OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

Fig. 2 TURN-ON AND TURN-OFF DELAYS, DATA TO OUTPUT



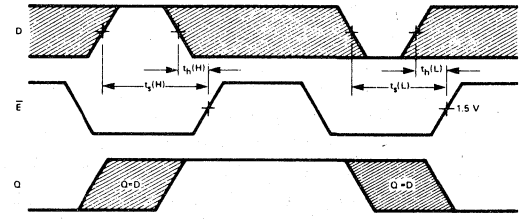
OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = H, A = STABLE

Fig. 3 TURN-ON AND TURN-OFF DELAYS, ADDRESS TO OUTPUT



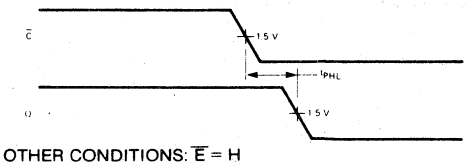
OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = L, D = H

Fig. 4 SET-UP AND HOLD TIME, DATA TO ENABLE



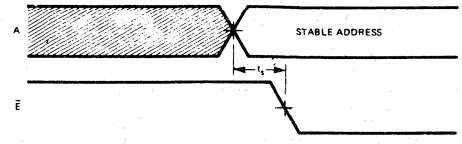
OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

Fig. 5 TURN-ON DELAY, CLEAR TO OUTPUT



OTHER CONDITIONS: $\overline{E}$ = H

Fig. 6 SET-UP TIME, ADDRESS TO ENABLE (SEE NOTES 5 AND 6)



OTHER CONDITIONS: $\overline{C}$ = H

SN54LS257A/SN74LS257A

QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION – The LSTTL/MSI SN54LS257A/SN74LS257A is a Quad 2-Input Multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable (E_O) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL familes.

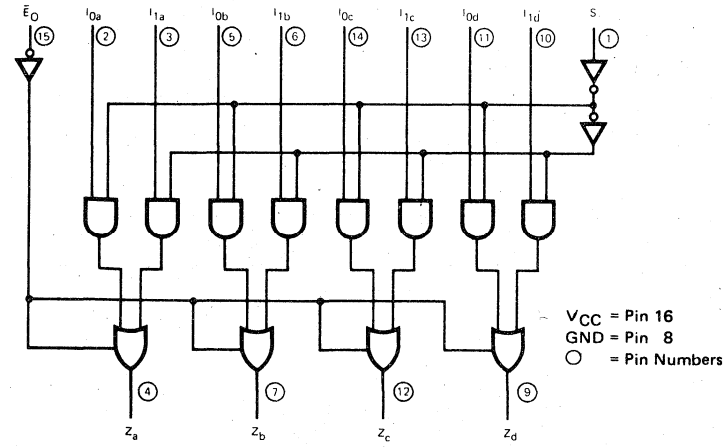
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER
- NON-INVERTING 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

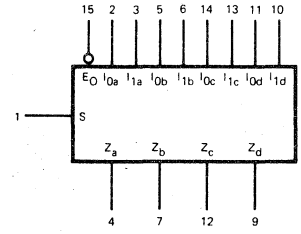
		LOADING (Note a) HIGH	LOW
S	Common Data Select Input	1.0 U.L.	0.5 U.L.
$\overline{E}_O$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{0d}$	Data Inputs from Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs from Source 1	0.5 U.L.	0.25 U.L.
$Z_a - Z_d$	Multiplexer Outputs (Note b)	65(25) U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM

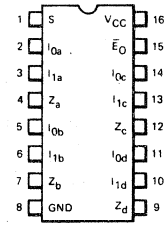


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS257A is a Quad 2-Input Multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a Common Data Select Input. When the Select Input is LOW, the I_0 inputs are selected and when Select is HIGH, the I_1 inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form.

The LS257A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E}_O \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \qquad Z_b = \overline{E}_O \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$Z_c = \overline{E}_O \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \qquad Z_d = \overline{E}_O \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

When the Output Enable Input ($\overline{E}_O$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{E}_O$	S	I_0	I_1	Z
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High impedance (off)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS257AX	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS257AX	4.75 V	5.0 V	5.25 V	0°C to + 70°C

X = package type: W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	I_{OH} = −1.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1		V	I_{OH} = −2.6 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, $V_{\overline{E}}$ = 2.0 V
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V
I_{IH}	Input HIGH Current $\overline{E}_0$, I_{0x}, I_{1x}				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	S				40		
	Input HIGH Current at MAX Input Voltage $\overline{E}_0$, I_{0x}, I_{1x}				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
	S				0.2		
I_{IL}	Input LOW Current $\overline{E}_0$, I_{0x}, I_{1x}				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	S				−0.8		
I_{OS}	Output Short Circuit Current (Note 4)		−30		−130	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current, Outputs HIGH				10	mA	V_{CC} = MAX, V_{IN} = 4.5 V, $V_{\overline{E}}$ = 0 V
	Power Supply Current, Outputs LOW				16		V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 0 V
	Power Supply Current, Outputs OFF				17		V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25° C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V (See SN54LS251 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH}	Propagation Delay, Data to Output			18	ns	Fig. 1	C_L = 45 pF
t_{PHL}				18			
t_{PLH}	Propagation Delay, Select to Output			21	ns	Fig. 1	C_L = 45 pF
t_{PHL}				21			
t_{PZH}	Output Enable Time to HIGH Level			30	ns	Figs. 4, 5	C_L = 45 pF
t_{PZL}	Output Enable Time to LOW Level			30	ns	Figs. 3, 5	R_L = 667 Ω
t_{PLZ}	Output Disable Time from LOW Level			25	ns	Figs. 3, 5	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level			30	ns	Figs. 4, 5	R_L = 667 Ω

SN54LS258A/SN74LS258A

QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION – The LSTTL/MSI SN54LS258A/SN74LS258A is a Quad 2-Input Multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{E}_O$) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

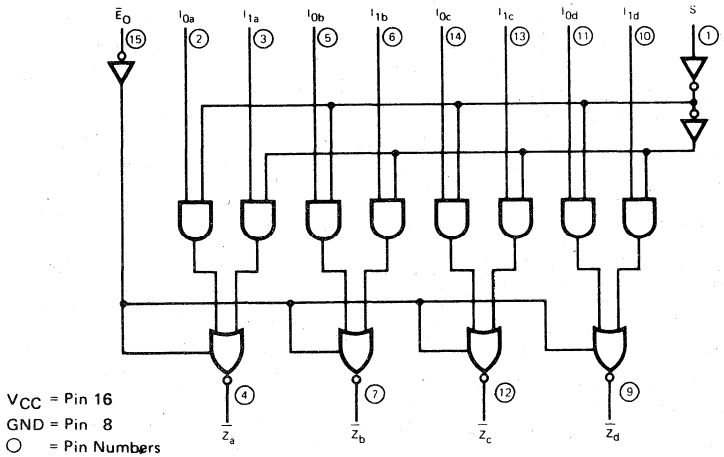
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER
- INVERTING 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

		LOADING (Note a	
		HIGH	LOW
S	Common Select Input	1.0 U.L.	0.5 U.L.
$\overline{E}_O$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{0d}$	Data Inputs from Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs from Source 1	0.5 U.L.	0.25 U.L.
$\overline{Z}_a - \overline{Z}_d$	Multiplexer Outputs (Note b)	65(25) U.L.	5(2.5) U.L.

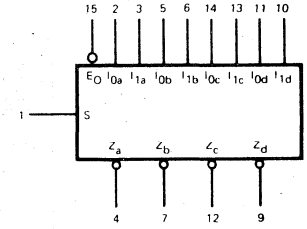
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



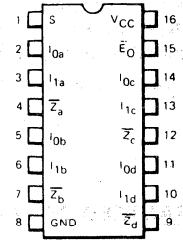
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS258A is a Quad 2-Input Multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a common Select Input (S). When the Select Input is LOW, the I_0 inputs are selected and when Select is HIGH, the I_1 inputs are selected. The data on the select inputs appears at the outputs in inverted form.

The LS258A Quad 2-Input Multiplexer is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{E}_O \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \qquad \overline{Z}_b = \overline{E}_O \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$\overline{Z}_c = \overline{E}_O \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \qquad \overline{Z}_d = \overline{E}_O \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

When the Output Enable Input ($\overline{E}_O$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{E}_O$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	(Z)
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High Impedance (Off)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS258AX	4.5 V	5.0 V	5.5 V	55°C to +125°C
SN74LS258AX	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type, W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or
		74	2.4	3.1		V	I_{OH} = −2.6 mA	V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 24 mA	V_{IL} per Truth Table
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{IH}	Input HIGH Current $\overline{E}_0$, I_{0x}, I_{1x}				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	S				40			
	Input HIGH Current at MAX Input Voltage $\overline{E}_0$, I_{0x}, I_{1x}				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
	S				0.2			
I_{IL}	Input LOW Current $\overline{E}_0$, I_{0x}, I_{1x}				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
	S				−0.8			
I_{OS}	Output Short Circuit Current (Note 4)		−30		−130	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current, Outputs HIGH				7	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 0 V	
	Power Supply Current, Outputs LOW				11	mA	V_{CC} = MAX, V_{IN} = 4.5 V, $V_{\overline{E}}$ = 0 V	
	Power Supply Current, Outputs OFF				12	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V	

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V (See SN54LS251 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output			14 14	ns	Fig. 1	C_L = 45 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Output			21 21	ns	Fig. 1	C_L = 45 pF
t_{PZH}	Output Enable Time to HIGH Level			30	ns	Figs. 4, 5	C_L = 45 pF
t_{PZL}	Output Enable Time to LOW Level			30	ns	Figs. 3, 5	R_L = 667 Ω
t_{PLZ}	Output Disable Time from LOW Level			25	ns	Figs. 3, 5	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level			30	ns	Figs. 4, 5	R_L = 667 Ω

SN54LS259/SN74LS259

8-BIT ADDRESSABLE LATCH

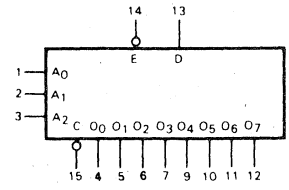
DESCRIPTION — The 54LS/74LS259 is a high-speed 8-Bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW common Clear for resetting all latches, as well as, an active LOW Enable.

- **SERIAL-TO-PARALLEL CONVERSION**
- **EIGHT BITS OF STORAGE WITH OUTPUT OF EACH BIT AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **ACTIVE HIGH DEMULTIPLEXING OR DECODING CAPABILITY**
- **EASILY EXPANDABLE**
- **COMMON CLEAR**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES		LOADING (Note a) HIGH	LOW
A_0, A_1, A_2	Address Inputs	0.5 U.L.	0.25 U.L.
D	Data Input	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
$\overline{C}$	Clear (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_0 to Q_7	Parallel Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.

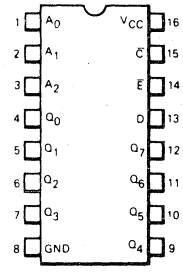
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL

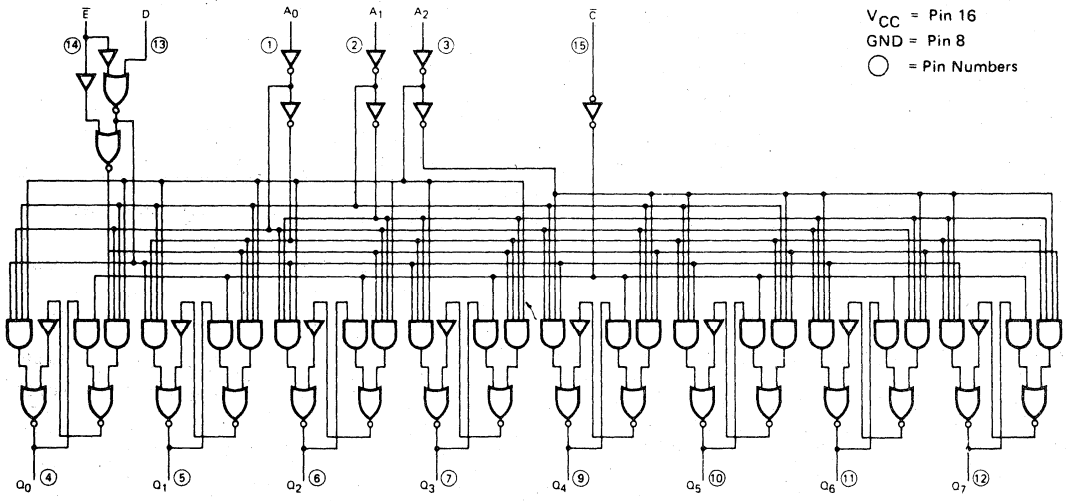


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
◯ = Pin Numbers

FUNCTIONAL DESCRIPTION — The 54LS/74LS259 has four modes of operation as shown in the mode selection table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other inputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs.

When operating the 54LS/74LS259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The truth table below summarizes the operations of the 54LS/74LS259.

MODE SELECTION

$\overline{E}$	$\overline{C}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH Eight-Channel Demultiplexer
H	L	Clear

TRUTH TABLE

						PRESENT OUTPUT STATES								
$\overline{C}$	$\overline{E}$	D	A_0	A_1	A_2	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	MODE
L	H	X	X	X	X	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1} →								Memory
H	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1} →					Addressable
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1} →						Latch
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} →						
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} →						
H	L	L	H	H	H	Q_{N-1} →						Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1} →						Q_{N-1}	H	

X = Don't Care Condition
L = LOW Voltage Level
H = HIGH Voltage Level
Q_{N-1} = Previous Output State

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS259X	4.5 V	5.0 V	5.5 V	-55°C to 125°C
SN74LS259X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1			
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH}
		74		0.35	0.5		I_{OL} = 8.0 mA; or V_{IL} per Truth Table
V_{IH}	Input HIGH Level		2.0			V	Guaranteed Input Logical HIGH Voltage for All Inputs
V_{IL}	Input LOW Level	54			0.7	V	Guaranteed Input Logical LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage				−1.5	V	V_{CC} = MIN, I_{IN} = 18 mA
I_{IL}	Input LOW Current A_0, A_1, A_2, D, C, E				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{IH}	Input HIGH Current A_1, A_2, A_3, D, C, E				20 40	μA	V_{CC} = MAX, V_{IN} = 2.4 V
I_{IH}	Input HIGH Current A_1, A_2, A_3, D, C, E				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			20	36	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operations under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
t_{PLH}	Turn-Off Delay, Enable to Output		20	27	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn-On Delay, Enable to Output		16	24	ns	Fig. 1
t_{PLH}	Turn-Off Delay, Data to Output		20	30	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn-On Delay, Data to Output		13	20	ns	Fig. 2
t_{PLH}	Turn-Off Delay, Address to Output		20	30	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn-On Delay, Address to Output		14	20	ns	Fig. 3
t_{PHL}	Turn-On Delay, Clear to Output		12	18	ns	V_{CC} = 5.0 V, C_L = 15pF Fig. 5

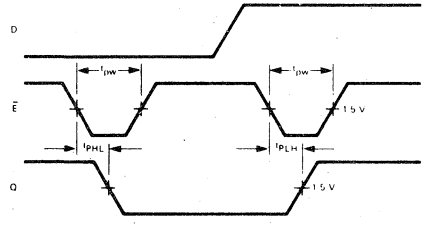
AC SET-UP REQUIREMENTS $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_s (H) t_h (H)	Set-up Time HIGH, Data to Enable Hold Time HIGH, Data to Enable	20 0	13 -7.0		ns ns	V_{CC} = 5.0 V Fig. 4
t_s (L) t_h (L)	Set-up Time LOW, Data to Enable Hold Time LOW, Data to Enable	15 0	7 10		ns ns	
t_s (A-$\overline{E}$)	Set-up Time, Address to Enable (See Note 1)	0	-7.0		ns	V_{CC} = 5.0 V Fig. 6
t_{pw} ($\overline{E}$)	Enable Pulse Width	17	12		ns	V_{CC} = 5.0 V Fig. 1

NOTES:
1. The Address to Enable Set-up Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The shaded areas indicate when the inputs are permitted to change for predictable output performance.

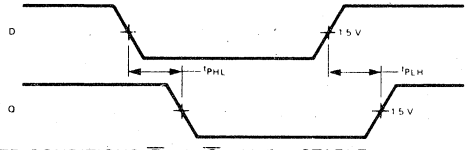
AC WAVEFORMS

Fig. 1 TURN-ON AND TURN-OFF DELAYS, ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



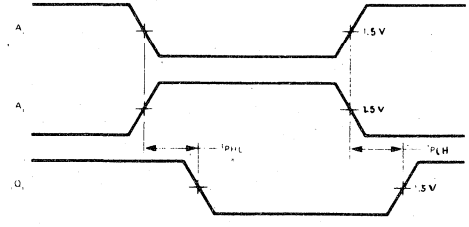
OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

Fig. 2 TURN-ON AND TURN-OFF DELAYS, DATA TO OUTPUT



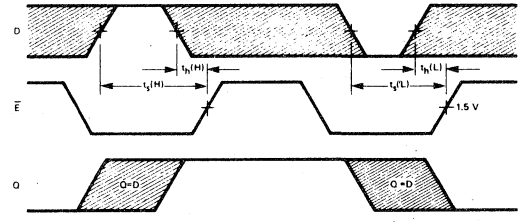
OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = H, A = STABLE

Fig. 3 TURN-ON AND TURN-OFF DELAYS, ADDRESS TO OUTPUT



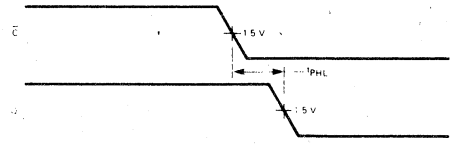
OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = L, D = H

Fig. 4 SET-UP AND HOLD TIME, DATA TO ENABLE



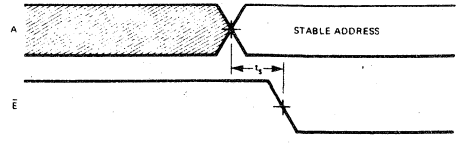
OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

Fig. 5 TURN-ON DELAY, CLEAR TO OUTPUT



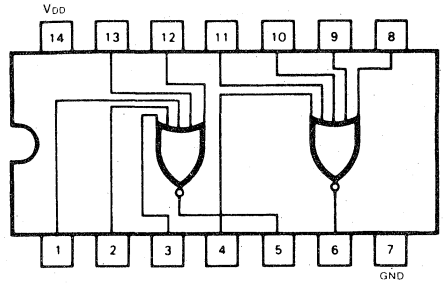
OTHER CONDITIONS: $\overline{E}$ = H

Fig. 6 SET-UP TIME, ADDRESS TO ENABLE (SEE NOTES 1 AND 2)



OTHER CONDITIONS: $\overline{C}$ = H

SN54LS260/SN74LS260
DUAL 5-INPUT NOR GATE



GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS260X	4.5 V	5.0 V	5.5 V	-55°C to +125°C
SN74LS260X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpack, J for Ceramic Dip, N for Plastic Dip

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			-0.65	-1.5	V	V_{CC} = MIN, I_{IN} = -18 mA
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4			V_{CC} = MIN, I_{OH} = -400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				-0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit		-15		-100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH				4.0	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW				5.5	mA	V_{CC} = MAX, Inputs Open

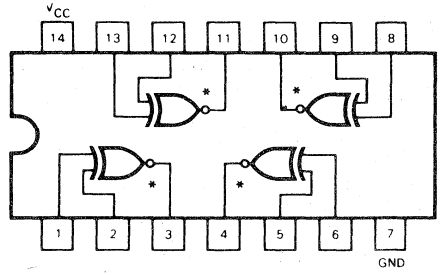
AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	3.0	5.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	6.0	12	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

SN54LS266/SN74LS266

QUAD 2-INPUT EXCLUSIVE NOR GATE



TRUTH TABLE

IN		OUT
A	B	Z
L	L	H
L	H	L
H	L	L
H	H	H

*Open Collector Outputs

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS266X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS266X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V; V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CC}	Power Supply Current			8.0	13	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, Other Input LOW			23 23	ns	V_{CC} = 5.0 V
t_{PLH} t_{PHL}	Propagation Delay, Other Input HIGH			23 23	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

SN54LS273/SN74LS273
8-BIT REGISTER WITH CLEAR

DESCRIPTION – The 54LS/74LS273 is a high-speed 8-Bit Register. The register consists of eight D-Type Flip-Flops with a Common Clock and an asynchronous active LOW Master Reset. This device is supplied in a 20-pin package featuring 0.3 inch lead spacing.

- **8-BIT HIGH SPEED REGISTER**
- **PARALLEL REGISTER**
- **COMMON CLOCK AND MASTER RESET**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
D_0-D_7	Data Inputs	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_0-Q_7	Register Outputs (Note b)	10 U.L.	5 (2.5) U.L.

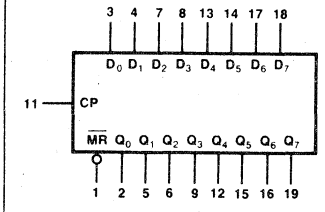
NOTES:
a. 1 TTL Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

TRUTH TABLE

$\overline{MR}$	CP	D_x	Q_x
L	X	X	L
H	↑	H	H
H	↑	L	L

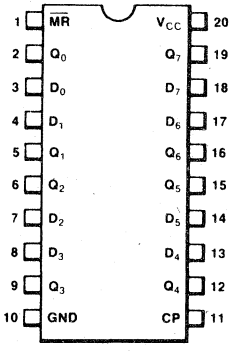
H = High Logic Level
L = Low Logic Level
X = Immaterial

LOGIC SYMBOL

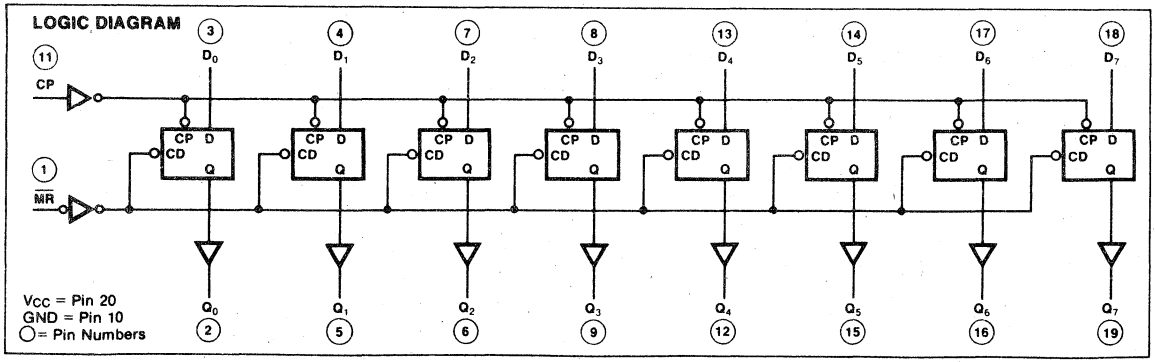


V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAM DIP (TOP VIEW)



LOGIC DIAGRAM



VCC = Pin 20
GND = Pin 10
○= Pin Numbers

FUNCTIONAL DESCRIPTION – The 54LS/74LS273 is an 8-Bit Parallel Register with a common Clock and common Master Reset.

When the $\overline{MR}$ input is LOW, the Q outputs are LOW, independent of the other inputs. Information meeting the set-up and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS273X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS273X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA; V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5		I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Input HIGH Current at MAX Input Voltage				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short-Circuit Current (Note 3)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			17	28	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operations under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

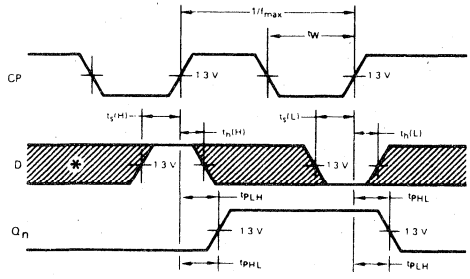
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay , Clock to Output			20 22	ns	Fig. 1
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q Output			28	ns	Fig. 2
f_{MAX}	Maximum Input Clock Frequency	30	45		MHz	Fig. 1

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_wCP	Minimum Clock Pulse Width	15	10		ns	Fig. 1
t_s	Set-up Time, Data to Clock (HIGH or LOW)	20			ns	Fig. 1
t_h	Hold Time, Data to Clock (HIGH or LOW)	5			ns	Fig. 1
t_{rec}	Recovery Time for $\overline{MR}$	15			ns	Fig. 2
$t_w\overline{MR}$	Minimum $\overline{MR}$ Pulse Width	15	8		ns	Fig. 2

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, CLOCK PULSE WIDTH, FREQUENCY, SET-UP AND HOLD TIMES DATA TO CLOCK



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME

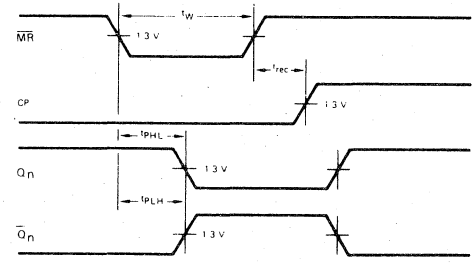


Fig. 2

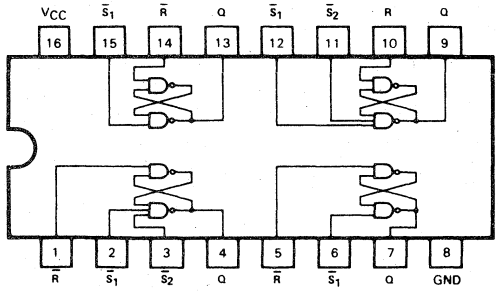
DEFINITIONS OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) – is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH Data to the Q outputs.

QUAD SET-RESET LATCH



TRUTH TABLE

INPUTS			OUTPUT
$\bar{S}_1$	$\bar{S}_2$	$\bar{R}$	(Q)
L	L	L	h
L	X	H	H
X	L	H	H
H	H	L	L
H	H	H	No Change

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
h = The output is HIGH as long as S_1 or S_2 is LOW. If all inputs go HIGH simultaneously, the output state is indeterminate; otherwise, it follows the Truth Table.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS279X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS279X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current			3.8	7.0	mA	V_{CC} = MAX

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay, $\bar{S}$ to Output			22	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}				15		
t_{PHL}	Propagation Delay, $\bar{R}$ to Output			27	ns	

SN54LS280/SN74LS280

9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

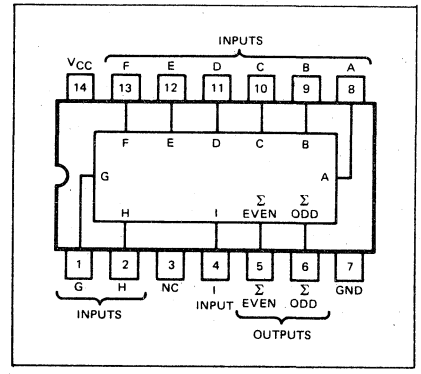
Advance Information

DESCRIPTION — These universal, 9-bit parity generators/checkers feature odd/even outputs to facilitate operation of either odd or even parity. The word length is easily expanded by cascading.

This device can be used to upgrade the performance of most systems utilizing the LS180 parity generator/checker. Although the LS280 is implemented without expander inputs, the corresponding function is provided by an input at pin 4 and the absence of any connection at pin 3. This permits the LS280 to be substituted for the LS180 to produce an identical function even if LS280's are mixed with LS180's.

These devices are fully compatible with most other TTL and DTL circuits. All LS280 inputs are buffered to lower the drive requirements to one LS unit load.

(TOP VIEW)



NC - No internal connection.

- **GENERATES EITHER ODD OR EVEN PARITY FOR NINE DATA LINES**
- **TYPICAL DATA-TO-OUTPUT DELAY OF ONLY 33 ns**
- **CASCADABLE FOR n-BITS**
- **CAN BE USED TO UPGRADE SYSTEMS USING MSI PARITY CIRCUITS**
- **TYPICAL POWER DISSIPATION = 80 mW**

FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = high level, L = low level

This is advance information and specifications are subject to change without notice.

SN54LS283/SN74LS283

4-BIT BINARY FULL ADDER WITH FAST CARRY

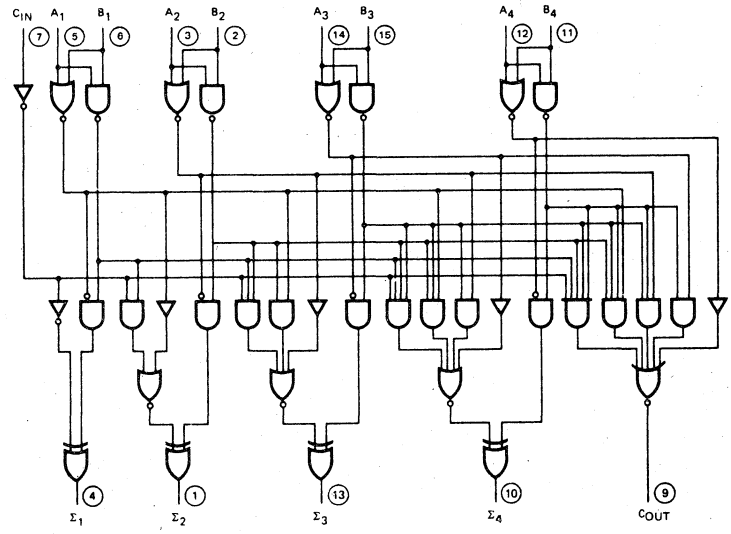
DESCRIPTION — The SN54LS283/SN74LS283 is a high-speed 4-Bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words ($A_1 - A_4$, $B_1 - B_4$) and a Carry Input (C_{IN}). It generates the binary Sum outputs ($\Sigma_1 - \Sigma_4$) and the Carry Output (C_{OUT}) from the most significant bit. The LS283 operates with either active HIGH or active LOW operands (positive or negative logic).

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$A_1 - A_4$	Operand A Inputs	1.0 U.L.	0.5 U.L.
$B_1 - B_4$	Operand B Inputs	1.0 U.L.	0.5 U.L.
C_{IN}	Carry Input	0.5 U.L.	0.25 U.L.
$\Sigma_1 - \Sigma_4$	Sum Outputs (Note b)	10 U.L.	5(2.5) U.L.
C_{OUT}	Carry Output (Note b)	10 U.L.	5(2.5) U.L.

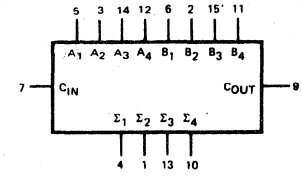
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for commercial (74) Temperature Ranges.

LOGIC DIAGRAM



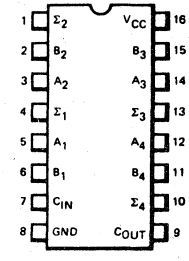
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS283 adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs ($\Sigma_1 - \Sigma_4$) and outgoing carry (C_{OUT}) outputs.

$$C_{IN}+(A_1+B_1)+2(A_2+B_2)+4(A_3+B_3)+8(A_4+B_4) = \Sigma_1+2\Sigma_2+4\Sigma_3+8\Sigma_4+16C_{OUT}$$

Where: (+) = plus

Due to the symmetry of the binary add function the LS283 can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH inputs, Carry In can not be left open, but must be held LOW when no carry in is intended.

Example:

	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}	
logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10+9=19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry+5+6=12)

Interchanging inputs of equal weight does not affect the operation, thus C_{IN}, A_1, B_1, can be arbitrarity assigned to pins 7, 5 or 3.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS283X	4.5 V	5.0 V	5.5 V	–55°C to +125°C
SN74LS283X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type: W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current C_{IN} Any A or B				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	C_{IN} Any A or B				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current C_{IN} Any A or B				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			22	39	mA	V_{CC} = MAX, All Inputs = 0 V
				19	34	mA	V_{CC} = MAX, A Inputs = 4.5 V

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, C_{IN} Input to Any Σ Output			24 24	ns	V_{CC} = 5.0 V C_L = 15 pF Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to Σ Outputs			24 24	ns	
t_{PLH} t_{PHL}	Propagation Delay, C_{IN} Input to C_{OUT} Output			17 17	ns	
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to C_{OUT} Output			17 17	ns	

AC WAVEFORMS

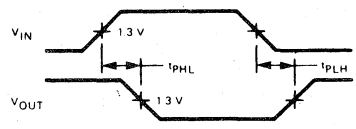


Fig. 1

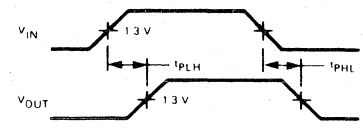


Fig. 2

Advance Information

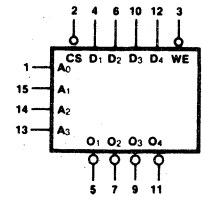
SN54LS289/SN74LS289

64-BIT RANDOM ACCESS MEMORY WITH OPEN COLLECTOR OUTPUTS

DESCRIPTION – The 54LS/74LS289 is a high-speed, low-power 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading, and addresses are fully decoded on-chip. Outputs are open-collector type and are in the off (HIGH) state whenever the Chip Select (CS) input is HIGH. The outputs are active only in the Read mode; output data is the complement of the stored data.

- **OPEN COLLECTOR OUTPUTS FOR WIRED-AND APPLICATIONS**
- **BUFFERED INPUTS MINIMIZE LOADING**
- **ADDRESS DECODING ON-CHIP**
- **DIODE CLAMPED INPUTS MINIMIZE RINGING**
- **LOW POWER SCHOTTKY DESIGN MINIMIZES POWER CONSUMPTION**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

A_n	Address Input
$\overline{CS}$	Chip Select (Active LOW) Input
D_n	Data Input
O_n	Data (Inverted) Output
$\overline{WE}$	Write Enable (Active LOW) Input

FUNCTION TABLE

INPUTS $\overline{CS}$	INPUTS $\overline{WE}$	OPERATION	CONDITION OF OUTPUTS
L	L	Write	Off (HIGH)
L	H	Read	Complement of Stored Data
H	X	Inhibit	Off (HIGH)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

SN54LS290/SN74LS290

DECADE COUNTER

SN54LS293/SN74LS293

4-BIT BINARY COUNTER

DESCRIPTION – The SN54LS290/SN74LS290 and SN54LS293/SN74LS293 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS290) or divide-by-eight (LS293) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to $\overline{CP}$) to form BCD, Bi-quinary, or Modulo-16 counters. Both of the counters have a 2-input gated Master Reset (Clear), and the LS290 also has a 2-input gated Master Set (Preset 9).

- **CORNER POWER PIN VERSIONS OF THE LS90 and LS93**
- **LOW POWER CONSUMPTION .... TYPICALLY 45 mW**
- **HIGH COUNT RATES .... TYPICALLY 50 MHz**
- **CHOICE OF COUNTING MODES .... BCD, BI-QUINARY, BINARY**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$\overline{CP}_0$	Clock (Active LOW going edge) Input to ÷2 Section.	3.0 U.L.	1.5 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷5 Section (LS290).	2.0 U.L.	2.0 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷ 8 Section (LS293).	1.0 U.L.	1.0 U.L.
MR_1, MR_2	Master Reset (Clear) Inputs	0.5 U.L.	0.25 U.L.
MS_1, MS_2	Master Set (Preset-9, LS290) Inputs	0.5 U.L.	0.25 U.L.
Q_0	Output from ÷2 Section (Notes b & c)	10 U.L.	5(2.5) U.L.
Q_1, Q_2, Q_3	Outputs from ÷5 & ÷8 Sections (Note b)	10 U.L.	5(2.5) U.L.

NOTES:

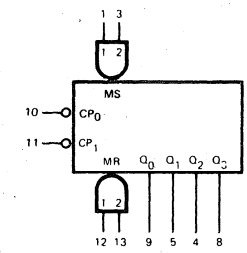
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

c. The Q_0 Outputs are guaranteed to drive the full fan-out plus the $\overline{CP}_1$ Input of the device.

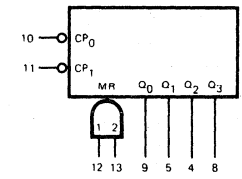
LOGIC SYMBOL

LS290



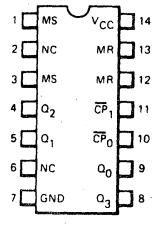
V_{CC} = Pin 14
GND = Pin 7
NC = Pins 2, 6

LS293



V_{CC} = Pin 14
GND = Pin 7
NC = Pins 1, 2, 3, 6

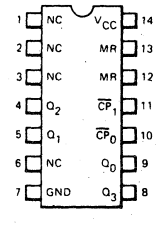
CONNECTION DIAGRAM **LS290**
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

NC – No Internal Connection

CONNECTION DIAGRAM **LS293**
DIP (TOP VIEW)

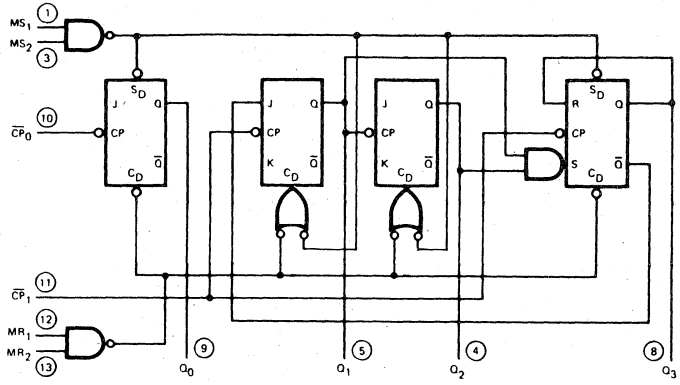


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

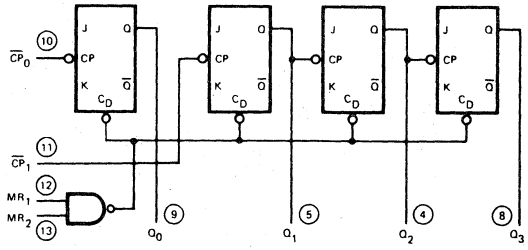
NC – No internal connection

LOGIC DIAGRAMS

LS290



LS293



FUNCTIONAL DESCRIPTION – The LS290 and LS293 are 4-bit ripple type Decade, and 4-Bit Binary counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS290) or divide-by-eight (LS293) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided on both counters which overrides the clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) is provided on the LS290 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes:

LS290

A. BCD Decade (8421) Counter – the $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Bi-quinary Divide-By-Ten Counter – The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output Q_0.

C. Divide-By-Two and Divide-By-Five Counter – No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain binary divide-by-five operation at the Q_3 output.

LS293

A. 4-Bit Ripple Counter – The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous division of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the truth table.

B. 3-Bit Ripple Counter – The input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1, Q_2, and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

LS290 MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

LS293 MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

LS290
BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to Input CP_1 for BCD count.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note: Output Q_0 connected to input CP_1.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
SN54LS290X SN54LS293X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS290X SN74LS293X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA; V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current MS, MR				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	$\overline{CP}_0$				20		
	$\overline{CP}_1$ (LS290)				20		
	$\overline{CP}_1$ (LS293)				20		
	MS, MR				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
	$\overline{CP}_0$, $\overline{CP}_1$ (LS293)				0.1		V_{CC} = MAX, V_{IN} = 5.5 V
	$\overline{CP}_1$ (LS290)				0.1		V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current MS, MR				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	$\overline{CP}_0$				−2.4		
	$\overline{CP}_1$ (LS290)				−3.2		
	$\overline{CP}_1$ (LS293)				−1.6		
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			9	15	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS				UNITS	TEST CONDITIONS	
		LS290		LS293				
		MIN	MAX	MIN	MAX			
f_{MAX}	$\overline{CP}_0$ Input Count Frequency	32		32		MHz	Fig. 1	
f_{MAX}	$\overline{CP}_1$ Input Count Frequency	16		16		MHz	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_0 Output		16 18		16 18	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_1$ Input to Q_1 Output		16 21		16 21	ns		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_1$ Input to Q_2 Output		32 35		32 35	ns		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_1$ Input to Q_3 Output		32 35		51 51	ns		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_3 Output		48 50		70 70	ns		
t_{PLH}	MS Input to Q_0 and Q_3 Outputs		30			ns	Fig. 3	
t_{PHL}	MS Input to Q_1 and Q_2Outputs		40			ns	Fig. 2	
t_{PHL}	MR Input to Any Output		40		40	ns	Fig. 2	

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS				UNITS	TEST CONDITIONS	
		LS290		LS293				
		MIN	MAX	MIN	MAX			
t_W	$\overline{CP}_0$ Pulse Width	15		15		ns	Fig. 1	V_{CC} = 5.0 V
t_W	$\overline{CP}_1$ Pulse Width	30		30		ns		
t_W	MS Pulse Width	15				ns	Fig. 2, 3	
t_W	MR Pulse Width	15		15		ns	Fig. 2	
t_{rec}	Recovery Time MS to $\overline{CP}$	25				ns	Fig. 2, 3	
t_{rec}	Recovery Time MR to $\overline{CP}$	25		25		ns	Fig. 2	

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

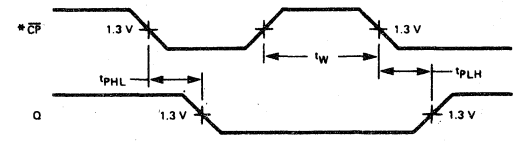


Fig. 1

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.

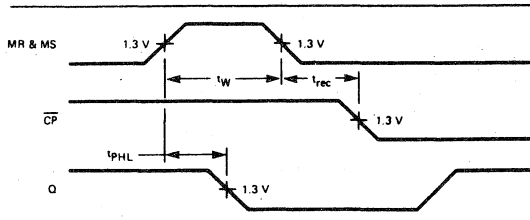


Fig. 2

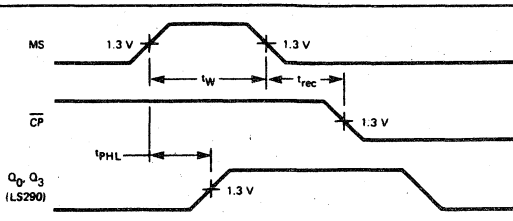


Fig. 3

SN54LS295A/SN74LS295A

4-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

DESCRIPTION — The SN54LS295A/SN74LS295A is a 4-Bit Shift Register with serial and parallel synchronous operating modes, and independent 3-state output buffers. The Parallel Enable input (PE) controls the shift-right or parallel load operation. All data transfers and shifting occur synchronous with the HIGH to LOW clock transition.

The 3-State output buffers are controlled by an active HIGH Output Enable input (EO). Disabling the output buffers does not affect the shifting or loading of input data, but it does inhibit serial expansion.

The LS295 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

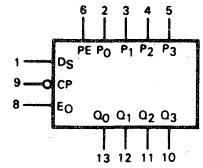
- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**
- **NEGATIVE EDGE-TRIGGERED CLOCK INPUT**
- **PARALLEL ENABLE MODE CONTROL INPUT**
- **3-STATE BUSSABLE OUTPUT BUFFERS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
PE	Parallel Enable Input	0.5 U.L.	0.25 U.L.
D_S	Serial Data Input	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	Parallel Data Input	0.5 U.L.	0.25 U.L.
E_O	Output Enable Input	0.5 U.L.	0.25 U.L.
$\overline{CP}$	Clock Pulse (Active LOW Going Edge) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	3-State Outputs (Note b)	65(25) U.L.	5(2.5) U.L.

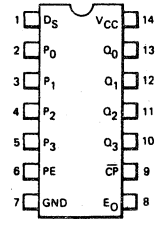
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



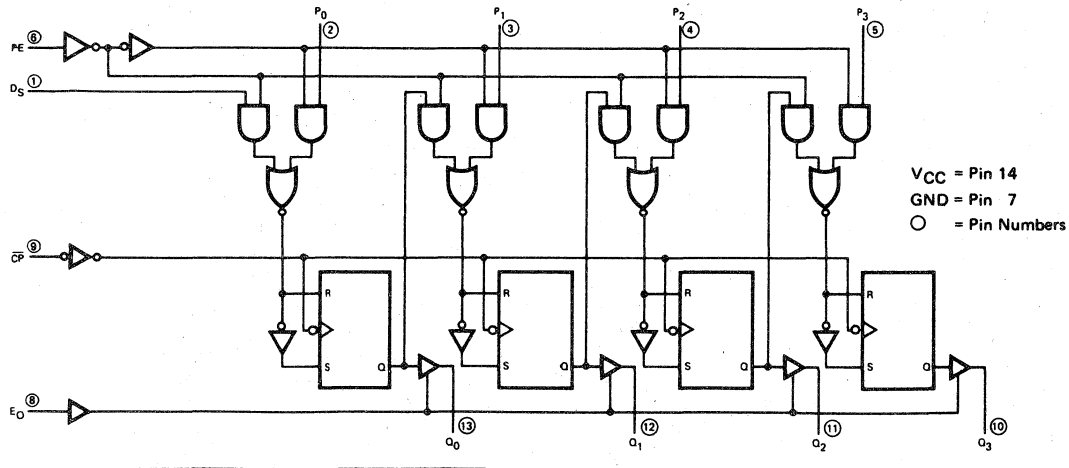
V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION – The LS295 is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial Data (D_S) and four Parallel Data ($P_0 - P_3$) inputs and four parallel 3-State output buffers ($Q_0 - Q_3$). When the Parallel Enable (PE) input is HIGH, data is transferred from the Parallel Data Inputs ($P_0 - P_3$) into the register synchronous with the HIGH to LOW transition of the Clock ($\overline{CP}$). When the PE is LOW, a HIGH to LOW transition on the clock transfers the serial data on the D_S input to register Q_0, and shifts data from Q_0 to Q_1, Q_1 to Q_2 and Q_2 to Q_3. The input data and parallel enable are fully edge-triggered and must be stable only one set-up time before the HIGH to LOW clock transition.

The 3-State output buffers are controlled by an active HIGH Output Enable input (E_O). When the E_O is HIGH, the four register outputs appear at the $Q_0 - Q_3$ outputs. When E_O is LOW, the outputs are forced to a high impedance "off" state. The 3-State output buffers are completely independent of the register operation, i.e., the input transitions on the E_O input do not affect the serial or parallel data transfers of the register. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-State devices whose outputs are tied together are designed so there is no overlap.

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS*			
	PE	$\overline{CP}$	D_S	P_n	Q_0	Q_1	Q_2	Q_3
Shift Right	l	⎍	l	X	L	q_0	q_1	q_2
	l	⎍	h	X	H	q_0	q_1	q_2
Parallel Load	h	⎍	X	p_n	p_0	p_1	p_2	p_3

*The indicated data appears at the Q outputs when E_O is HIGH. When E_O is LOW, the indicated data is loaded into the register, but the outputs are all forced to the high impedance "off" state.

L = LOW Voltage Levels
H = HIGH Voltage Levels
X = Don't Care

$p_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

l = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.

h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS295AX	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS295AX	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	I_{OH} = −1.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.4			I_{OH} = −2.6 mA
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2.0 V
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 2.0 V
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current, Outputs HIGH			14	23	mA	V_{CC} = MAX, V_{CP} = ⎍, V_E = 4.5 V
	Power Supply Current, Outputs Off			15	25	mA	V_{CC} = MAX, V_{CP} = 0 V, V_E = 0 V

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Shift Frequency	30	45		MHz	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH}	Propagation Delay, Clock to Output		24	30	ns	Fig. 1	
t_{PHL}			16	26			

AC CHARACTERISTICS: for 3-State Output Buffers (See Page 5-98 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PZH}	Output Enable Time to HIGH Level		12	18	ns	Figs. 4, 5	C_L = 15 pF
t_{PZL}	Output Enable Time to LOW Level		14	20	ns	Figs. 3, 5	R_L = 2 kΩ
t_{PLZ}	Output Disable Time from LOW Level		17	24	ns	Figs. 3, 5	C_L = 5 pF
t_{PHZ}	Output Disable Time from HIGH Level		15	20	ns	Figs. 4, 5	R_L = 2 kΩ

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_W(CP)	Clock Pulse Width	20	7		ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_s(Data)	Set-up Time, Data to Clock	20	7		ns	Fig. 1	
t_h(Data)	Hold Time, Data to Clock	10	2		ns		
t_s(PE)	Set-up Time, PE to Clock	20	7		ns	Fig. 2	
t_h(PE)	Hold Time, PE to Clock	0			ns		

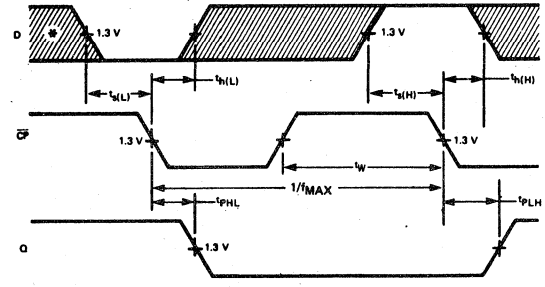
DEFINITION OF TERMS

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



*The Data Input is D_S for PE = LOW and P_n for PE = HIGH.

Fig. 1

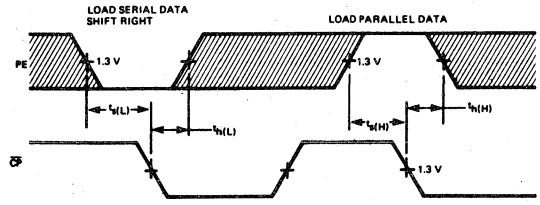


Fig. 2

SN54LS298/SN74LS298

QUAD 2-PORT REGISTER
(QUAD 2-INPUT MULTIPLEXER WITH STORAGE)

DESCRIPTION – The SN54LS298/SN74LS298 is a Quad 2-Port Register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register synchronous with the HIGH to LOW transition of the Clock input.

The LS298 is fabricated with the Schottky barrier process for high speed and is completely compatible with all Motorola TTL families.

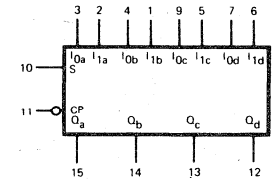
- SELECT FROM TWO DATA SOURCES
- FULLY EDGE-TRIGGERED OPERATION
- TYPICAL POWER DISSIPATION OF 65 mW
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

		LOADING (Note a) HIGH	LOW
S	Common Select Input	0.5 U.L.	0.25 U.L.
$\overline{CP}$	Clock (Active LOW Going Edge) Input	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{0d}$	Data Inputs From Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs From Source 1	0.5 U.L.	0.25 U.L.
$Q_a - Q_d$	Register Outputs (Note b)	10 U.L.	5(2.5) U.L.

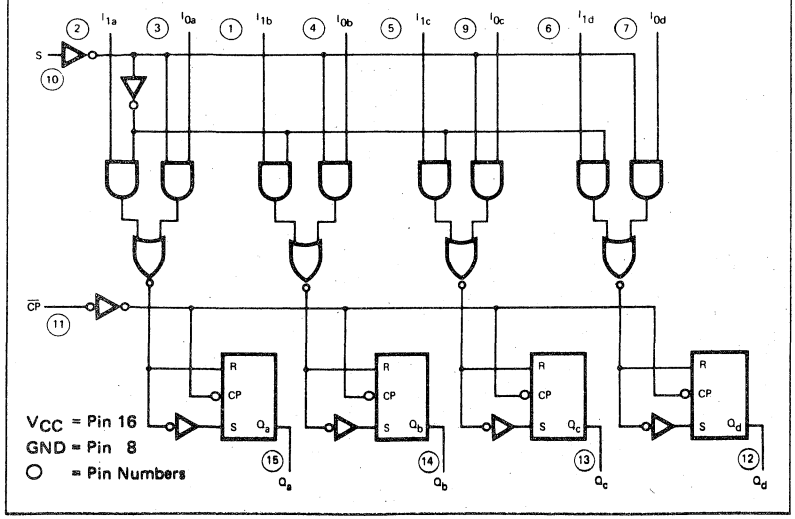
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL

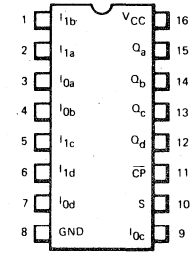


V_{CC} = Pin 16
GND = Pin 8

LOGIC OR BLOCK DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS298 is a high speed Quad 2-Port Register. It selects four bits of data from two sources (ports) under the control of a Common Select Input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH to LOW transition of the Clock input ($\overline{CP}$). The 4-bit output register is fully edge-triggered. The Data inputs (I) and Select input (S) must be stable only one set-up time prior to the HIGH to LOW transition of the clock for predictable operation.

TRUTH TABLE

INPUTS			OUTPUT
S	I_0	I_1	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
l = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.
h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS298X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS298X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			13	21	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		16 16	25 25	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
$t_{W(H)}$	Clock Pulse Width (HIGH)	20	11		ns	Fig. 1	V_{CC} = 5.0 V
$t_{W(L)}$	Clock Pulse Width (LOW)	20	11		ns		
$t_{s(Data)}$	Set-up Time, Data to Clock	15	10		ns	Fig. 1	
$t_{h(Data)}$	Hold Time, Data to Clock	5.0	1		ns		
$t_{s(S)}$	Set-up Time, Select to Clock	20	20		ns	Fig. 2	
$t_{h(S)}$	Hold Time, Select to Clock	0	−2.0		ns		

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

AC WAVEFORMS

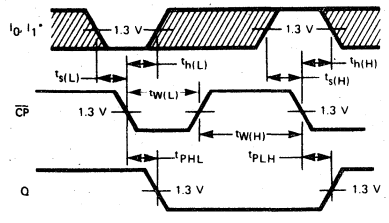


Fig. 1

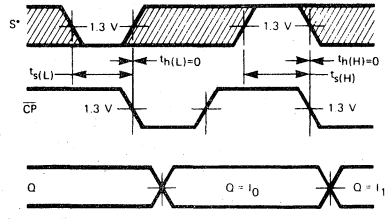


Fig. 2

*The shaded areas indicate when the input is permitted to change for predictable output performance.

SN54LS299/SN74LS299

8-BIT UNIVERSAL SHIFT/STORAGE REGISTER WITH COMMON PARALLEL I/O PINS

Advance Information

DESCRIPTION — The 54LS/74LS299 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data.

The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q_0 and Q_7 to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

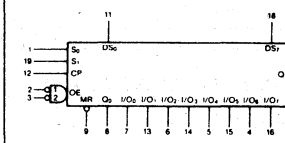
- **COMMON I/O FOR REDUCED PIN COUNT**
- **FOUR OPERATION MODES: SHIFT LEFT, SHIFT RIGHT, LOAD AND STORE**
- **SEPARATE SHIFT RIGHT SERIAL INPUT AND SHIFT LEFT SERIAL INPUT FOR EASY CASCADING**
- **3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
CP	Clock Pulse (active positive-going edge) Input	0.5 U.L.	0.25 U.L.
DS_0	Serial Data Input for Right Shift	0.5 U.L.	0.25 U.L.
DS_7	Serial Data Input for Left Shift	0.5 U.L.	0.25 U.L.
I/O_n	Parallel Data Input or Parallel Output (3-State) (Note c)	0.5 U.L. 65(25) U.L.	0.25 U.L. 15(7.5) U.L.
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable (active LOW) Inputs	0.5 U.L.	0.25 U.L.
Q_0, Q_7	Serial Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{MR}$	Asynchronous Master Reset (active LOW) Input	0.5 U.L.	0.25 U.L.
S_0, S_1	Mode Select Inputs	1 U.L.	0.5 U.L.

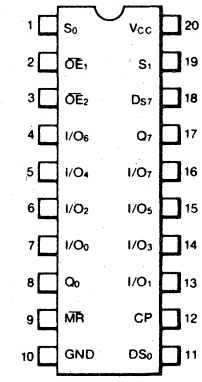
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.
c. The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74), the Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



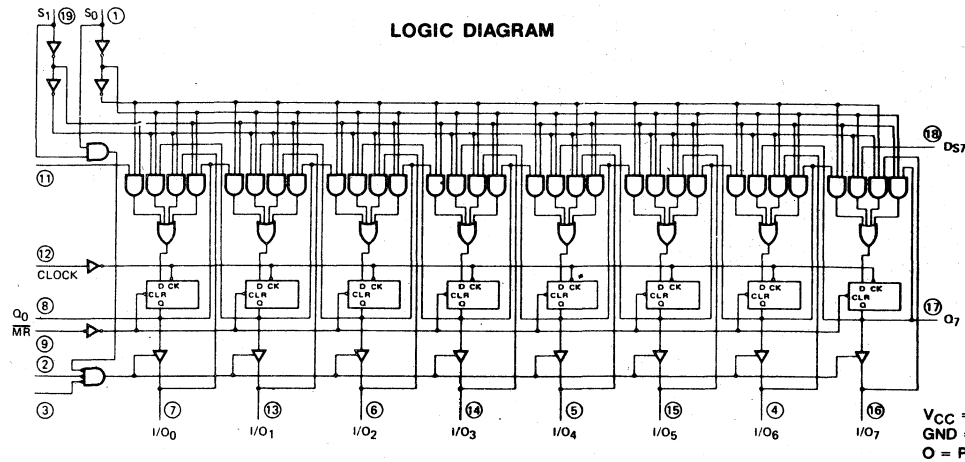
V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10
O = Pin Numbers

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS299X	4.5 V	5.0 V	5.5 V	-55°C to +125°C
SN74LS299X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			-0.65	-1.5	V	V_{CC} = MIN, I_{IN} = -18 mA
V_{OH}	Output HIGH Voltage Q_0, Q_7	54	2.4	3.4		V	I_{OH} = -400 μA V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1		V	
V_{OH}	Output HIGH Voltage I/O_0 thru I/O_7	54	2.4	3.4		V	I_{OH} = -1.0 mA V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1		V	I_{OH} = -2.6 mA
V_{OL}	Output LOW Voltage Q_0, Q_7	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
V_{OL}	Output LOW Voltage I/O_0 thru I/O_7	54, 74		0.25	0.4	V	I_{OL} = 12.0 mA V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24.0 mA
I_{OZH}	Output Off Current HIGH				40	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, $\overline{V_E}$ = 2.0 V
I_{OZL}	Output Off Current LOW				-400	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $\overline{V_E}$ = 2.0 V
I_{IH}	Input HIGH Current All inputs except S_0, S_1				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	S_0, S_1				40		
	Input HIGH Current at MAX Input Voltage All inputs except S_0, S_1				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
	S_0, S_1				0.2		
I_{IL}	Input LOW Current All inputs except S_0, S_1				-0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	S_0, S_1				-0.8		
I_{OS}	Output Short Circuit Current (Note 4)	I/O_0 thru I/O_7	-30		-130	mA	V_{CC} = MAX, V_{OUT} = 0 V
		Q_0, Q_7	-20		-100		
I_{CC}	Power Supply Current			35	60	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operations under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

FUNCTION TABLE

INPUTS								RESPONSE
$\overline{MR}$	S_1	S_0	$\overline{OE}_1$	$\overline{OE}_2$	CP	DS_0	DS_7	
L	X	X	H	X	X	X	X	Asynchronous Reset; $Q_0 = Q_7$ = LOW I/O Voltage Undetermined
L	X	X	X	H	X	X	X	
L	H	H	X	X	X	X	X	
L	L	X	L	L	X	X	X	Asynchronous Reset; $Q_0 = Q_7$ = LOW I/O Voltage LOW
L	X	L	L	L	X	X	X	
X	L	H	X	X	⌐	D	X	Shift Right; $D \rightarrow Q_0$; $Q_0 \rightarrow Q_1$; etc.
H	L	H	L	L	⌐	D	X	Shift Right; $D \rightarrow Q_0$ & I/O_0; $Q_0 \rightarrow Q_1$ & I/O_1; etc.
H	H	L	X	X	⌐	X	D	Shift Left; $D \rightarrow Q_7$; $Q_7 \rightarrow Q_6$; etc.
H	H	L	L	L	⌐	X	D	Shift Left; $D \rightarrow Q_7$ & I/O_7; $Q_7 \rightarrow Q_6$ & I/O_6; etc.
H	H	H	X	X	⌐	X	X	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	L	H	X	X	X	X	Hold: I/O Voltage undetermined
H	L	L	X	H	X	X	X	
H	L	L	L	L	X	X	X	Hold: $I/O_n = Q_n$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_wH (CP)	Minimum Clock Pulse Width HIGH	20			ns	
t_wL (CP)	Minimum Clock Pulse Width LOW	20			ns	
t_wL (MR)	Minimum Master Reset Pulse Width LOW	20			ns	
t_s	Set-up Time, S_0 or S_1 to CP	10			ns	
t_h	Hold Time, S_0 or S_1 to CP	10			ns	
t_s (H)	Set-up Time I/O_0 thru I/O_7, DS_0, DS_7 to CP (HIGH)	20			ns	
t_s (L)	Set-up Time I/O_0 thru I/O_7, DS_0, DS_7 to CP (LOW)	20			ns	
t_h	Hold Time (HIGH or LOW) I/O_0 thru I/O_7, DS_0, DS_7 to CP	0			ns	
t_{rec}	Master Reset Recovery Time	20			ns	

DEFINITION OF TERMS:

SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	**Maximum Input Frequency**	35	50		MHz	V_{CC} = 5.0 V
t_{PHL} t_{PLH}	**Propagation Delay, Clock** To Q_0 or Q_7			25 25	ns	C_L = 15 pF
t_{PHL} t_{PLH}	**Propagation Delay, Clock** To I/O_0 thru I/O_7			25 25	ns	
t_{PHL} t_{PHL}	Master Reset To Q_0 or Q_7 Master Reset To I/O_0 thru I/O_7			35 35	ns	
t_{PZH} t_{PZL}	Output Enable Time			35 35	ns	C_L = 5 pF R_L = 667 Ω
t_{PHZ} t_{PLZ}	Output Disable Time			25 25	ns	V_{CC} = 5.0 V

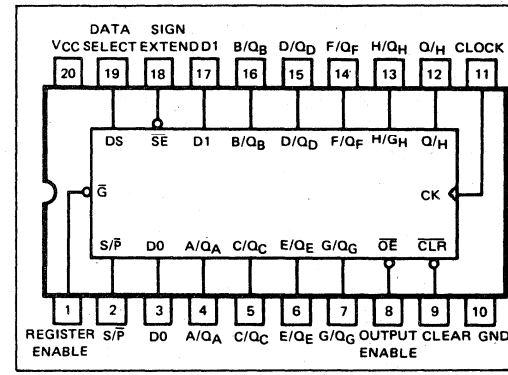
SN54LS322/SN74LS322

8-BIT SHIFT REGISTERS WITH SIGN EXTEND

Advance Information

DESCRIPTION — These 8-bit shift registers have multiplexed input/output data ports to accomplish full 8-bit data handling in a single 20-pin package. Serial data may enter the shift-right register through either D0 or D1 inputs as selected by the data select pin. A serial output is also provided. Synchronous parallel loading is achieved by taking the register enable and the S/$\overline{P}$ inputs low. This places the three-state input/output ports in the data input mode. Data is entered on the low-to-high clock transition. The data extend function repeats the sign in the Q_A flip-flop during shifting. An overriding clear input clears the internal registers when taken low whether the outputs are enabled or off. The output enable does not affect synchronous operation of the register.

(TOP VIEW)



- **MULTIPLEXED INPUTS/OUTPUTS PROVIDE IMPROVED BIT DENSITY**
- **SIGN EXTEND FUNCTION**
- **DIRECT OVERRIDING CLEAR**
- **3-STATE OUTPUTS DRIVE BUS LINES DIRECTLY**

FUNCTION TABLE

OPERATION	INPUTS							INPUTS/OUTPUTS				OUTPUT
	CLEAR	REGISTER ENABLE	S/$\overline{P}$	SIGN EXTEND	DATA SELECT	OUTPUT ENABLE	CLOCK	A/Q_A	B/Q_B	C/Q_C ...	H/Q_H	$Q_{H'}$
Clear	L	H	X	X	X	L	X	L	L	L	L	L
	L	X	H	X	X	L	X	L	L	L	L	L
Hold	H	H	X	X	X	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{H0}	Q_{H0}
Shift Right	H	L	H	H	L	L	↑	D0	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Gn}
	H	L	H	H	H	L	↑	D1	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Gn}
Sign Extend	H	L	H	L	X	L	↑	Q_{An}	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Gn}
Load	H	L	L	X	X	X	↑	a	b	c	h	h

When the output enable is high, the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected. If both the register enable input and the S/$\overline{P}$ input are low while the clear input is low, the register is cleared while the eight input/output terminals are disabled to the high-impedance state.

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
Q_{A0} . . . Q_{H0} = the level of Q_A through Q_H, respectively, before the indicated steady-state conditions were established
Q_{An} . . . Q_{Hn} = the level of Q_A through Q_H, respectively, before the most recent ↑ transition of the clock
D0, D1 = the level of steady-state inputs at inputs D0 and D1 respectively
a . . . h = the level of steady-state inputs at inputs A through H respectively

This is advance information and specifications are subject to change without notice.

SN54LS323/SN74LS323

8-BIT UNIVERSAL SHIFT/STORAGE REGISTER WITH SYNCHRONOUS RESET AND COMMON I/O PINS

Advance Information

DESCRIPTION—The 54LS/74LS323 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Its function is similar to the 54LS/74LS299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate inputs and outputs are provided for flip-flops Q_0 and Q_7 to allow easy cascading.

Four operation modes are possible: hold (store), shift left, shift right, and parallel load. All modes are activated on the LOW-to-HIGH transition of the Clock.

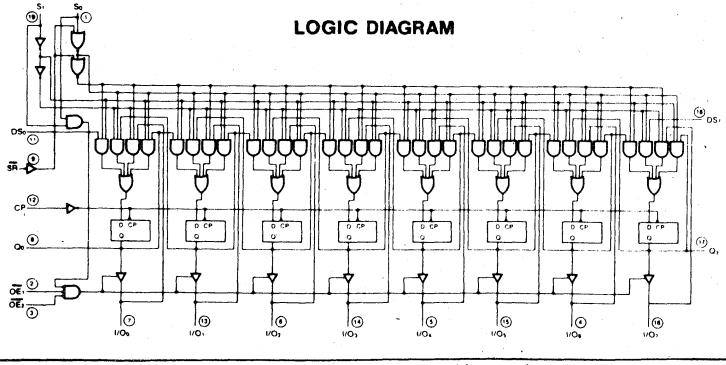
- **COMMON I/O FOR REDUCED PIN COUNT**
- **FOUR OPERATION MODES: SHIFT LEFT, SHIFT RIGHT, PARALLEL LOAD AND STORE**
- **SEPARATE CONTINUOUS INPUTS AND OUTPUTS FROM Q_0 AND Q_7 ALLOW EASY CASCADING**
- **FULLY SYNCHRONOUS RESET**
- **3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATIBLE**

PIN NAMES

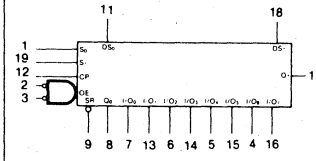
		LOADING (Note a) HIGH	LOW
CP	Clock Pulse (active positive-going edge) Input	0.5 U.L.	0.25 U.L.
DS_0	Serial Data Input For Right Shift	0.5 U.L.	0.25 U.L.
DS_7	Serial Data Input For Left Shift	0.5 U.L.	0.25 U.L.
I/O_n	Parallel Data Input or	1.0 U.L.	0.5 U.L.
	Parallel Output (3-State) (Note c)	65(25) U.L.	15(7.5) U.L.
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable (active LOW) Inputs	0.5 U.L.	0.25 U.L.
Q_0, Q_7	Serial Outputs (Note b)	10 U.L.	5(2.5) U.L.
S_0, S_1	Mode Select Inputs	1 U.L.	
$\overline{SR}$	Synchronous Reset (active LOW) Input	0.5 U.L.	0.25 U.L.

NOTES:
a. 1 TTL LOAD = 40 μA HIGH/1.6 mA LOW.
b. The output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial Temperature Ranges.
c. The output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial Temperature Ranges.
The output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial Temperature Ranges.

LOGIC DIAGRAM

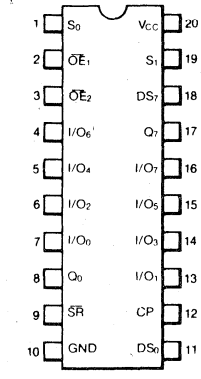


LOGIC SYMBOL



V_{CC} = 20
GND = 10

CONNECTION DIAGRAM
DIP (TOP VIEW)
54LS/74LS323



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION The logic diagram and truth table indicate the functional characteristics of the 54LS/75LS323 Universal Shift/Storage Register. This device is similar in operation to the 54LS/74LS299 except for synchronous reset. A partial list of the common features are described below:

1. They use eight D-type edge-triggered flip-flops that respond only to the LOW-to-HIGH transition of the Clock (CP). The only timing restriction, therefore, is that the mode control (S_0, S_1) and data inputs (DS_0, DS_7, I/O_0-I/O_7) be stable at least a set-up time prior to the positive transition of the Clock Pulse.

2. When $S_0 = S_1 = 1$, I/O_0-I/O_7 are parallel inputs to flip-flops Q_0-Q_7 respectively, and the outputs of Q_0-Q_7 are in the high impedence state regardless of the state of $\overline{OE}_1$ or $\overline{OE}_2$.

An important unique feature of the 54LS/74LS323 is a fully Synchronous Reset that requires only to be stable at least one set-up time prior to the positive transition of the Clock Pulse.

TRUTH TABLE

INPUTS								RESPONSE
$\overline{SR}$	S_1	S_0	$\overline{OE}_1$	$\overline{OE}_2$	CP	DS_0	DS_7	
L	X	X	H	X	⎍	X	X	Synchronous Reset, $Q_0 = Q_7$ = LOW
L	X	X	X	H	⎍	X	X	I/O voltage undetermined
L	H	H	X	X	⎍	X	X	
L	L	X	L	L	⎍	X	X	Synchronous Reset; $Q_0 = Q_7$ = LOW
L	X	L	L	L	⎍	X	X	I/O voltage LOW
H	L	H	X	X	⎍	D	X	Shift Right; $D \rightarrow Q_0$; $Q_0 \rightarrow Q_1$; etc.
H	L	H	L	L	⎍	D	X	Shift Right; $D \rightarrow Q_0$ & I/O_0; $Q_0 \rightarrow Q_1$ & I/O_1; etc.
H	H	L	X	X	⎍	X	D	Shift Left; $D \rightarrow Q_7$; $Q_7 \rightarrow Q_6$; etc.
H	H	L	L	L	⎍	X	D	Shift Left; $D \rightarrow Q_7$ & I/O_7; $Q_7 \rightarrow Q_6$ & I/O_6; etc.
H	H	H	X	X	⎍	X	X	Parallel Load $I/O_n \rightarrow Q_n$
H	L	L	H	X	X	X	X	Hold; I/O Voltage Undetermined
H	L	L	X	H	X	X	X	
H	L	L	L	L	X	X	X	Hold; $I/O_n = Q_n$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS323X	4.5 V	5.0 V	5.5 V	-55°C to +125°C
SN74LS323X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f_{MAX}	Maximum input frequency	35	50		MHz	V_{CC} = 5.0 V
t_{PHL} t_{PLH}	**Propagation Delay, CP** To Q_0 or Q_7			25 25	ns	C_L = 15 pF
t_{PLH} t_{PLH}	**Propagation Delay, CP** To I/O_0 thru I/O_7			25 25	ns	
t_{PZH} t_{PZL}	Output Enable Time			35 35	ns	C_L = 5 pF R_L = 667Ω
t_{PHZ} t_{PLZ}	Output Disable Time			25 25	ns	V_{CC} = 5.0 V

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_wH (CP)	Minimum Clock Pulse Width HIGH	20			ns	
t_wL (CP)	Minimum Clock Pulse Width LOW	20			ns	
t_s	**Set-up Time, $\overline{SR}$ to CP**	10			ns	
t_s	Set-up Time, S_0 or S to CP	10			ns	V_{CC} = 5.0 V
t_h	**Hold Time, $\overline{SR}$ to CP**	10			ns	C_L = 15 pF
t_h	Hold Time, S_0 or S to CP	10			ns	
t_s (H)	Set-up Time I/O_0 thru I/O_7, DS_0-DS_7 to CP (HIGH)	20			ns	
t_s (L)	Set-up Time I/O_0 thru I/O_7, DS_0-DS_7 to CP (LOW)	20			ns	
t_h	Hold Time (HIGH or LOW) I/O_0 thru I/O_7, DS_0-DS_7 to CP	0			ns	

DEFINITION OF TERMS:

SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

SN54LS324/SN74LS324 • SN54LS325/SN74LS325
SN54LS326/SN74LS326 • SN54LS327/SN74LS327

VOLTAGE-CONTROLLED OSCILLATORS

Advance Information

DESCRIPTION – Except for the LS324, all of these circuits feature two independent voltage-controlled oscillators on a single monolithic chip. The LS324, LS325 and LS326 have complementary outputs. Output frequency of the VCO is established by a single external component, in combination with voltage inputs, one for frequency control and on the LS324, another one for frequency range. These inputs can vary the output frequency by changing the voltage applied to them. These highly stable oscillators can operate at any frequency typically between 0.12 Hz and 30 MHz. With 2 volts on the frequency control input and the range input of the LS324, output frequency can be approximated as follows:

$$f_o = \frac{1 \times 10^{-4}}{C_{ext}}$$

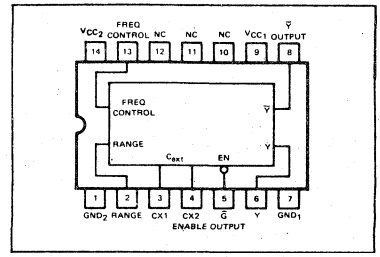
where: f_o = output frequency in hertz

C_{ext} = external capacitance in farads.

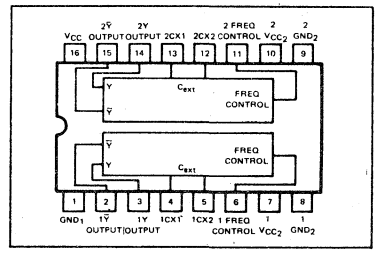
These devices can operate from a single 5-volt supply. However, a set of supply-voltage and ground pins (V_{CC1} and Gnd_1) is provided for the enable, synchronization-gating, and output sections, and a separate set (V_{CC2} and GND_2) is provided for the oscillator and associated frequency-control circuits so isolation can be accomplished in the system. Disabling either VCO of the LS325 and LS327 can be accomplished by removing the appropriate V_{CC2}. An enable input is available on both LS324 and LS326. While this input is low, the output is enabled. While the enable input is high, Y is high and $\overline{Y}$ is low.

- **LS325, LS326 AND LS327 HAVE TWO INDEPENDENT VCO'S IN A SINGLE PACKAGE**
- **SEPARATE SUPPLY VOLTAGE PINS FOR ISOLATION OF FREQUENCY CONTROL INPUTS AND OSCILLATORS FROM OUTPUT CIRCUITRY**
- **OUTPUT FREQUENCY SET BY ONE EXTERNAL COMPONENT:**
  - **CRYSTAL FOR HIGH-STABILITY FIXED-FREQUENCY OPERATION**
  - **CAPACITOR FOR FIXED-OR VARIABLE-FREQUENCY OPERATION**
- **HIGHLY STABLE OPERATION OVER SPECIFIED TEMPERATURE AND/OR SUPPLY VOLTAGE RANGES**

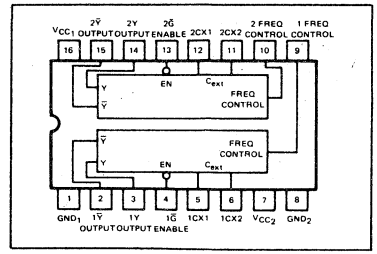
LS324 (TOP VIEW)



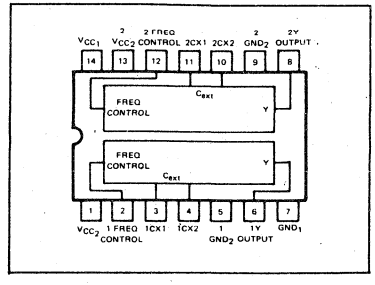
LS325 (TOP VIEW)



LS326 (TOP VIEW)



LS327 (TOP VIEW)



This is advance information and specifications are subject to change without notice.

Advance Information

SN54LS352/SN74LS352

DUAL 4-INPUT MULTIPLEXER

DESCRIPTION – The 54LS/74LS352 is a very high-speed Dual 4-Input Multiplexer with Common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The 54LS/74LS352 is the functional equivalent of the 54LS/74LS153 except with inverted outputs.

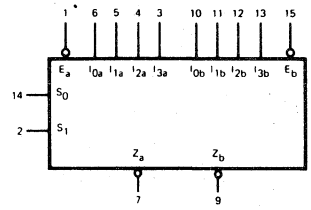
- **INVERTED VERSION OF THE 54LS/74LS153**
- **SEPARATE ENABLES FOR EACH MULTIPLEXER**
- **INPUT CLAMP DIODE LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
S_0, S_1	Common Select Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
I_0, I_1	Multiplexer Inputs	0.5 U.L.	0.75 U.L.
$\overline{Z}$	Multiplexer Outputs (note b)	10 U.L.	5 (2.5) U.L.

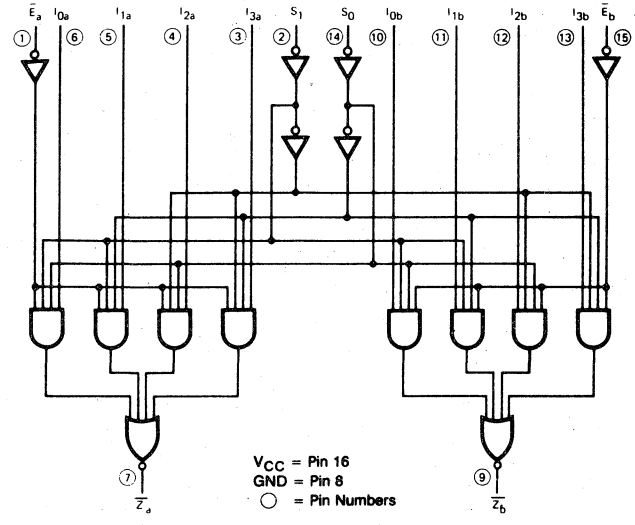
NOTES:
a. 1 TTL Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL

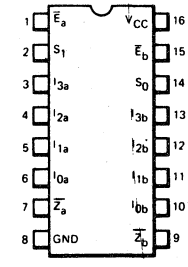


V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The 54LS/74LS352 is a Dual 4-Input Multiplexer. It selects two bits of data from up to four sources under the control of the common Select Inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs ($\overline{Z}_a$, $\overline{Z}_b$) are forced HIGH.

The logic equations for the outputs are shown below.

$$\overline{Z}_a = \overline{E}_a \cdot \overline{(I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)}$$

$$\overline{Z}_b = \overline{E}_b \cdot \overline{(I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)}$$

The 54LS/74LS352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select Inputs. A less obvious application is a function generator. The 54LS/74LS352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	$\overline{Z}$
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS352X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS352X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.2	10	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operations under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		16 17	29 38	ns	Fig. 2	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output		11 15	24 32	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		8 7	20 26	ns	Fig. 2	

AC WAVEFORMS

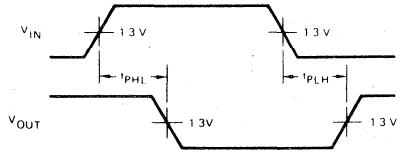


Fig. 1

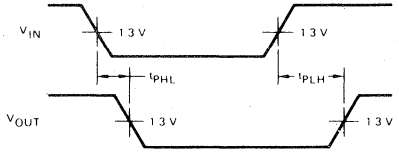


Fig. 2

Advance Information

SN54LS353/SN74LS353

DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

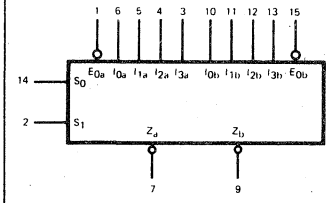
DESCRIPTION — TheLSTTL/MSI 54LS/74LS353 is a Dual 4-Input Multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable (E_0) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL families.

- **INVERTED VERSION OF 54LS/74LS253**
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES		LOADING (Note a) HIGH	LOW
S_0, S_1	Common Select Inputs	0.5 U.L.	0.25 U.L.
Multiplexer A			
$\overline{E}_{0a}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{3a}$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
$\overline{Z}_a$	Multiplexer Output (Note b)	65(25) U.L.	5(2.5) U.L.
Multiplexer B			
$\overline{E}_{0b}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_{0b} - I_{3b}$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
$\overline{Z}_b$	Multiplexer Output (Note b)	65(25) U.L.	5(2.5) U.L.

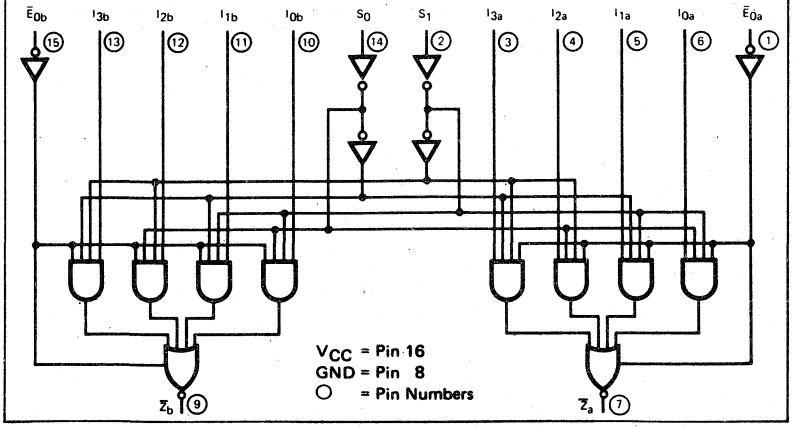
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military and 65 U.L. for Commercial Temperature Ranges.

LOGIC SYMBOL

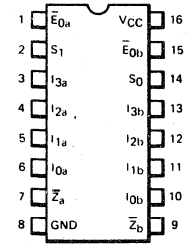


V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The 54LS/74LS353 contains two identical 4-input Multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable (E_{0a}, E_{0b}) inputs which when HIGH, forces the outputs to a high impedance (high Z) state.

The logic equations for the outputs are shown below:

$$\overline{Z_a} = \overline{\overline{E}_{0a} \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)}$$

$$\overline{Z_b} = \overline{\overline{E}_{0b} \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)}$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{E}_0$	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

H = HIGH Level
L = LOW Level
X = Immaterial
(Z) = High Impedance (off)
Address inputs S_0 and S_1 are common to both sections.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS353X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS353X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1			I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V, $\overline{V_E}$ = 2.0 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $\overline{V_E}$ = 2.0 V	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				-0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{SC}	Output Short Circuit Current (Note 4)		-20		-100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current, Outputs LOW			7.0	12	mA	V_{CC} = MAX, V_{IN} = 0 V, $\overline{V_E}$ = 0 V	
	Power Supply Current, Outputs Off			8.5	14		V_{CC} = MAX, V_{IN} = 0 V, $\overline{V_E}$ = 4.5 V	

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operations under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		10 10	25 20	ns	Fig. 1	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		20 16	45 32	ns	Fig. 1	C_L = 15 pF
t_{PZH}	Output Enable Time to HIGH Level		12	23	ns	Figs. 4, 5	C_L = 15 pF, R_L = 2 kΩ
t_{PZL}	Output Enable Time to LOW Level		11	23	ns	Figs. 3, 5	
t_{PLZ}	Output Disable Time from LOW Level		22	27	ns	Figs. 3, 5	C_L = 5 pF, R_L = 2 kΩ
t_{PHZ}	Output Disable Time from HIGH Level		11	41	ns	Figs. 4, 5	

3-STATE WAVEFORMS

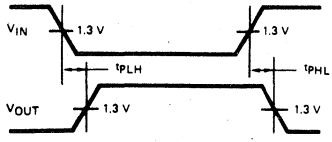


Fig. 1

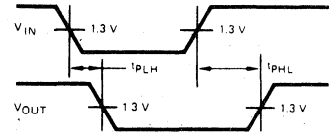


Fig. 2

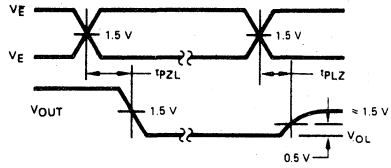


Fig. 3

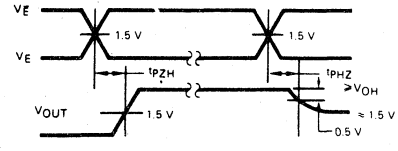
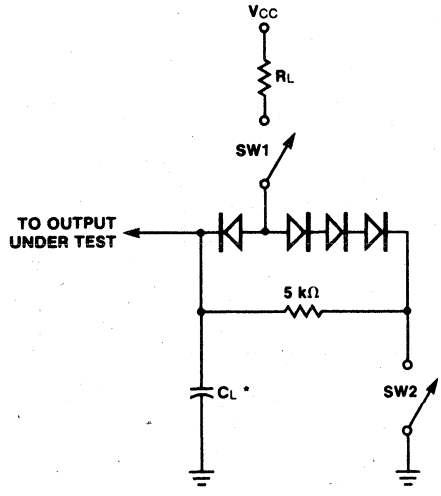


Fig. 4

AC LOAD CIRCUIT



*Includes Jig and Probe Capacitance

Fig. 5

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

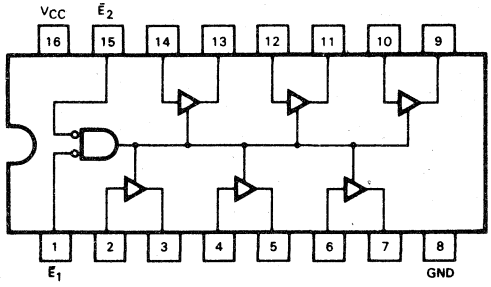
SN54LS365A/SN74LS365A • SN54LS366A/SN74LS366A
SN54LS367A/SN74LS367A • SN54LS368A/SN74LS368A

3-STATE HEX BUFFERS
(Formerly LS365, LS366, LS367, LS368)

DESCRIPTION — These devices are high speed hex buffers with 3-state outputs. They are organized as single 6-bit or 2-bit/4-bit, with inverting or non-inverting data (D) paths. The outputs are designed to drive 15 TTL Unit Loads or 60 Low Power Schottky loads when the Enable (E) is LOW.

When the Output Enable Input (E) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

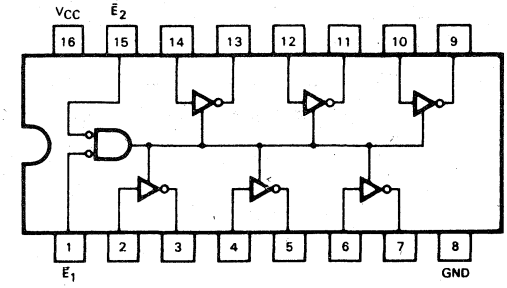
SN54LS365A/SN74LS365A
HEX 3-STATE BUFFER WITH COMMON 2-INPUT NOR ENABLE



TRUTH TABLE

INPUTS			OUTPUT
$\bar{E}_1$	$\bar{E}_2$	D	
L	L	L	L
L	L	H	H
H	X	X	(Z)
X	H	X	(Z)

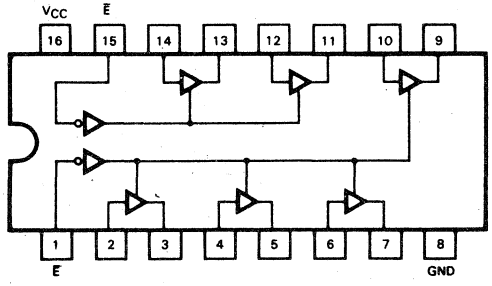
SN54LS366A/SN74LS366A
HEX 3-STATE INVERTER BUFFER WITH COMMON 2-INPUT NOR ENABLE



TRUTH TABLE

INPUTS			OUTPUT
$\bar{E}_1$	$\bar{E}_2$	D	
L	L	L	H
L	L	H	L
H	X	X	(Z)
X	H	X	(Z)

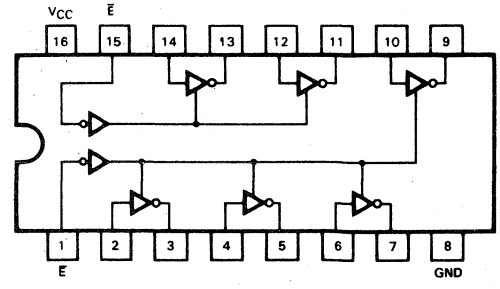
SN54LS367A/SN74LS367A
HEX 3-STATE BUFFER SEPARATE 2-BIT AND 4-BIT SECTIONS



TRUTH TABLE

INPUTS		OUTPUT
$\bar{E}$	D	
L	L	L
L	H	H
H	X	(Z)

SN54LS368A/SN74LS368A
HEX 3-STATE INVERTER BUFFER SEPARATE 2-BIT AND 4-BIT SECTIONS



TRUTH TABLE

INPUTS		OUTPUT
$\bar{E}$	D	
L	L	H
L	H	L
H	X	(Z)

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE MIN	SUPPLY VOLTAGE TYP	SUPPLY VOLTAGE MAX	TEMPERATURE
SN54LS365AX SN54LS366AX SN54LS367AX SN54LS368AX	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS365AX SN74LS366AX SN74LS367AX SN74LS368AX	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4			I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1			I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)		−30		−130	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current	LS365A/367A		13.5	24	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V	
		LS366A/368A		11.8	21			

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V (See SN54LS125A for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output (LS365A • LS367A)			10 16	ns	Fig. 2	C_L = 45 pF
t_{PLH} t_{PHL}	Propagation Delay, Data to Output (LS366A • LS368A)			10 16	ns	Fig. 1	C_L = 45 pF
t_{PZH}	Output Enable Time to HIGH Level			16	ns	Figs. 4, 5	C_L = 45 pF
t_{PZL}	Output Enable Time to LOW Level			30	ns	Figs. 3, 5	R_L = 667 Ω
t_{PLZ}	Output Disable Time from LOW Level			15	ns	Figs. 3, 5	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level			23	ns	Figs. 4, 5	R_L = 667 Ω

Advance Information

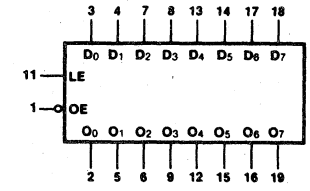
SN54LS373/SN74LS373

OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS

DESCRIPTION — The 54LS/74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedence state.

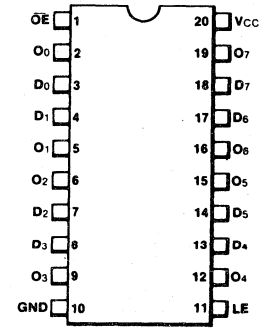
- **EIGHT LATCHES IN A SINGLE PACKAGE**
- **3-STATE OUTPUTS FOR BUS INTERFACING**
- **HYSTERESIS ON LATCH ENABLE**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATABLE**

LOGIC SYMBOL



VCC = Pin 20
GND = Pin10

CONNECTION DIAGRAM DIP (TOP VIEW)



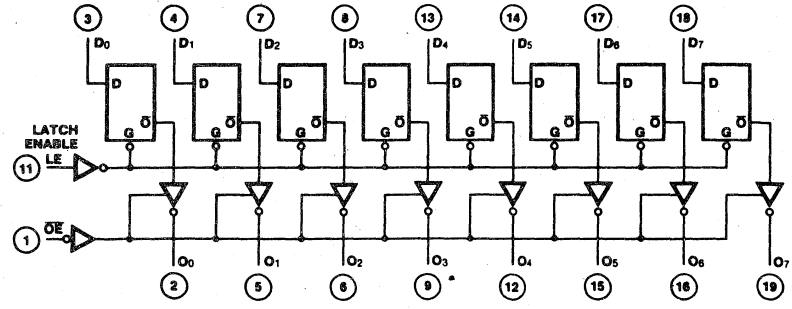
PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
D_0 - D_7	Data Inputs	0.5 U.L.	0.25 U.L.
LE	Latch Enable (Active HIGH) input	0.5 U.L.	0.25 U.L.
$\overline{OE}$	Output Enable (Active LOW) input	0.5 U.L.	0.25 U.L.
O_0 - O_7	Outputs (Note b)	65 (25) U.L.	15 (7.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

b) The Output LOW drive factor is 7.5 U.L. for Military and 25 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



VCC = Pin 20
GND = Pin 10
O= Pin Numbers

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS373X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS373X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGES (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	I_{OH} = −1.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1			I_{OH} = −2.6 mA
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 12 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5		I_{OL} = 24 mA
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2.0 V
I_{OZL}	Input Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, V_E = 2.0 V
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Input HIGH Current at MAX Input Voltage				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−30		−130	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current, Outputs OFF			24	40	mA	V_{CC} = MAX, V_{IN} = 0 V, V_E = 4.5 V

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operations under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_sD	Set-up Time Data to Negative Going LE	0	−2.0		ns	Fig. 1	
t_hD	Hold Time Data to Negative Going LE	10	7.0		ns	Fig. 1	V_{CC} = 5.0 V
t_wLE	Minimum LE Pulse Width HIGH or LOW	15	10		ns	Fig. 1	

DEFINITION OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to LE transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the LE transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition.

AC CHARACTERISTICS : $T_A = 25°C$, $V_{CC} = 5.0\ V$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		10 16	18 27	ns	Fig. 1	$C_L = 45\ pF$
t_{PLH} t_{PHL}	Propagation Delay, LE to Output		14 24	25 36	ns	Fig. 1	$C_L = 45\ pF$
t_{PZH}	Output Enable Time to HIGH Level		15	28	ns	Figs. 3, 4	$C_L = 15\ pF$
t_{PZL}	Output Enable Time to LOW Level		22	36	ns	Figs. 2, 4	$R_L = 667\Omega$
t_{PLZ}	Output Disable Time from LOW Level		13	25	ns	Figs. 2, 4	$C_L = 5.0\ pF$
t_{PHZ}	Output Disable Time from HIGH Level		11	20	ns	Figs. 3, 4	$R_L = 667\Omega$

AC WAVEFORMS

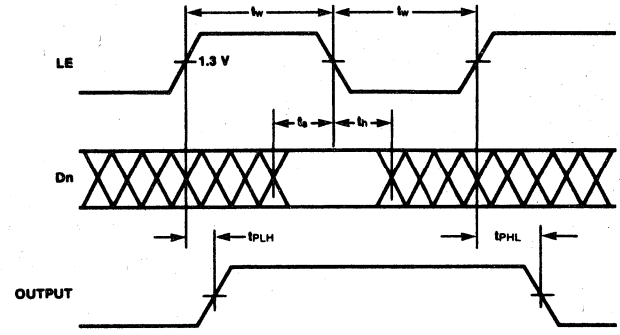


Fig. 1

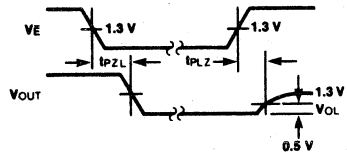


Fig. 2

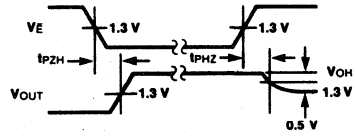
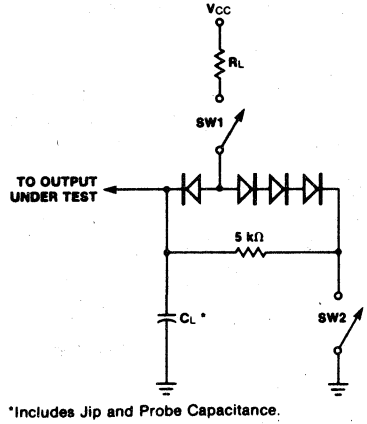


Fig. 3

AC LOAD CIRCUIT



*Includes Jip and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 4

Advance Information

SN54LS374/SN74LS374

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

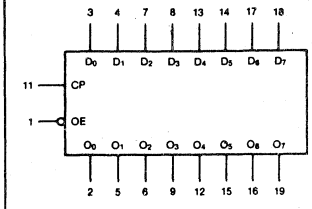
DESCRIPTION —The 54LS/74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) is common to all flip-flops. The 54LS/74LS374 is manufactured using advanced Low Power Schottky technology and is compatible with all Motorola TTL families

- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED POSITIVE EDGE-TRIGGERED CLOCK**
- **3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS**
- **HYSTERISIS ON OUTPUT ENABLE INPUT TO IMPROVE NOISE MARGIN**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES		LOADING (Note a) HIGH	LOW
D_0-D_7	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH going edge) Input	0.5 U.L.	0.25 U.L.
$\overline{OE}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
O_0-O_7	Outputs (Note b)	65(25) U.L.	15(7.5) U.L.

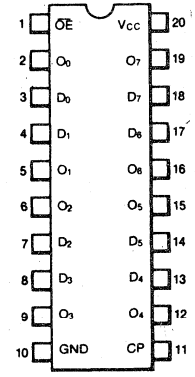
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The output LOW drive factor is 7.5 U.L. for military (54) and 24 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



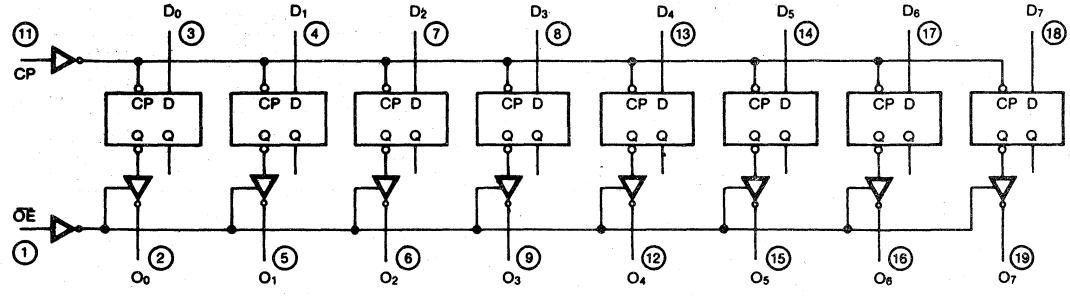
V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



TRUTH TABLE

Dn	CP	$\overline{OE}$	On
H	⎍	L	H
L	⎍	L	L
X	X	H	Z*

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedence

*Note: Contents of flip-flops unaffected by the state of the Output Enable input ($\overline{OE}$)

FUNCTIONAL DESCRIPTION—The 54LS/74LS374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The Clock and Output Enable are common. The eight flip-flops will store the state of their individual D inputs that meet the set-up and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are refected on the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedence state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	I_{OH} = −1.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1		V	I_{OH} = −2.6 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 12 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, $V_{\overline{E}}$ = 2.0 V
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Input HIGH Current at MAX Input Voltage				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		-30		-130	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current, Outputs OFF			27	45	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operations under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0\ V$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay, CP To Output			28 34	ns	Fig. 1	$C_L = 45\ pF$
t_{PZH}	Output Enable Time to HIGH Level			28	ns	Figs. 3, 4	$C_L = 45\ pF$
t_{PZL}	Output Enable Time to LOW Level			36	ns	Figs. 2, 4	$R_L = 667\Omega$
t_{PLZ}	Output Disable Time from LOW Level			24	ns	Figs. 2, 4	$C_L = 5.0\ pF$
t_{PHZ}	Output Disable Time from HIGH Level			18	ns	Figs. 3, 4	$R_L = 667\Omega$
f_{MAX}	Maximum Input Frequency	35	50		MHz	Fig. 1	$C_L = 45\ pF$

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
T_wCP	Minimum Clock Pulse Width, HIGH or LOW	13	10		ns	Fig. 1	$V_{CC} = 5.0\ V$
t_s	Minimum Set-up Time, Data to CP	20	15		ns	Fig. 1	
t_h	Minimum Hold Time, Data to CP	0	−3		ns	Fig. 1	

DEFINITION OF TERMS:

SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative Hold Time indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

AC WAVEFORMS

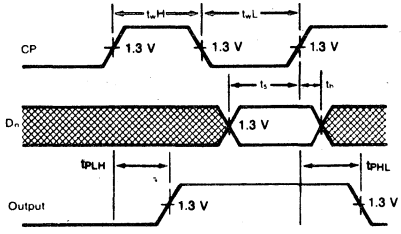


Fig. 1

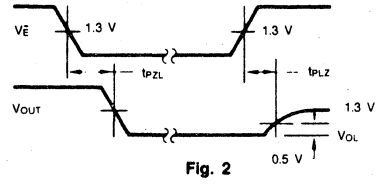


Fig. 2

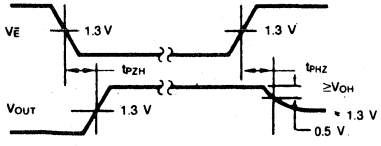
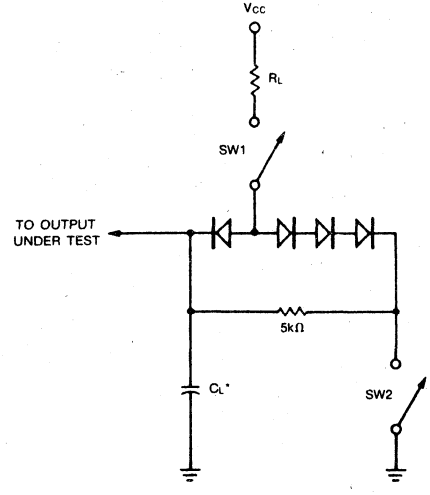


Fig. 3

AC LOAD CIRCUIT



*Includes Jig and Probe Capacitance.

Fig. 4

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Advance Information

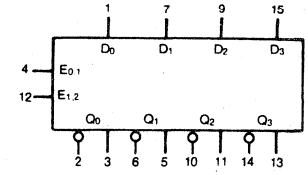
SN54LS375/SN74LS375

4-BIT LATCH

DESCRIPTION — The 54LS/74LS375 is a 4-Bit D-Type Latch for use as temporary storage for binary information between processing limits and input/output or indicator units. When the Enable (E) input is HIGH, information present at the D input will be transferred to the Q output and, if E is HIGH, the Q output will follow the input. When E goes LOW, the information present at the D input prior to its set up time will be retained at the Q outputs.

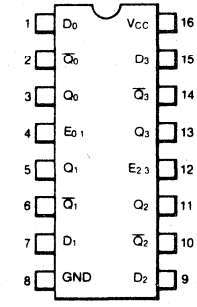
This device is functionally identical to the 54LS/74LS75 except for the corner power pins. For complete discussion of electrical characteristics, truth tables and operations information, refer to the 54LS/74LS75 data sheet.

LOGIC SYMBOL



V_{CC} = 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



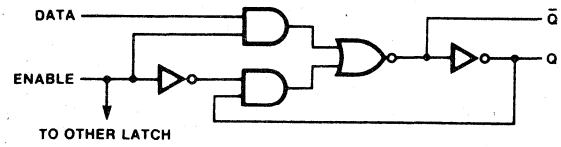
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOW
D_1-D_4	Data Inputs	0.5 U.L.	0.25 U.L.
E_{0-1}	Enable Input Latches 0, 1	2.0 U.L.	1.0 U.L.
E_{2-3}	Enable Input Latches 2, 3	2.0 U.L.	1.0 U.L.
Q_1-Q_4	Latch Outputs (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{Q}_1$-$\overline{Q}_4$	Complementary Latch Outputs (Note b)	10 U.L.	5 (2.5) U.L.

Notes:
a. 1 TTL Unit Load (U.L.) = 40μA HIGH/1.6mA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



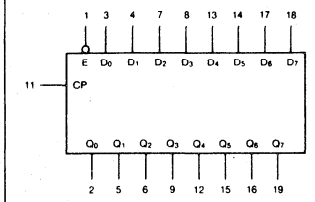
SN54LS377/SN74LS377

OCTAL D FLIP-FLOP WITH COMMON ENABLE AND CLOCK

DESCRIPTION: The 54LS/74LS377 is an 8-bit register built using advanced Low Power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common clock enable. The device is packaged in the space-saving (0.3 inch row spacing) 20-pin package.

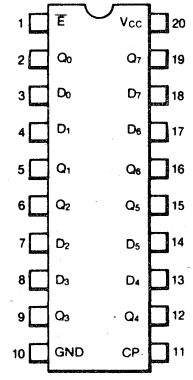
- **8-BIT HIGH SPEED PARALLEL REGISTERS**
- **POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOPS**
- **FULLY BUFFERED COMMON CLOCK AND ENABLE INPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



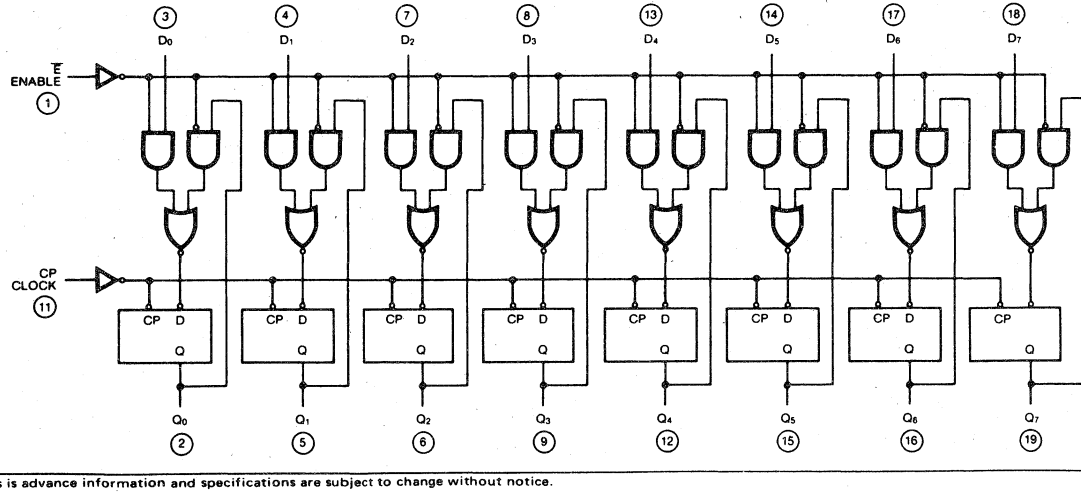
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
D_0-D_7	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
Q_0-Q_7	True Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The 54LS/74LS377 consists of eight edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable input ($\overline{E}$) are common to all flip-flops.

When $\overline{E}$ is LOW, new data is entered into the register on the next LOW-to-HIGH transition of (CP). When $\overline{E}$ is HIGH, the register will retain the present data independent of the CP.

TRUTH TABLE

$\overline{E}$	CP	D_n	Q_n
H	↑	X	No Change
L	↑	H	H
L	↑	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS377X	4.5 V	5.0 V	5.5 V	-55° C to +125° C
SN74LS377X	4.75 V	5.0 V	5.25 V	0° C to +70° C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage, All inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage, All inputs	
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			-0.65	-1.5	V	V_{CC} = MIN, I_{IN} = 18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = -400 μA	
		74	2.7	3.5			V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4 mA	V_{CC} = MIN, V_{IN} = V_{IH}
		74		0.35	0.5		I_{OL} = 8 mA	or V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				-0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 4)		-20		-100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			17	28	mA	V_{CC} = MAX	

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operations under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
F_{MAX}	Maximum Input Clock Frequency	30	45		MHz	Fig. 1	$V_{CC} = 5.0$ V
t_{PLH}	Propagation Delay,		17	27	ns	Fig. 1	$C_L = 15$ pF
t_{PHL}	Clock to Output		18	27	ns		

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_w CP	Minimum Clockpulse Width	20			ns	Fig. 1	
t_s	Set-up Time Data to Clock (HIGH or LOW)	20			ns	Fig. 1	
t_h	Hold Time, Data to Clock (HIGH or LOW)	5			ns	Fig. 1	
$t_s(H)$	Set-up Time HIGH, Enable to Clock	10			ns	Fig. 1	$V_{CC} = 5.0$ V
$t_h(H)$	Hold Time HIGH, Enable to Clock	5			ns	Fig. 1	$C_L = 15$pF
$t_s(L)$	Set-up Time LOW, Enable to Clock	25			ns	Fig. 1	
$t_h(L)$	Hold Time LOW, Enable to Clock	5			ns	Fig. 1	

DEFINITION OF TERMS:

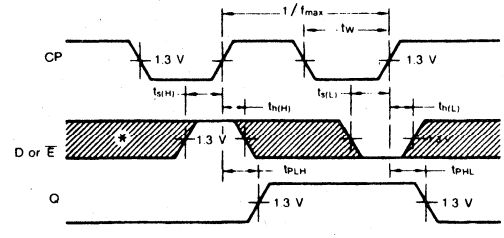
SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative Hold Time indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, CLOCK PULSE WIDTH, FREQUENCY, SET-UP AND HOLD TIMES DATA OR ENABLE TO CLOCK



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Advance Information

SN54LS378/SN74LS378

HEX PARALLEL D REGISTER WITH ENABLE

DESCRIPTION – The 54LS/74LS378 is a 6-Bit Register with a buffered common enable. This device is similar to the 54LS/74LS174, but with common Enable rather than common Master Reset.

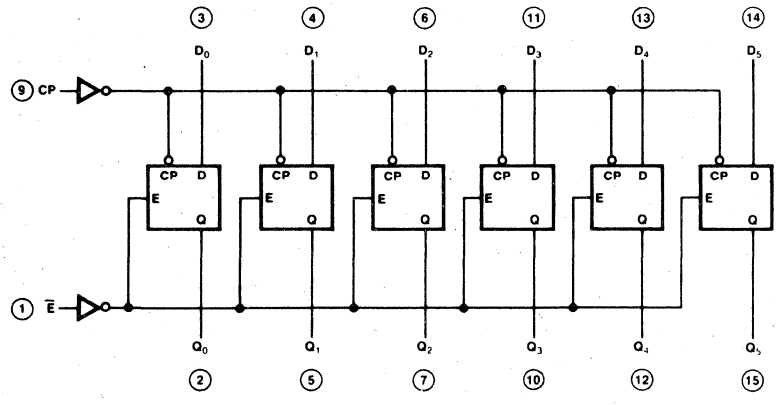
- **6-BIT HIGH-SPEED PARALLEL REGISTER**
- **POSITIVE EDGE-TRIGGERED D-TYPE INPUTS**
- **FULLY BUFFERED COMMON CLOCK AND ENABLE INPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULL TTL AND CMOS COMPATIBLE**

PIN NAMES

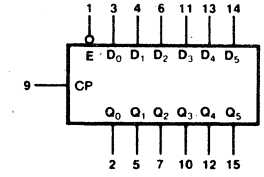
		LOADING (Note a)	
		HIGH	LOW
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
D_0-D_5	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge Input)	0.5 U.L.	0.25 U.L.
Q_0-Q_5	True Outputs (Note b)	0.10 U.L.	0.25 U.L.

Notes:
a. 1 TTL Unit Load (U.L.) = 40μA HIGH 1.6mA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM

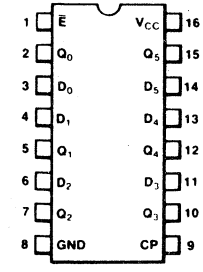


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The 54LS/74LS378 consists of six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable (E) inputs are common to all flip flops.

When the $\overline{E}$ input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the $\overline{E}$ input is HIGH the register will retain the present data independent of the CP input.

TRUTH TABLE

$\overline{E}$	CP	D_n	Q_n
H	⎍	X	No change
L	⎍	H	H
L	⎍	L	L

H = High Voltage Level
L = Low Voltage Level
X = Immaterial

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS378X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS378X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			16	27	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operations under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

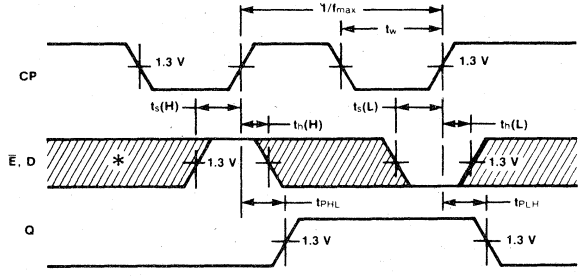
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	CP to Q Output			27 27	ns ns	Fig. 1	V_{CC} = 5.0 V
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 1	

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_s	Set-up Time, Data to Clock (HIGH or LOW)	20			ns	Fig. 1	V_{CC} = 5.0 V
t_h	Hold Time, Data to Clock (HIGH or LOW)	5			ns	Fig. 1	
t_s	Set-up Time, Enable to Clock (HIGH or LOW)	25			ns	Fig. 1	
t_h	Hold Time Enable to Clock (HIGH or LOW)	5			ns	Fig. 1	
t_{WCP}	Minimum Clock Pulse Width	20					

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, CLOCK PULSE WIDTH, FREQUENCY, SET-UP AND HOLD TIMES DATA, ENABLE TO CLOCK



*The shaded areas indicate when the input is permitted to change for predictable output performance.

DEFINITION OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

Advance Information

SN54LS379/SN74LS379

QUAD PARALLEL REGISTER WITH ENABLE

DESCRIPTION — The 54LS/74LS379 is a 4-Bit Register with buffered common Enable. This device is similar to the 54LS/74LS175 but features the common Enable rather than common Master Reset.

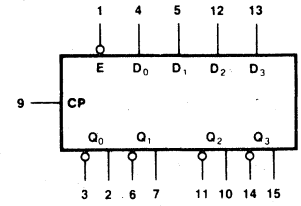
- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED POSITIVE EDGE-TRIGGERED CLOCK**
- **BUFFERED COMMON ENABLE INPUT**
- **TRUE AND COMPLEMENT OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
D_0-D_3	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
Q_0-Q_3	True Outputs (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{Q}_0$-$\overline{Q}_3$	Complemented Outputs (Note b)	10 U.L.	5 (2.5) U.L.

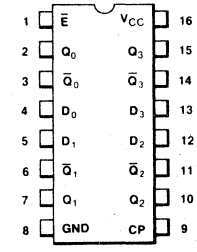
Notes:
a. 1 TTL Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



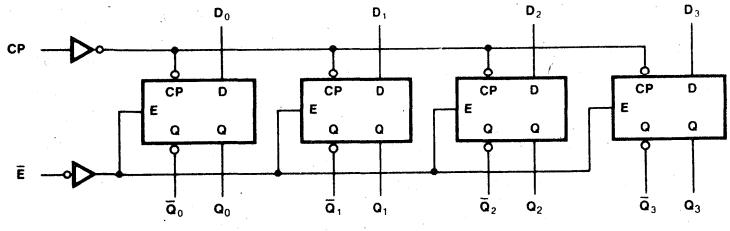
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION – The 54LS/74LS379 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops. When the $\overline{E}$ input is HIGH, the register will retain the present data independent of the CP input.

TRUTH TABLE

$\overline{E}$	CP	D_n	Q_n	$\overline{Q}_n$
H	⎍	X	No Change	No Change
L	⎍	H	H	L
L	⎍	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS379X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS379X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA; V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5		I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current $\overline{E}$, D_0-D_3, CP				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Input HIGH Current at MAX Input Voltage $\overline{E}$, D_0-D_3, CP				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current $\overline{E}$, D_0-D_3, CP				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current				18	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C

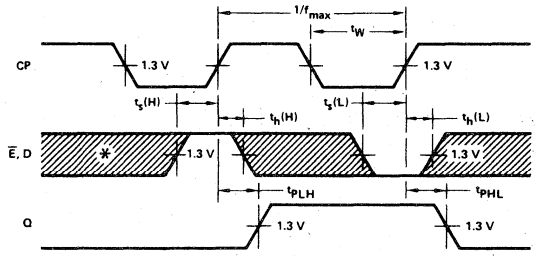
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	CP to Output			20 22	ns	Fig. 1, V_{CC} = 5.0V C_L = 15 pF
f_{MAX}	Maximum Clock Frequency	30	45		MHz	

AC SET-UP REQUIREMENTS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_s	Set-Up Time, Data to Clock (HIGH or LOW)	20			ns	Fig. 1
t_h	Hold Time, Data to Clock (HIGH or LOW)	5			ns	Fig. 1
t_s	Set-up Time, Enable to Clock	25			ns	Fig. 1
t_h	Hold Time, Enable to Clock	5			ns	Fig. 1
t_wCP	Minimum Clock Pulse Width	17	10		ns	

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS,
CLOCK PULSE WIDTH, FREQUENCY,
SET-UP AND HOLD TIMES DATA, ENABLE TO CLOCK



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

DEFINITION OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

SN54LS384/SN74LS384

8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

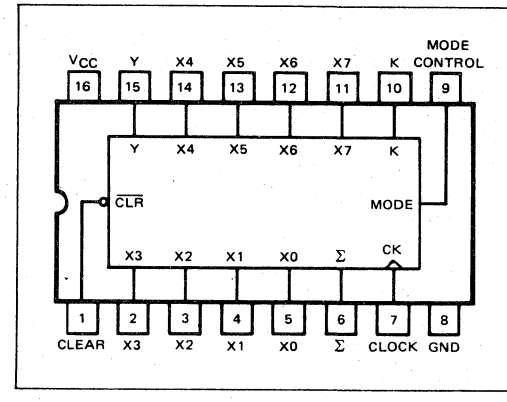
Advance Information

DESCRIPTION – The SN54LS/74LS384 is an 8 x 1 bit sequential logic element that performs digital multiplication of two numbers represented in two's-complement form to obtain a two's-complement product. The device accepts an 8-bit multiplicand (X input) and stores this data in eight internal latches. These X latches are controlled by the clear input. With the clear input low, all internal flip-flops are cleared and the X latches opened to accept new multiplicand data. When the clear input is high, the latches are closed.

The multiplier word data is passed by the Y input in a serial bit stream, least significant bit first. The product is clocked out the Σ output.

The multiplication of an m-bit number by an n-bit number results in an (m + n)-bit product. The LS384 must be clocked for m + n clock cycles to produce this two's complement product. The n-bit multiplier (Y-input) sign bit data must be extended for the remaining m bits to complete the multiplication cycle.

(TOP VIEW)



- **TWO'S-COMPLEMENT MULTIPLICATION**
- **8-BIT PARALLEL MULTIPLICAND DATA INPUT**
- **SERIAL DATA OUTPUT FOR MULTIPLICATION PRODUCT**
- **MAGNITUDE ONLY MULTIPLICATION**
- **SERIAL MULTIPLIER DATA INPUT**
- **CASCADABLE FOR ANY NUMBER OF BITS**
- **40 MHz TYPICAL MAXIMUM CLOCK FREQUENCY**

INPUTS				INTERNAL	OUTPUT	FUNCTION
CLR	CK	X_j	Y	Y_{-1}	Σ	
L	X	Data	X	L	L	Load new multiplicand and clear internal sum and carry registers
H	↑	X	L	L	Output per Booth's algorithm	Shift sum register
H	↑	X	L	H		Add multiplicand to sum register and shift
H	↑	X	H	L		Subtract multiplicand from sum register and shift
H	↑	X	H	H		Shift sum register

H = high-level, L = low-level, X = irrelevant, ↑ = low-to-high-level transition

This is advance information and specifications are subject to change without notice.

SN54LS385/SN74LS385

QUADRUPLE SERIAL ADDERS/SUBTRACTORS

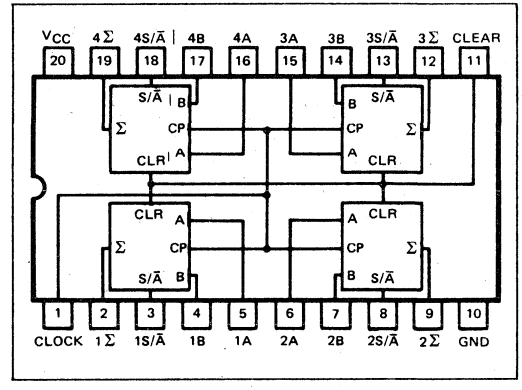
Advance Information

DESCRIPTION — The SN54LS/74LS385 is a general-purpose adder/subtractor which is useful as a companion part to the SN54LS384/SN74LS384 two's-complement multiplier. The LS385 contains four independent adder/subtractor elements with common clock and clear.

Each of four independent sum (Σ) outputs reflects the respective A and B input and is controlled by the S/$\overline{A}$ pin.

When low, the clear input asynchronously resets the sum flip-flop low and the carry flip-flop either high in the subtract mode or low in the add mode. The clock is positive-edge triggered and controls the sum and carry flip-flops.

(TOP VIEW)



- **FOUR SYNCHRONOUS ELEMENTS IN A SINGLE 20-PIN PACKAGE**
- **INDEPENDENT TWO'S-COMPLEMENT ADDITION/SUBTRACTION**
- **BUFFERED CLOCK AND DIRECT CLEAR INPUTS**

FUNCTION TABLE

SELECTED	INPUTS					INTERNAL CARRY D INPUT		Σ OUTPUT
FUNCTION	CLEAR	S/Ā	A	B	CLOCK	BEFORE ↑	AFTER ↑	AFTER ↑
Clear	L	L	X	X	X	L	L	L
	L	H	X	X	X	H	H	L
Add	H	L	L	L	↑	L	L	L
	H	L	L	L	↑	H	L	H
	H	L	L	H	↑	L	L	H
	H	L	L	H	↑	H	H	L
	H	L	H	L	↑	L	L	H
	H	L	H	L	↑	H	H	L
	H	L	H	H	↑	L	H	L
	H	L	H	H	↑	H	H	H
Subtract	H	H	L	L	↑	L	L	H
	H	H	L	L	↑	H	H	L
	H	H	L	H	↑	L	L	L
	H	H	L	H	↑	H	L	H
	H	H	H	L	↑	L	H	L
	H	H	H	L	↑	H	H	H
	H	H	H	H	↑	L	L	H
	H	H	H	H	↑	H	H	L

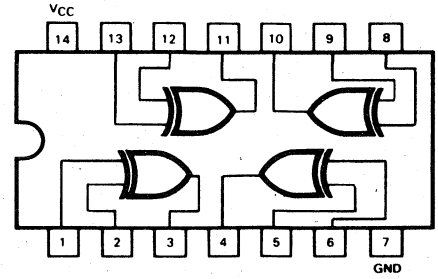
H = high level, L = low level, X = irrelevant,
↑ = transition from low to high level at the clock input

This is advance information and specifications are subject to change without notice.

SN54LS386/SN74LS386

QUAD 2-INPUT EXCLUSIVE-OR GATE

CONNECTION AND LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE MIN	SUPPLY VOLTAGE TYP	SUPPLY VOLTAGE MAX	TEMPERATURE
SN54LS386X	4.5 V	5.0 V	5.5 V	-55°C to +125°C
SN74LS386X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			-0.65	-1.5	V	V_{CC} = MIN, I_{IN} = -18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = -400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				-0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-20		-100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Supply Current			6.1	10	mA	V_{CC} = MAX, V_{IN} = 0 V

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, Other Input LOW			12 17	ns	V_{CC} = 5.0 V
t_{PLH} t_{PHL}	Propagation Delay, Other Input HIGH			10 12	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

SN54LS390/SN74LS390 • SN54LS393/SN74LS393

DUAL DECADE COUNTER
DUAL 4-STAGE BINARY COUNTER

DESCRIPTION — The 54LS/74LS390 and 54LS/74LS393 each contain a pair of high-speed 4-stage ripple counters. Each half of the LS390 is partitioned into a divide-by-two section and a divide-by-five section, with a separate clock input for each section. The two sections can be connected to count in the 8.4.2.1 BCD code or they can count in a bi-quinary sequence to provide a square wave (50% duty cycle) at the final output.

Each half of the LS393 operates as a Modulo-16 binary divider, with the last three stages triggered in a ripple fashion. In both the 'LS390 and the 'LS393, the flip-flops are triggered by a HIGH-to-LOW transition of their CP inputs. Each half of each circuit type has a Master Reset input which responds to a HIGH signal by forcing all four outputs to the LOW state.

FEATURES

- **DUAL VERSIONS OF LS290 AND LS293**
- **LS390 HAS SEPARATE CLOCKS ALLOWING ÷2, ÷2.5, ÷5**
- **INDIVIDUAL ASYNCHRONOUS CLEAR FOR EACH COUNTER**
- **TYPICAL MAX COUNT FREQUENCY OF 50 MHZ**
- **INPUT CLAMP DIODES MINIMIZE HIGH SPEED TERMINATION EFFECTS**

PIN NAMES		LOADING (Note a) HIGH	LOW
$\overline{CP}$	Clock (Active LOW going edge) Input to +16 (LS393)	0.5 U.L.	1.0 U.L.
$\overline{CP}_0$	Clock (Active LOW going edge) Input to ÷2 (LS390)	0.5 U.L.	1.0 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷5 (LS390)	0.5 U.L.	1.5 U.L.
MR	Master Reset (Active HIGH) Input	0.5 U.L.	0.25 U.L.
Q_0-Q_3	Flip-Flop outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:

a. **1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.**

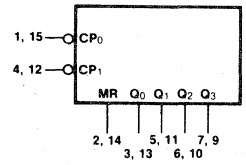
b. **The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.**

FUNCTIONAL DESCRIPTION — Each half of the 54LS/74LS393 Operates in the Modulo 16 binary sequence, as indicated in the ÷16 Truth Table. The first flip-flop is triggered by HIGH-to-LOW transitions of the CP input signal. Each of the other flip-flops is triggered by a HIGH-to-LOW transition of the Q output of the preceding flip-flop. Thus state changes of the Q outputs do not occur simultaneously. This means that logic signals derived from combinations of these outputs will be subject to decoding spikes and, therefore, should not be used as clocks for other counters, registers or flip-flops. A HIGH signal on MR forces all outputs to the LOW state and prevents counting

Each half of the 'LS390 contains a ÷5 section that is independent except for the common MR function. The ÷5 section operates in 4.2.1 binary sequence, as shown in the ÷5 Truth Table, with the third stage output exhibiting a 20% duty cycle when the input frequency is constant. To obtain a ÷10 function having a 50% duty cycle output, connect the input signal to $\overline{CP}_1$ and connect the Q_3 output to the $\overline{CP}_0$ input; the Q_0 output provides the desired 50% duty cycle output. If the input frequency is connected to $\overline{CP}_0$ and the Q_0 output is connected to $\overline{CP}_1$, a decade divider operating in the 8.4.2.1 BCD code is obtained, as shown in the BCD Truth Table. Since the flip-flops change state asynchronously, logic signals derived from combinations of 'LS390 outputs are also subject to decoding spikes. A HIGH signal on MR forces all outputs LOW and prevents counting.

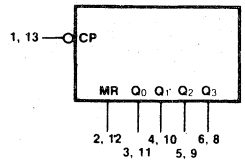
LOGIC SYMBOLS

54LS/74LS390 One Half Shown



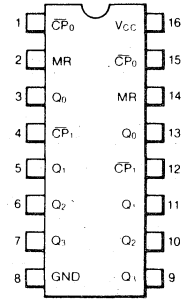
V_{CC} = Pin 16
GND = Pin 8

54LS/74LS393 One Half Shown

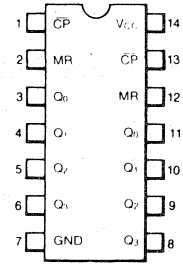


CONNECTION DIAGRAMS
DIP (TOP VIEW)

54LS/74LS390

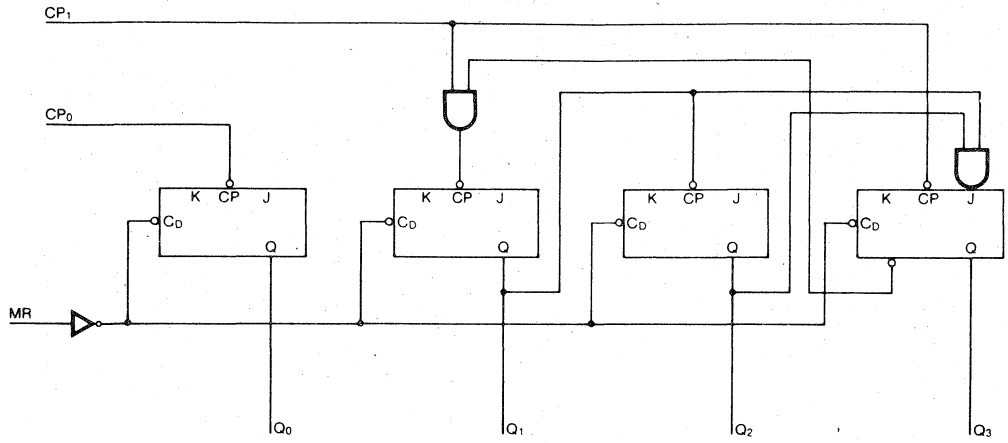


54LS/74LS393

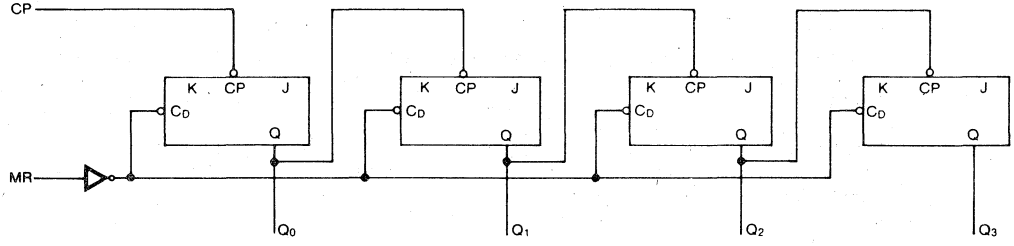


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

54LS/74LS390 LOGIC DIAGRAM (one half shown)



54LS/74LS393 LOGIC DIAGRAM (one half shown)



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS390X SN54LS393X	4.5 V	5.0 V	5.5 V	-55°C to +125°C
SN74LS390X SN74LS393X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

54LS/74LS390 BCD TRUTH TABLE (Input on $\overline{CP}_0$; Q_0 $\overline{CP}_1$)

COUNT	OUTPUTS			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

54LS/74LS390 ÷ 5 TRUTH TABLE (Input on $\overline{CP}_1$)

COUNT	OUTPUTS		
	Q_3	Q_2	Q_1
0	L	L	L
1	L	L	H
2	L	H	L
3	L	H	H
4	H	L	L

54LS/74LS393 TRUTH TABLE

COUNT	OUTPUTS			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMTER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			-0.65	-1.5	V	V_{CC} = MIN, I_{IN} = -18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = -400 μA
		74	2.7	3.4			V_{IN} = V_{IL} or V_{IH} per Truth Table
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 8 mA; V_{CC} = MIN V_{IH} or
		74		0.35	0.5		I_{OL} = 8 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current			1.0	20.0	μA	V_{CC} = MAX V_{IN} = 2.7 V
	$\overline{CP}$, $\overline{CP}_0$, $\overline{CP}_1$				0.1	mA	V_{CC} = MAX V_{IN} = 5.5 V
	MR				0.1	mA	V_{CC} = MAX V_{IN} = 10 V
I_{IL}	Input LOW Current						
	MR				-0.4		
	$\overline{CP}$, $\overline{CP}_0$				-1.6	mA	V_{CC} = MAX
	$\overline{CP}_1$				-2.4		V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		-15		-100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current	LS390		20	25	mA	V_{CC} = MAX
		LS393		20	30		

NOTES:
1. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC2} = 5.0 V, T_A = 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	$\overline{CP}$ or $\overline{CP_0}$ to Q_0		10 10	20 20	ns	Fig. 1	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH} t_{PHL}	$\overline{CP_1}$ to Q_1		23 23	60 60	ns	Fig. 1	
t_{PHL}	MR to Any Q		30	39	ns	Fig. 2	
f_{MAX}	$\overline{CP}$ or $\overline{CP_0}$ Input Count Frequency	40	50		MHz	Fig. 1	
f_{MAX}	$\overline{CP_1}$ Input Count Frequency	20	25		MHz	Fig. 1	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_W	$\overline{CP}$ or $\overline{CP_0}$ Pulse Width	12	9		ns	Fig. 1	$V_{CC} = 5.0$ V
t_W	$\overline{CP_1}$ Pulse Width	24	20		ns	Fig. 1	
t_W	MR Pulse Width	18	15		ns	Fig. 2	
t_{rec}	MR to $\overline{CP}$	15	10		ns	Fig. 2	

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH to LOW in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

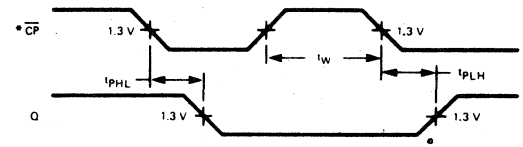


Fig. 1

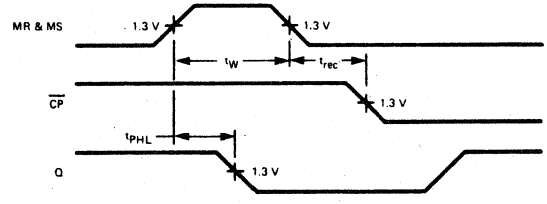


Fig. 2

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.

SN54LS395/SN74LS395

4-BIT SHIFT REGISTER WITH 3-STATE OUTPUTS

DESCRIPTION – The 54LS/74LS395 is a 4-Bit Register with 3-state outputs and can operate in either a synchronous parallel load or a serial shift-right mode, as determined by the Select input. An asynchronous active LOW Master Reset (MR) input overrides the synchronous operations and clears the register. An active LOW Output Enable (OE) input controls the 3-state output buffers, but does not interfere with the other operations. The fourth stage also has a conventional output for linking purposes in multi-stage serial operations.

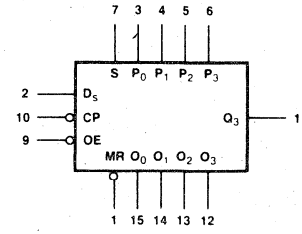
- **SHIFT LEFT OR PARALLEL 4-BIT REGISTER**
- **3-STATE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATIBLE**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
P_0-P_3	Parallel inputs	0.5 U.L.	0.25 U.L.
D_S	Serial Data input	0.5 U.L.	0.25 U.L.
S	Mode Select input	0.5 U.L.	0.25 U.L.
$\overline{CP}$	Clock (Active LOW) input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) input	0.5 U.L.	0.25 U.L.
$\overline{OE}$	Output Enable (Active LOW) input	0.5 U.L.	0.25 U.L.
O_0-O_3	3-State Register Outputs	10 U.L.	5 (2.5) U.L.
Q_3	Register Output	10 U.L.	5 (2.5) U.L.

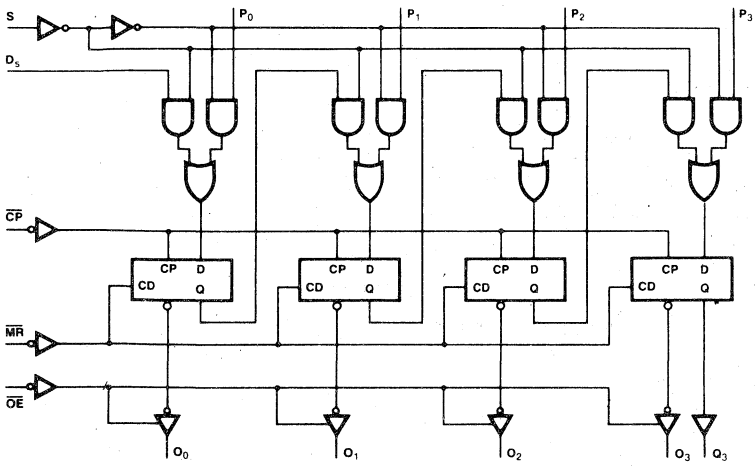
NOTES:
a. 1 TTL Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for MILITARY (54) and 5 U.L. for COMMERCIAL (74) Temperature Ranges.

LOGIC SYMBOL

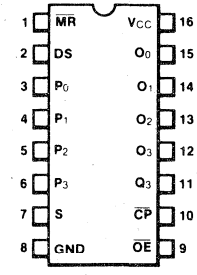


V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS395X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS395X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

FUNCTIONAL DESCRIPTION – The 54LS/74LS395 contains four D-type edge-triggered flip-flops and auxiliary gating to select a D input either from a Parallel (Pn) input or from the preceding stage. When the Select input is HIGH, the Pn inputs are enabled. A LOW signal on the S input enables the serial inputs for shift-right operations, as indicated in the Truth Table.

State changes are initiated by HIGH-to-LOW transitions on the Clock Pulse (CP) input. Signals on the P_n, D_s and S inputs can change when the Clock is in either state, provided that the recommended set-up and hold times are observed. When the S input is LOW, a CP HIGH-LOW transition transfers data in Q_0 to Q_1, Q_1 to Q_2, and Q_2 to Q_3. A left-shift is accomplished by connecting the outputs back to the P_n inputs, but offset one place to the left, i.e., O_3 to P_2, O_2 to P_1, and O_1 to P_0, with P_3 acting as the linking input from another package.

When the $\overline{OE}$ input is HIGH, the output buffers are disabled and the O_0-O_3 outputs are in a high impedance condition. The shifting, parallel loading or resetting operations can still be accomplished, however.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGES (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage				−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.4			V	I_{OH} = −1.0 mA; V_{CC} = MIN, V_{IN} = V_{IH}
		74	2.4				I_{OH} = −2.6 mA; or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54, 74			0.4	V	I_{OL} = 4.0mA; V_{CC} = MIN, V_{IN} = V_{IH}
		74			0.5	V	I_{OL} = 8.0mA; or V_{IL} per Truth Table
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2.0 V
I_{OZL}	Input Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 2.0 V
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					100	μA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−15		−130	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current Outputs HIGH				29	mA	V_{CC} = MAX, V_{CP} = ⎍, V_E = 4.5 V
	Power Supply Current Outputs LOW				25		V_{CC} = MAX, V_{CP} = 0 V, V_E = 0 V

AC CHARACTERISTICS : T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Maximum Input Shift Frequency	30			MHz	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH}	Propagation Delay, Clock to Output			35	ns	Fig. 1	
t_{PHL}				25			
t_{PHL}	Propagation Delay MR to Output			35	ns	Fig. 1	

AC CHARACTERISTICS: For 3-State Output Buffers

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PZH}	Output Enable Time to HIGH Level			20	ns	Fig. 4, 5	C_L = 15 pF
t_{PZL}	Output Enable Time to LOW Level			20	ns	Fig. 3, 5	R_L = 2 kΩ
t_{PLZ}	Output Disable Time from LOW Level			17	ns	Fig. 3, 5	C_L = 5 pF
t_{PHZ}	Output Disable Time from HIGH Level			23	ns	Figs. 4, 5	R_L = 2 kΩ

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_wCP	Clock Pulse Width	18			ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_s	Set-up Time, Data to Clock	20			ns	Fig. 1	
t_h	Hold Time, Data to Clock	5			ns	Fig. 1	
t_s	Set-up Time, Select to Clock	20			ns	Fig. 2	
t_h	Hold Time, Select to Clock	5			ns	Fig. 2	
t_wMR	Master Reset Minimum Pulse Width	20			ns	Fig. 1	

MODE SELECT – TRUTH TABLE

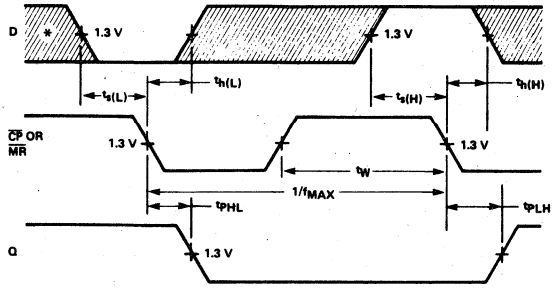
Operating Mode	Inputs @ t_n					Outputs @ t_{n+1}			
	$\overline{MR}$	$\overline{CP}$	S	D_S	P_n	O_0	O_1	O_2	O_3
Asynchronous Reset	L	X	X	X	X	L	L	L	L
Shift, SET First Stage	H	⌐¬	L	H	X	H	O_{0n}	O_{1n}	O_{2n}
Shift, RESET First Stage	H	⌐¬	L	L	X	L	O_{0n}	O_{1n}	O_{2n}
Parallel Load	H	⌐¬	H	X	P_n	P_0	P_1	P_2	P_3

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
$t_{n, n+1}$ = time before and after CP HIGH-to-LOW transition

NOTE:
When $\overline{OE}$ is LOW, outputs O_0-O_3 are in the high impedance state; however, this does not affect other operations or the Q_3 output.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



*The Data Input is D_S for S = LOW and P_n for S = HIGH.

Fig. 1

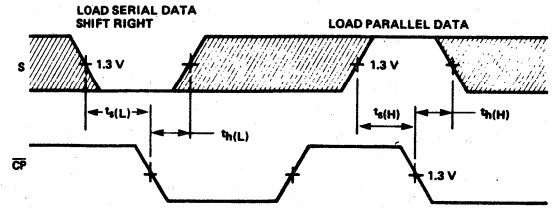


Fig. 2

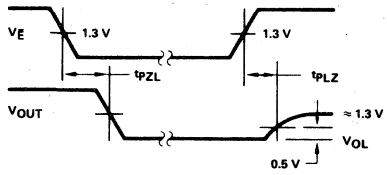


Fig. 3

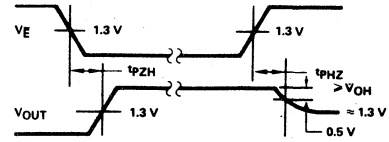
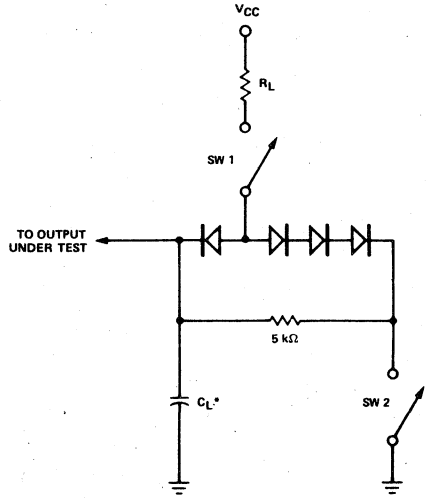


Fig. 4

AC LOAD CIRCUIT



*Includes Jig and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 5

SN54LS398/SN74LS398 • SN54LS399/SN74LS399

QUAD 2-PORT REGISTER
(QUAD 2-INPUT MULTIPLEXER WITH STORAGE)

Advance Information

DESCRIPTION—The 54LS/74LS398 and 54LS/74LS399 are Quad 2-Port Registers. They are the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register on the LOW-to-HIGH transition of the Clock input. The 54LS/74LS398 features both Q and $\overline{Q}$ inputs, while the 54LS/74LS399 has only Q outputs.

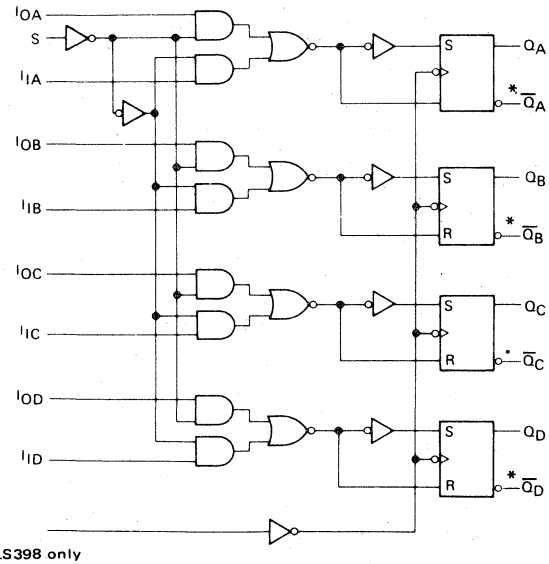
- **SELECT FROM TWO DATA SOURCES**
- **FULLY POSITIVE EDGE-TRIGGERED OPERATION**
- **BOTH TRUE AND COMPLEMENTED OUTPUTS ON 54LS/74LS398**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
S	Common Select Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
I_{0a} — I_{0d}	Data Inputs From Source 0	0.5 U.L.	0.25 U.L.
I_{1a} — I_{0d}	Data Inputs From Source 1	0.5 U.L.	0.25 U.L.
Q_a — Q_d	Register True Outputs (Note b)	1.0 U.L.	5(2.5) U.L.
Q_a — Q_d	Register Complementary Outputs (Note b)	10 U.L.	5(2.5) U.L.

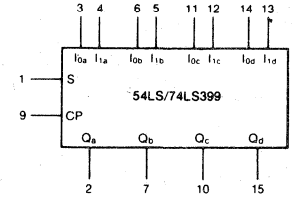
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

FUNCTIONAL BLOCK DIAGRAM



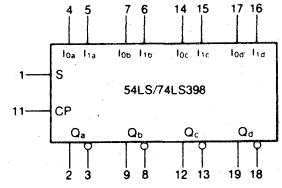
*54LS/74LS398 only

LOGIC SYMBOL



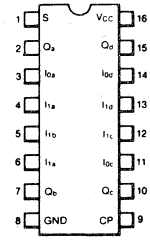
V_{CC} = 16
GND = 8

LOGIC SYMBOL

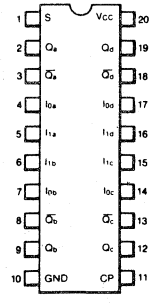


V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)
54LS/74LS399



CONNECTION DIAGRAM
DIP (TOP VIEW)
54LS/74LS398



FUNCTIONAL DESCRIPTION — The 54LS/74LS398 and 54LS/74LS399 are high-speed Quad 2-Port Registers. They select four bits of data from two sources (Ports) under the control of a common Select Input (S). The selected data is transferred to a 4-Bit Output Register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-Bit RS type output register is fully edge-triggered. The Data inputs (I) and Select inputs (S) must be stable only a set-up time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation. The 54LS/74LS398 has both Q and Q Outputs available.

FUNCTION TABLE

INPUTS			OUTPUTS	
S	I_0	I_1	Q	$\overline{Q}$*
l	l	X	L	H
l	h	X	H	L
h	X	l	L	H
h	X	h	H	L

* 54LS/74LS398 ONLY

l = LOW Voltage Level one set-up time prior to the LOW-to-HIGH clock transition
h = HIGH Voltage Level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURES
	MIN	TYP	MAX	
SN54LS398X SN54LS399X	4.5 V	5.0 V	5.5 V	-55°C to +125°C
SN74LS398X SN74LS399X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA | V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA | V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		-20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			7.3	13	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output Q			27 32	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to $\overline{Q}$ (LS398 only)			27 32	ns	Fig. 1	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
$t_{W(H)}$	Clock Pulse Width (HIGH)	20			ns	Fig. 1	V_{CC} = 5.0 V
$t_{W(L)}$	Clock Pulse Width (LOW)	20			ns		
$t_{s(Data)}$	Set-up Time, Data to Clock	20			ns	Fig. 1	
$t_{h(Data)}$	Hold Time, Data to Clock	0			ns		
$t_{s(S)}$	Set-up Time, Select to Clock	25			ns	Fig. 2	
$t_{h(S)}$	Hold Time, Select to Clock	0			ns		

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative Hold Time indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

AC WAVEFORMS

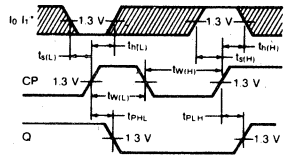


Fig. 1

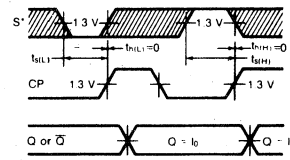


Fig. 2

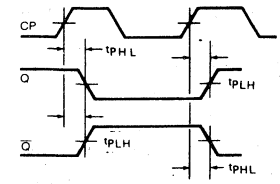


Fig. 3

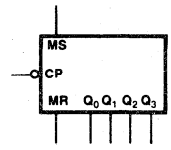
*The shaded areas indicate when the input is permitted to change for predictable output performance.

SN54LS490/SN74LS490
DUAL DECADE COUNTER

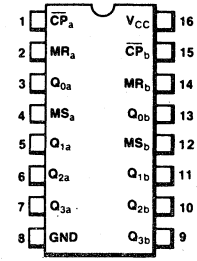
DESCRIPTION – The 54LS/74LS490 contains a pair of high-speed 4-stage ripple counters. Each half of the 54LS/74LS490 has individual Clock, Master Reset and Master Set (Preset 9) inputs. Each section counts in the 8, 4, 2, 1 BCD code.

- **DUAL VERSION OF 54LS/74LS90**
- **INDIVIDUAL ASYNCHRONOUS CLEAR AND PRESET TO 9 FOR EACH COUNTER**
- **COUNT FREQUENCY – TYPICALLY 65 MHz**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL
(EACH HALF)



CONNECTION DIAGRAM
DIP (TOP VIEW)

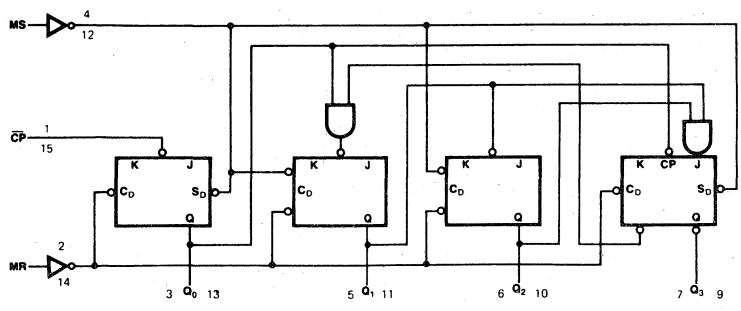


PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
MS	Master Set (Set to 9) Input	0.5 U.L.	0.25 U.L.
MR	Master Reset	0.5 U.L.	0.25 U.L.
$\overline{CP}$	Clock Input (Active LOW Going Edge)	1.5 U.L.	1.5 U.L.
Q_0-Q_3	Counter Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM (ONE HALF SHOWN)



TRUTH TABLE

COUNT	OUTPUTS			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS490X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS490X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54 74			0.7 0.8	V	Guaranteed Input LOW Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54 74	2.5 2.7			V	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	74, 54 74		0.25 0.35	0.4 0.5	V	I_{OL} = 4 mA; I_{OL} = 8 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current MR, MS $\overline{CP}$				20 60	μA μA	V_{CC} = MAX V_{IN} = 2.7 V
	$\overline{CP}$ MR, MS				300 100	μA μA	V_{IN} = 5.5 V $\overline{CP}$ only V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current $\overline{CP}$ MR, MS				−2.4 −0.4	mA mA	V_{CC} = MAX V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			19	26	mA	V_{CC} = MAX

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_w	$\overline{CP}$, MR or MS Pulse Width	20	14		ns	Figs. 1, 2, 3	V_{CC} = 5.0 V
t_{rec}	MR or MS to $\overline{CP}$	15	12		ns	Figs. 2, 3	

DEFINITION OF TERMS:

RECOVERY TIME (t_{rec}) – is defined as the minimum time required between the end of the MS or MR pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH Data to the Q outputs.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Maximum Input Count Frequency	40	65		MHz	Fig. 1	$V_{CC} = 5.0$ V $C_L = 15$ pF $R_L = 2$ kΩ
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to Q_0		5.0 6.0	15 15	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q_1 or Q_3		17 19	30 30	ns	Fig. 3	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to Q_2		25 26	45 45	ns	Fig. 2	
t_{PHL}	Propagation Delay, MR to Output		27	39	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, MS to Output		13 20	35 35	ns	Fig. 2	

NOTES:
1. Conditions for testing, not shown in the table, are chosen to guarantee operations under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at $V_{CC} = 5.0$ V, $T_A = 25°C$, and maximum loading.
4. Not more than one output should be shorted at a time.

AC WAVEFORMS

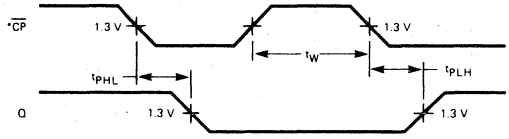


Fig. 1

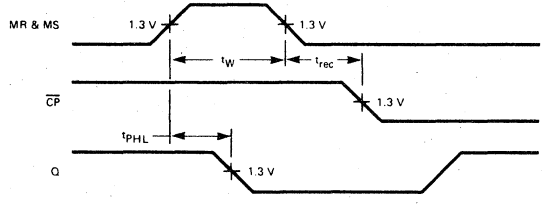


Fig. 2

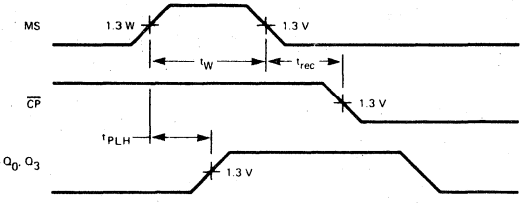


Fig. 3

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the Truth Table.

Advance Information

SN54LS502/SN74LS502

8-BIT SUCCESSIVE APPROXIMATION REGISTER

DESCRIPTION – The 54LS/74LS502 is an 8-Bit Register with the interstage logic necessary to perform serial-to-parallel conversion and provide an active LOW Conversion Complete (CC) signal coincident with storage of the eighth bit. An active LOW Start (S) input performs synchronous initialization which forces Q_7 LOW and all other outputs HIGH. Subsequent clocks shift this Q_7 LOW signal downstream which simultaneously backfills the register such that the first serial data (D input) bit is stored in Q_7, the second bit in Q_6, the third in Q_5, etc. The serial input data is also synchronized by an auxiliary flip-flop and brought out on Q_D.

Designed primarily for use in the successive approximation technique for analog to digital conversion, the 54LS/74LS502 can also be used as a serial to parallel converter, ring counter and as the storage and control element in recursive digital routines.

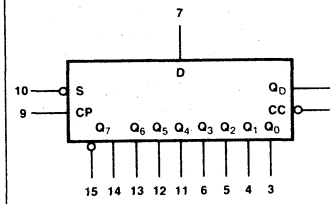
- **LOW POWER SCHOTTKY VERSION OF 2502**
- **STORAGE AND CONTROL FOR SUCCESSIVE APPROXIMATION**
- **A TO D CONVERTERS**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{CC}$	Conversion complete (active LOW) output (note b)	10 U.L.	5(2.5) U.L
CP	Clock Pulse (active HIGH going edge) input	0.5 U.L.	0.25 U.L.
D	Serial Data Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_7$	Parallel Register Outputs	10 U.L.	5(2.5) U.L.
$\overline{Q_7}$	Complement of Q_7 output	10 U.L.	5(2.5) U.L.
Q_D	Synchronized serial data output	10 U.L.	5(2.5) U.L.
$\overline{S}$	Start (active LOW) input	0.5 U.L.	0.25 U.L.

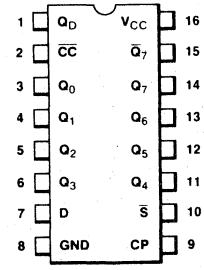
NOTES:
a) 1 TTL Unit Load (U.L.)=40μA HIGH/1.6mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

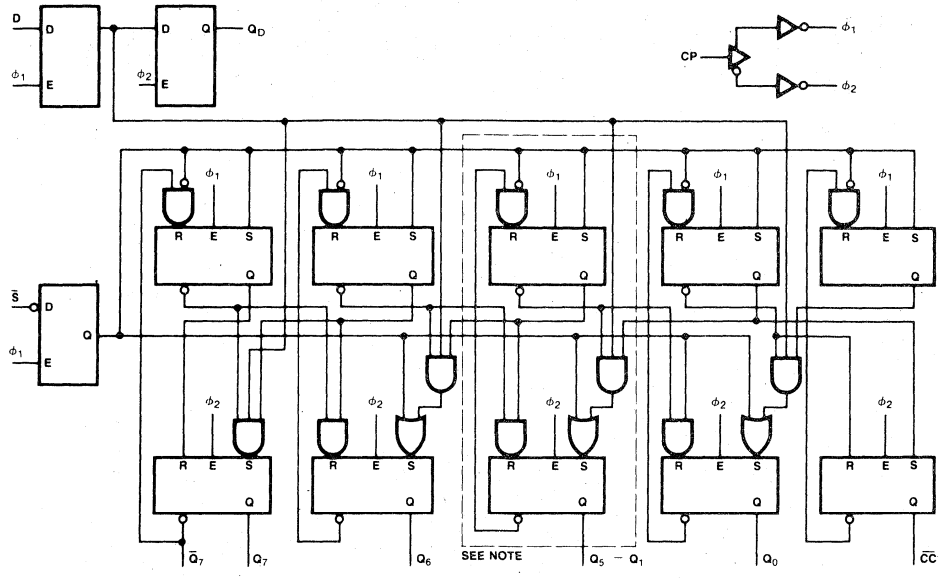
CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

This is advance information and specifications are subject to change without notice.

LOGIC DIAGRAM



Note: Cell logic is repeated for register stages Q_5 to Q_1.

FUNCTIONAL DESCRIPTION – The register stages are composed of transparent RS latches arranged in Master/Slave pairs. The master and slave latches are enabled separately by non-overlapping complementary signals ϕ_1 and ϕ_2 derived internally from the CP input. Master latches are enabled when CP is LOW and slave latches are enabled when CP is HIGH. Information is transferred from master to slave, and thus to the outputs, by the LOW-to-HIGH transition of CP.

Initializing the register requires a LOW signal on $\overline{S}$ while exercising CP. With $\overline{S}$ and CP LOW, all master latches are SET (Q side HIGH). A LOW-to-HIGH CP transition, with S remaining LOW, then forces the slave latches to the condition wherein Q_7 is LOW and all other register outputs, including $\overline{CC}$, are HIGH. This condition will prevail as long as $\overline{S}$ remains LOW, regardless of subsequent CP rising edge. To start the conversion process, $\overline{S}$ must return to the HIGH state. On the next CP rising edge, the information stored in the serial data input latch is transferred to Q_D and Q_7, while Q_6 is forced to the LOW state. On the rising edge of the next seven clocks, this LOW signal is shifted downstream, one bit at a time, while the serial data enters the register position one bit behind this LOW signal, as shown in the Truth Table. Note that after a serial data bit appears at a particular output, that register position undergoes no further changes. After the shifted LOW signal reaches $\overline{CC}$, the register is locked up and no further changes can occur until the register is initialized for the next conversion process.

Figure 1 shows a simplified hook-up of a 54LS/74LS502, a D/A converter and a comparator arranged to convert an analog input voltage into an 8-bit binary number by the successive approximation technique. Figure 2 is an idealized graph showing the various values that the D/A converter output voltage can assume in the course of the conversion. The vertical axis is calibrated in fractions of the full-scale output capability of the D/A converter and the horizontal axis represents the successive states of the Truth Table. At time t_1, Q_7 is LOW and Q_6-Q_0 are HIGH, causing the D/A output to be one-half of full scale. If the analog input voltage is greater than this voltage the comparator output (hence the D input of the 54LS/74LS502) will be LOW, and at times t_2 the D/A output will rise to three-fourths of full scale because Q_7 will remain LOW and contribute 50% while Q_6 is forced LOW and contributes another 25%. On the other hand, if the analog input voltage is less than one-half of full scale, the comparator output will be HIGH and Q_7 will go HIGH at t_2. Q_6 will still be forced LOW at t_2, and the D/A output will decrease to 25% of full scale.

Thus with each successive clock, the D/A output will change by smaller increments. When the conversion is completed at t_9, the binary number represented by the register outputs will be the numerator of the fraction n/256, representing the analog input voltage as a fraction of the fullscale output D/A converter.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS502X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS502X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

TRUTH TABLE

Time	Inputs		Outputs									
t_n	D	$\overline{S}$	Q_D	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	$\overline{CC}$
0	X	L	X	X	X	X	X	X	X	X	X	X
1	D_7	H	X	L	H	H	H	H	H	H	H	H
2	D_6	H	D_7	D_7	L	H	H	H	H	H	H	H
3	D_6	H	D_6	↓	D_6	L	H	H	H	H	H	H
4	D_4	H	D_5	↓	↓	D_5	L	H	H	H	H	H
5	D_3	H	D_4	↓	↓	↓	D_4	L	H	H	H	H
6	D_2	H	D_3	↓	↓	↓	↓	D_3	L	H	H	H
7	D_1	H	D_2	↓	↓	↓	↓	↓	D_2	L	H	H
8	D_0	H	D_1	↓	↓	↓	↓	↓	↓	D_1	L	H
9	X	H	D_0	↓	↓	↓	↓	↓	↓	↓	D_0	L
10	X	H	X	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = immaterial

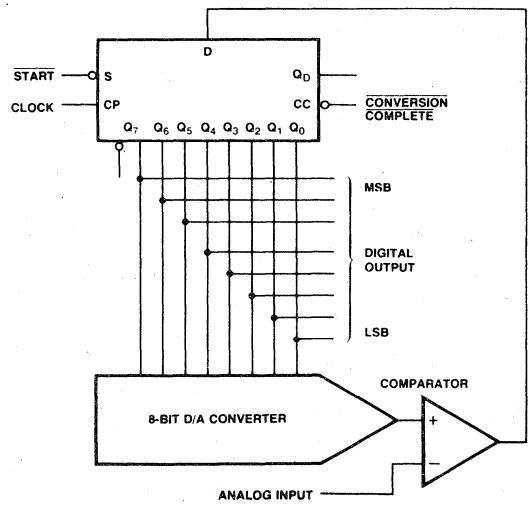


Fig. 1

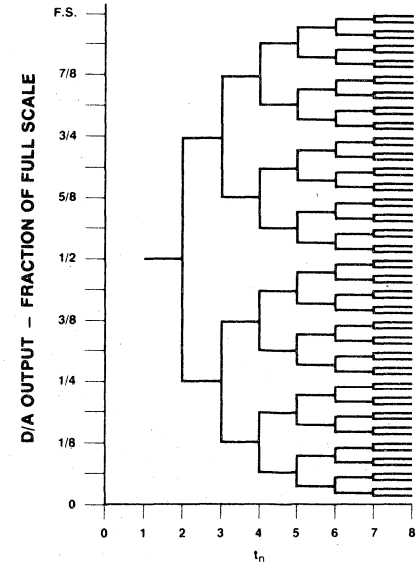


Fig. 2

Advance Information

SN54LS540/SN74LS540 • SN54LS541/SN74LS541

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

DESCRIPTION – The 54LS/74LS540 and 54LS/74LS541 are similar in function to the 54LS/74LS240 and 54LS/74LS241, respectively, except that Inputs and Outputs are on opposite sides of the package (see Logic Diagram). This pinout arrangement makes these devices especially useful as output ports for the Microprocessors, allowing ease of layout and greater PC board density.

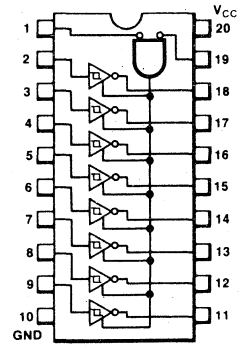
- HYSTERESIS AT INPUTS TO IMPROVE NOISE MARGIN
- PNP INPUTS REDUCE LOADING
- 3-STATE OUTPUTS DRIVE BUS LINES
- INPUTS AND OUTPUTS OPPOSITE SIDE OF PACKAGE, ALLOWING EASIER INTERFACE TO MICROPROCESSORS
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

TRUTH TABLE

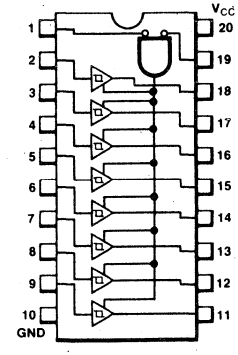
INPUTS			OUTPUTS	
E_1	E_2	D	LS540	LS541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
Z = High Impedance

LOGIC DIAGRAM AND CONNECTION DIAGRAM DIP (TOP VIEW)



LOGIC DIAGRAM AND CONNECTION DIAGRAM DIP (TOP VIEW)



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS540X SN54LS541X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS540X SN74LS541X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGES (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	I_{OH} = −12 mA; V_{CC} = MIN, V_{IN} = V_{IH}
		74	2.4	3.1			I_{OH} = −15 mA; or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 12 mA; V_{CC} = MIN, V_{IN} = V_{IH}
		74		0.35	0.5	V	I_{OL} = 24 mA; or V_{IL} per Truth Table
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2.0 V
I_{OZL}	Input Off Current LOW				−20	μA	V_{CC} = MAX. V_{OUT} = 0.4 V, V_E = 2.0 V
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX. V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX. V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−50		−225	mA	V_{CC} = MAX. V_{OUT} = 0 V
I_{CC}	Power Supply Current	LS540		29	50	mA	V_{CC} = MAX. V_{IN} = 0 V, V_E = 4.5 V
		LS541		32	54		

NOTES:
1. For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS : T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay, Data to Output LS540			14 18	ns	Fig. 2	C_L = 45 pF
t_{PLH} t_{PHL}	Propagation Delay Data to Output LS541			18 18	ns	Fig. 1	C_L = 45 pF
t_{PZH}	Output Enable Time to HIGH Level			23	ns	Figs. 4, 5	C_L = 45 pF
t_{PZL}	Output Enable Time to LOW Level			30	ns	Figs. 3, 5	R_L = 667 Ω
t_{PLZ}	Output Disable Time from LOW Level			25	ns	Figs. 3, 5	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level			18	ns	Figs. 4, 5	R_L = 667 Ω

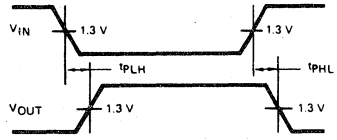


Fig. 1

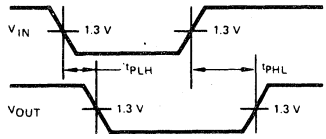


Fig. 2

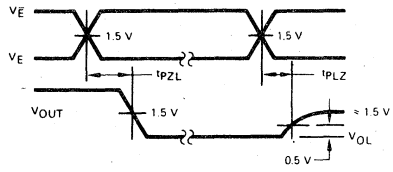


Fig. 3

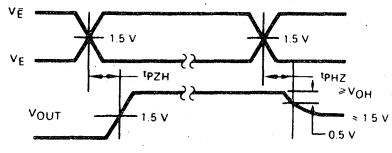
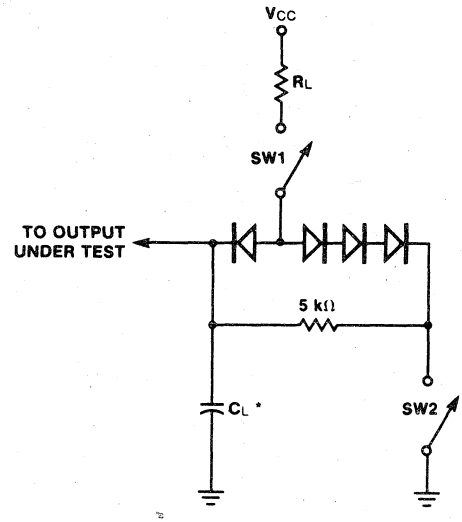


Fig. 4



SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 5

Advance Information

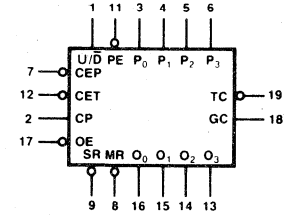
SN54LS568/SN74LS568 • SN54LS569/SN74LS569

UP/DOWN DECADE COUNTER • UP/DOWN BINARY COUNTER WITH 3-STATE OUTPUTS

DESCRIPTION — The 54LS/74LS568 and 54LS/74LS569 are 4-Stage Programmable Up/Down BCD and Binary Counters respectively. Each counter features both a Synchronous Reset (SR) and an Asynchronous Master Reset (MR), a single Up/Down (U/D) control and 3-state outputs for bus organized systems. Both counters are fully edge-triggered, with all functions except Master Reset (MR) and Output Enable (OE) synchronized to the LOW-to-HIGH transition of the Clock (CP) input.

Function and operation of these counters is similar to the 54LS/74LS168 and 54LS/74LS169.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

- **FULLY SYNCHRONOUS OPERATION**
- **FULL CARRY LOOKAHEAD FOR EASY CASCADING**
- **SINGLE UP/DOWN CONTROL INPUT**
- **FULL PRESET CAPABILITY**
- **3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS**
- **INPUT CLAMP DIODES TO LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATIBLE**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$\overline{CEP}$	Count Enable Parallel (active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{CET}$	Count Enable Trickle (active LOW) Input	1.0 U.L.	0.5 U.L.
CP	Clock Pulse (active positive going edge) Input	0.5 U.L.	0.25 U.L.
GC	Gated Clock Output (note b)	10.0 U.L.	0.5 (2.5) U.L.
$\overline{MR}$	Asynchronous Reset (active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{OE}$	3-State Output Enable (active LOW) Input	0.5 U.L.	0.25 U.L.
P_n	Parallel Data Input	0.5 U.L.	0.25 U.L.
$\overline{PE}$	Parallel Enable (active LOW) Input	0.5 U.L.	0.25 U.L.
O_n	Flip-Flop outputs (note b)	65 (25) U.L.	15 (7.5) U.L.
$\overline{TC}$	Terminal Count (active LOW) Output (note b)	10 U.L.	5 (2.5) U.L.
$\overline{SR}$	Synchronous Reset (active LOW) Input	1.0 U.L.	0.5 U.L.
$U/\overline{D}$	Up-Down Count Control Input	0.5 U.L.	0.25 U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

This is advance information and specifications are subject to change without notice.

FUNCTION TABLE

INPUTS							RESPONSE
$\overline{MR}$	$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	V/$\overline{D}$	CP	
L	X	X	X	X	X	X	Asynchronous RESET; Q_n = LOW
H	L	X	X	X	X	⎍	Synchronous RESET; Q_n = LOW
H	H	L	X	X	X	⎍	Parallel Load; $P_n \rightarrow Q_n$
H	H	H	H	X	X	X	Hold
H	H	H	X	H	X	X	Hold
H	H	H	L	L	H	⎍	Count Up
H	H	H	L	L	L	⎍	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

GC TRUTH TABLE

INPUTS				GC OUTPUT
$\overline{CEP}$	$\overline{CET}$	$\overline{TC}$*	CP	
L	L	L	⎍	⎍
H	X	X	X	H
X	H	X	X	H
L	L	H	X	H

*TC is generated internally.

Advance Information

SN54LS573/SN74LS573

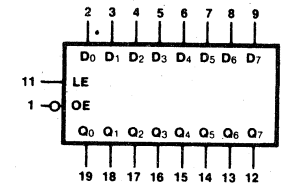
OCTAL D-TYPE LATCH WITH 3-STATE OUTPUTS

GENERAL DESCRIPTION – The 54LS/74LS573 is a High-Speed Octal Latch with Buffered Common Latch Enable (LE) and Buffered Common Output Enable (OE) inputs.

This device is functionally identical to the 54LS/74LS373, but has different pin-outs. For truth tables, discussion of operations and AC and DC specifications, please refer to the 54LS/74LS373 Data Sheet.

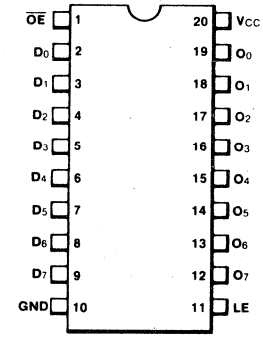
- **INPUTS AND OUTPUTS ON OPPOSITE SIDES OF PACKAGE ALLOWING EASY INTERFACE WITH MICROPROCESSORS**
- **USEFUL AS INPUT OR OUTPUT PORT FOR MICROPROCESSORS**
- **FUNCTIONALLY IDENTICAL TO 54LS/74LS373**
- **INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

CONNECTION DIAGRAM DIP (TOP VIEW)

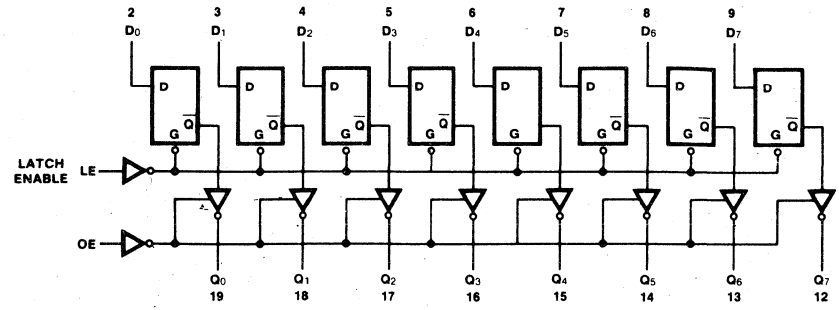


PIN NAMES

		LOADING (Note a) HIGH	LOW
D_0 - D_7	Data Inputs	0.5 U.L.	0.25 U.L.
LE	Latch Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{OE}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
O_0 - O_7	Outputs (Note b)	65 (25) U.L.	15 (7.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 μA HIGH 1.6 mA LOW
b) The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



VCC = Pin 20
GND = Pin 10
0 = Pin numbers

SN54LS574/SN74LS574

OCTAL D FLIP-FLOP WITH 3-STATE OUTPUTS

DESCRIPTION — The 54LS/74LS574 is a high-speed low-power Octal Flip-Flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

This device is functionally identical to the 54LS/74LS374 except for the pinouts. For complete discussions of operations, truth tables, AC and DC electrical specifications, refer to the 54LS/74LS374 data sheet.

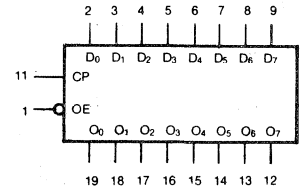
- **INPUTS AND OUTPUTS ON OPPOSITE SIDES OF PACKAGE ALLOWING EASY INTERFACE WITH MICROPROCESSORS**
- **USEFUL AS INPUT OR OUTPUT PORT FOR MICROPROCESSORS**
- **FUNCTIONALLY IDENTICAL TO 54LS/74LS374**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
$D_0 - D_7$	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH going edge) Input	0.5 U.L.	0.25 U.L.
$\overline{OE}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$O_0 - O_7$	Outputs (Note b)	65(25) U.L.	15(7.5) U.L.

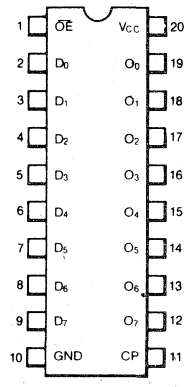
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



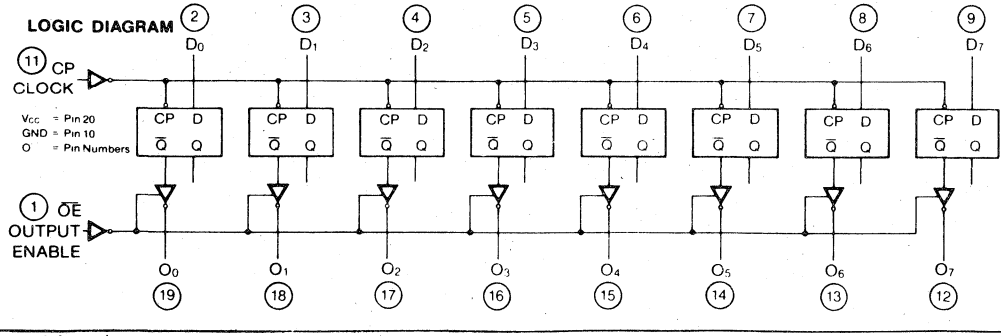
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
SN54LS574X	4.5 V	5.0 V	5.5 V	-55°C to +125°C
SN74LS574X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpack, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

LOGIC DIAGRAM



This is advance information and specifications are subject to change without notice.

SN54LS640/SN74LS640 • SN54LS641/SN74LS641
SN54LS642/SN74LS642 • SN54LS645/SN74LS645

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

Advance Information

DESCRIPTION — These octal bus transceivers are ideally suited for asynchronous two-way communication between data buses. Control function implementation minimizes external timing requirements.

These circuits allow data transmission from the A bus to B bus or from the B bus to A bus depending upon the logic level of the direction control (DIR) input. Enable input ($\overline{G}$) can disable the device so that the buses are effectively isolated.

- **BI-DIRECTIONAL BUS TRANSCEIVERS IN HIGH-DENSITY 20-PIN PACKAGES**
- **CHOICE OF TRUE OR INVERTING LOGIC**
- **CHOICE OF 3-STATE OR OPEN-COLLECTOR OUTPUTS**
- **PNP INPUTS REDUCE D-C LOADING ON BUS LINES**
- **HYSTERESIS AT BUS INPUTS IMPROVES NOISE MARGINS**

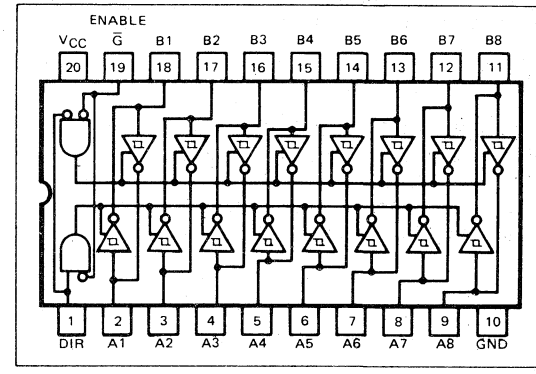
TYPE	LOGIC	OUTPUT
LS640	Inverting	3-State
LS641	Non-Inverting	o.c.
LS642	Inverting	o.c.
LS645	Non-Inverting	3-State

FUNCTION TABLE

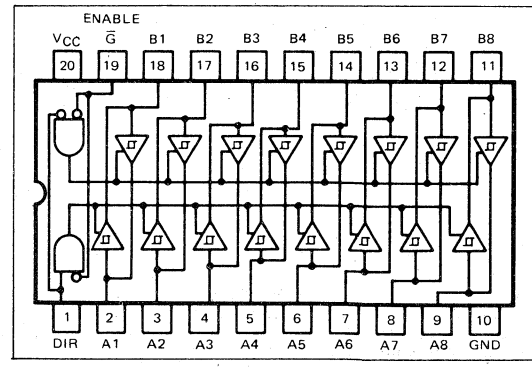
ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION	
		LS640, LS642	LS641, LS645
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

H = high level, L = low level, X = irrelevant

SN54LS640/SN74LS640
SN54LS642/SN74LS642
(TOP VIEW)



SN54LS641/SN74LS641
SN54LS645/SN74LS645
(TOP VIEW)



This is advance information and specifications are subject to change without notice.

SN54LS670/SN74LS670

4×4 REGISTER FILE WITH 3-STATE OUTPUTS

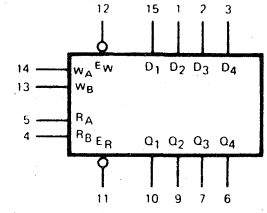
DESCRIPTION – The TTL/MSI SN54LS670/SN74LS670 is a high-speed, low-power 4 x 4 Register File organized as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

The 3-state outputs make it possible to connect up to 128 outputs to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

The SN54LS170/SN74LS170 provides a similar function to this device but it features open-collector outputs.

- **SIMULTANEOUS READ/WRITE OPERATION**
- **EXPANDABLE TO 512 WORDS BY n-BITS**
- **TYPICAL ACCESS TIME OF 20 ns**
- **3-STATE OUTPUTS FOR EXPANSION**
- **TYPICAL POWER DISSIPATION OF 125 mW**

LOGIC SYMBOL



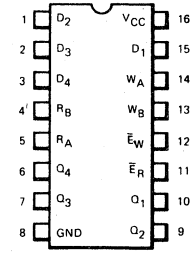
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
D_1-D_4	Data Inputs	0.5 U.L.	0.25 U.L.
W_A, W_B	Write Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_W$	Write Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
R_A, R_B	Read Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_R$	Read Enable (Active LOW) Input	1.5 U.L.	0.75 U.L.
Q_1-Q_4	Outputs (Note b)	65(25) U.L.	5(2.5) U.L.

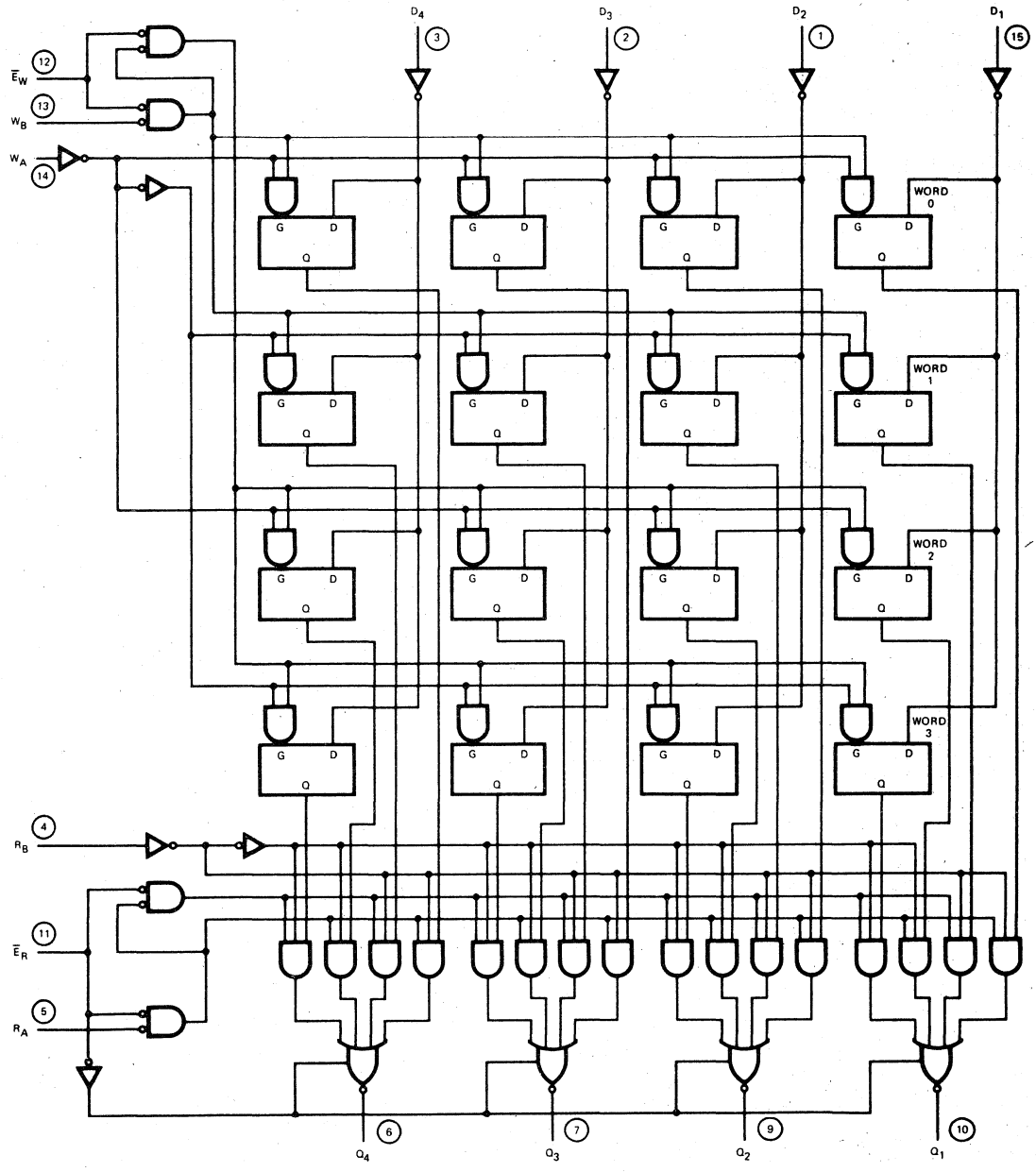
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5.0 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military and 65 U.L. for Commercial Temperature Ranges.

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



○ = Pin Numbers
V_{CC} = Pin 16
GND = Pin 8

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS670X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS670X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTIC OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	I_{OH} = −1.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1		V	I_{OH} = −2.6 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V, V_{IH} = 2 V
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, V_{IH} = 2 V
I_{IH}	Input HIGH Current Any D, R or W				20	μA	V_{CC} = MAX, V_{IN} 2.7 V
	$\overline{E}_W$				40	μA	V_{CC} = MAX, V_{IN} 2.7 V
	$\overline{E}_R$				60	μA	V_{CC} = MAX, V_{IN} 2.7 V
	Any D, R or W				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
	$\overline{E}_W$				0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
	$\overline{E}_R$				0.3	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current Any D, R or W				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	$\overline{E}_W$				−0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	$\overline{E}_R$				−1.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			30	50	mA	V_{CC} = MAX (Note 5)

NOTES:
1. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.
5. Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded and all outputs are open.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay R_A or R_B to Q Outputs			40 45	ns	Fig. 2	$V_{CC} = 5$ V $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, Negative Going $\overline{E}_W$ to Q Outputs			45 50	ns	Fig. 1	$R_L = 2$ kΩ
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs to Q Outputs			45 40	ns	Fig. 1	
t_{PZH}	Enable Time, Negative Going $\overline{E}_R$ to Q Outputs Going HIGH			35	ns	Fig. 4,5	$V_{CC} = 5$ V $C_L = 5.0$ pF $R_L = 2$ kΩ See Page 5-98 for 3-state Waveforms (Figs. 3,4,5)
t_{PZL}	Enable Time, Negative Going $\overline{E}_R$ to Q Outputs Going LOW			40	ns	Fig. 3,5	
t_{PHZ}	Disable Time, Positive Going $\overline{E}_R$ to Q Outputs Off from HIGH			50	ns	Fig. 4,5	
t_{PLZ}	Disable Time, Positive Going $\overline{E}_R$ to Q Outputs Off from LOW			35	ns	Fig. 3,5	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_W	Pulse Width (LOW) for $\overline{E}_W$	25			ns	$V_{CC} = 5$ V Fig. 6 (Note 9)
t_sD (Note 6)	Set-Up Time, Data Inputs with Respect to Positive-Going $\overline{E}_W$	10			ns	
t_hD	Hold Time, Data Inputs with Respect to Positive-Going $\overline{E}_W$	15			ns	
t_sW (Note 8)	Set-Up Time, Write Select Inputs W_A and W_B with Respect to Negative-Going $\overline{E}_W$	15			ns	
t_hW	Hold Time, Write Select Inputs W_A and W_B with Respect to Positive-Going $\overline{E}_W$	5			ns	

NOTES:
6. The Data to Enable Set-up Time is defined as the time required for the logic level to be present at the Data input prior to the enable transition from LOW to HIGH in order for the latch to recognize and store the new data.
7. The Hold Time (t_h) is defined as the minimum time following the enable transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition.
8. The Address to Enable Set-up Time is the time before the HIGH to LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
9. The shaded areas indicate when the input are permitted to change for predictable output performance.

AC WAVEFORMS

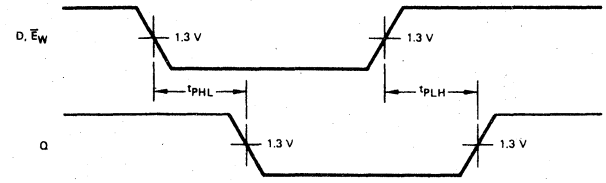


Fig. 1

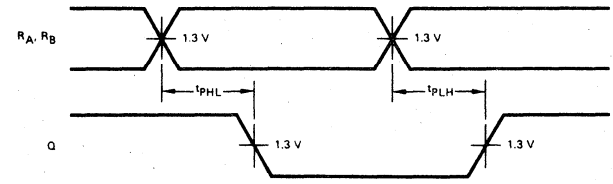


Fig. 2

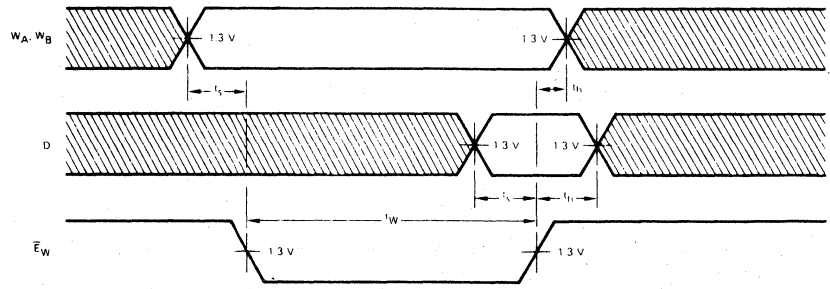
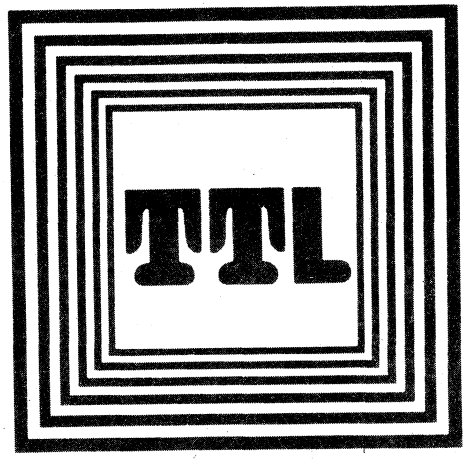


Fig. 6

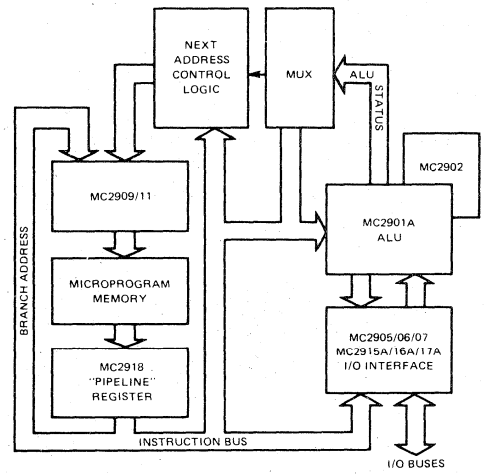
LOW POWER SCHOTTKY



M2900 Processor Family and Memories

M2900 MICROPROCESSOR FAMILY

Speed and versatility are the key attributes of this LSTTL 4-bit slice processor family. System clock frequency is 8.3 to 9.5 MHz. The 4-bit-wide components are structured or "sliced" parallel to the data flow, permitting system expansion to larger word lengths simply by connecting several parts (of each type) in parallel. The family is microprogrammable for efficient emulation of almost any computing machine.



The heart of the system is the MC2901A, a fully expandable 4-bit Arithmetic and Logic Unit (ALU). This device consists of a 16-word by 4-bit two-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The ALU function has look-ahead or ripple carry, three-state outputs, and various status-flag outputs. The look-ahead carry function is performed with an MC2902 Look-Ahead Carry Generator in conjunction with the ALU.

The MC2909 and MC2911 are 4-bit-wide address controllers intended for sequencing through a series of microinstructions contained in the microprogram memory. These controllers have a 4 x 4 stack that allows nesting of subroutines. The system speed can be improved by "pipelining" the contents of the microprogram into MC2918 4-bit registers. The MC2918 can also be used as an address register, condition code register, or for various other register applications.

The I/O interface can be achieved with several different bus transceiver devices. The MC2905/06/07 have high-current sinking, open-collector bus outputs. The driver side has four D-type edge-triggered flip-flops and the receiver side has four D-type latches. The MC2915A/16A/17A are three-state bus output options. These bus transceivers can be used to transfer information from the ALU to the main memory or other bus applications.

Future introductions include the MC2903 Microprocessor Slice, which adds to the features of the MC2901A an expandable register file, bulit-in logic circuitry for multiplication, division, normalization, parity generation, and sign extension. Also coming is the MC2910 Microprogram Controller, which addresses up to 4096 words of microcode. All internal elements of the MC2910 are 12-bits wide.

DEVICE	FUNCTIONS	NO. OF PINS
MC2901A	4-Bit Microprocessor Slice	40
MC2902	Look-Ahead Carry Generator	16
MC2903*	4-Bit Microprocessor Slice (Expandable Register File)	48
MC2905	Quad 2-Input Bus Transceiver with Three-State Receiver (Open-Collector Driver)	24
MC2906	Quad 2-Input Bus Transceiver with Parity (Open-Collector Driver)	24
MC2907	Quad Bus Transceiver with Three-State Receiver and Parity (Open-Collector Driver)	20
MC2909	Microprogram Sequencer, with Individual OR Input for Each Bit	28
MC2910*	12-Bit Microprogram Controller	40
MC2911	Microprogram Sequencer, without OR Inputs	20
MC2915A	Quad 2-Input Three-State Bus Transceiver	24
MC2916A	Quad 2-Input Three-State Bus Transceiver with Parity	24
MC2917A	Quad Three-State Bus Transceiver with Parity	20
MC2918	Quad D Register with Standard and Three-State Outputs	16

*To be introduced.

See Chapter 7 for Packaging.

MOTOROLA Semiconductors

MC2901A

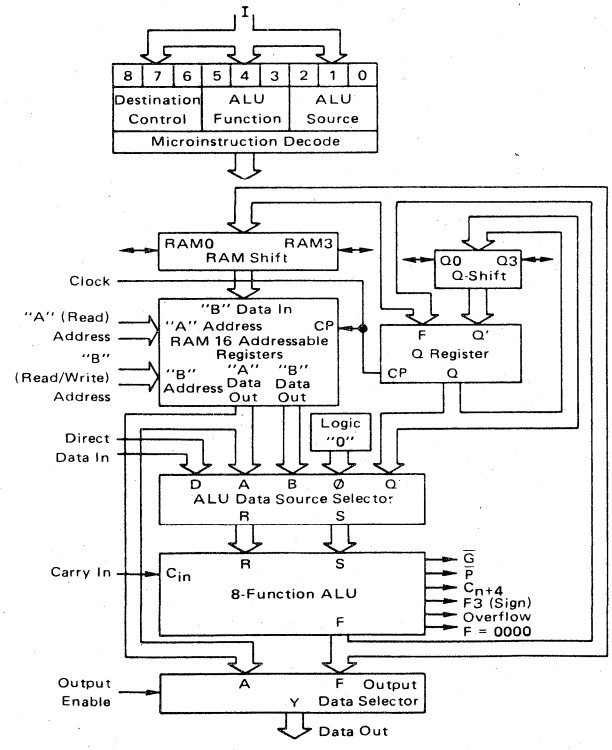
FOUR-BIT BIPOLAR MICROPROCESSOR SLICE

The four-bit bipolar microprocessor slice is designed, as a high-speed cascadable element intended for use in CPUs, peripheral controllers, programmable microprocessors, and numerous other applications. The microinstruction flexibility of the MC2901A will allow efficient emulation of almost any digital computing machine.

The device, as shown in the block diagram below, consists of a sixteen-word by four-bit, two-port RAM; a high-speed ALU; and, the associated shifting, decoding, and multiplexing circuitry. The 9-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look-ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. Advanced low-power Schottky processing is used to fabricate this 40-lead LSI chip.

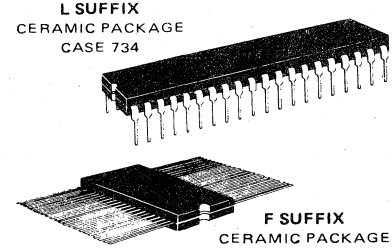
- Plug-in Replacement for MC2901
- 20% to 30% Faster Than MC2901 in Most System Configurations
- Major Speed Improvements in D Input and Carry Paths
- I_{OL} Raised to 20 mA on Y Outputs – 30% More Drive Than MC2901
- I_{CC} Reduced to 190 mA at 125°C – 30% Less Than MC2901
- V_{IL} Raised to 0.8 V Over Full Military Range for Increased Noise Immunity

MICROPROCESSOR SLICE BLOCK DIAGRAM



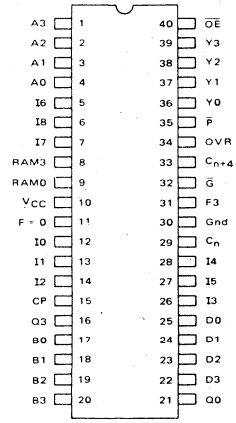
TTL
FOUR-BIT BIPOLAR MICROPROCESSOR SLICE

L SUFFIX
CERAMIC PACKAGE
CASE 734

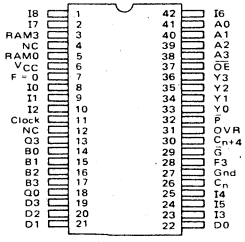


F SUFFIX
CERAMIC PACKAGE
CASE 735

DIP



FLAT PACK



CAUTION

MC2901AFM pinout differs from MC2901FM on pins 4, 11, 12, and 13.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	0°C to +70°C	MC2901ALC
Hermetic DIP	–55°C to +125°C	MC2901ALM
Hermetic Flat Pack	–55°C to +125°C	MC2901AFM

DS 9499

MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} Max
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

MC2901AXC — T_A = 0°C to +70°C, V_{CC} = 5.0 V ± 5% (Commercial), Min = 4.75 V, Max = 5.25 V

MC2901AXM — T_A = −55°C to +125°C, V_{CC} = 5.0 V ± 10% (Military), Min = 4.50 V, Max = 5.50 V

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.6 mA Y0, Y1, Y2, Y3	2.4			Volt
			I_{OH} = −1.0 mA, C_{n+4}	2.4			
			I_{OH} = −800 µA, OVR, $\overline{P}$	2.4			
			I_{OH} = −600 µA, F3	2.4			
			I_{OH} = −600 µA RAM0, 3, Q0, 3	2.4			
			I_{OH} = −1.6 mA, $\overline{G}$	2.4			
I_{CEX}	Output Lekage Current for F = 0 Output	V_{CC} = Min, V_{OH} = 5.5 V, V_{IN} = V_{IH} or V_{IL}				250	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 mA (Commercial) I_{OL} = 16 mA (Military) Y0, Y1, Y2, Y3			0.5	Volt
			I_{OL} = 16 mA, $\overline{G}$, F = 0			0.5	
			I_{OL} = 10 mA, C_{n+4}			0.5	
			I_{OL} = 8.0 mA, OVR, $\overline{P}$			0.5	
			I_{OL} = 6.0 mA, F3 RAM0, 3, Q0, 3			0.5	
V_{IH}	Input High Level	Guaranteed input logical High voltage for all inputs (Note 6)		2.0			Volt
V_{IL}	Input Low Level	Guaranteed input logical Low voltage for all inputs (Note 6)				0.8	Volt
V_I	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA				−1.5	Volt
I_{IL}	Input Low Current	V_{CC} = Max, V_{IN} = 0.5 V	Clock, $\overline{OE}$			−0.36	mA
			A0, A1, A2, A3			−0.36	
			B0, B1, B2, B3			−0.36	
			D0, D1, D2, D3			−0.72	
			I0, I1, I2, I6, I8			−0.36	
			I3, I4, I5, I7			−0.72	
			RAM0, 3, Q0, 3 (Note 4)			−0.8	
			C_n			−3.6	
I_{IH}	Input High Current	V_{CC} = Max, V_{IN} = 2.7 V	Clock, $\overline{OE}$			20	µA
			A0, A1, A2, A3			20	
			B0, B1, B2, B3			20	
			D0, D1, D2, D3			40	
			I0, I1, I2, I6, I8			20	
			I3, I4, I5, I7			40	
			RAM0, 3, Q0, 3 (Note 4)			100	
			C_n			200	
I_I	Input High Current	V_{CC} = Max, V_{IN} = 5.5 V				1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = Max	Y0, Y1, Y2, Y3; V_O = 2.4 V			50	µA
			Y0, Y1, Y2, Y3; V_O = 0.5 V			−50	
			RAM0, 3, Q0, 3; V_O = 2.4 V (Note 4)			100	
			RAM0, 3, Q0, 3; V_O = 0.5 V (Note 4)			−800	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = Max +0.5 V, V_O = 0.5 V	Y0, Y1, Y2, Y3, $\overline{G}$	−30		−85	mA
			C_{n+4}	−30		−85	
			OVR, $\overline{P}$	−30		−85	
			F3	−30		−85	
			RAM0, 3, Q0, 3	−30		−85	
I_{CC}	Power Supply Current (Note 5)	V_{CC} = Max	Commercial		160	265	mA
			Military		160	280	

NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with I678 in a state such that the three-state output is Off.
5. Worst case I_{CC} is at minimum temperature.
6. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Tables 1, 2, and 3 define the timing characteristics of the MC2901A over the operating voltage and temperature range. The tables are divided into three types of parameters: clock characteristics, combinational delays from inputs to outputs, and setup and hold time requirements. The later table defines the time prior to the end of the cycle (i.e., clock low-to-high transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5 V with V_{IL} = 0 V and V_{IH} = 3.0 V. For three-state disable tests, C_L = 5.0 pF and measurement is to 0.5 V change on output voltage level. Input rise and fall times are 1ns/V. All outputs are fully loaded.

TABLE 1 – CYCLE TIME AND CLOCK CHARACTERISTICS

Time	Commercial	Military
Read-Modify-Write Cycle (time from selection of A, B registers to end of cycle)	100 ns	110 ns
Maximum Clock Frequency to Shift Q Register (50% duty cycle) I = 432 or 632	15 MHz	12 MHz
Minimum Clock Low Time	30 ns	30 ns
Minimum Clock High Time	30 ns	30 ns
Minimum Clock Period	100 ns	110 ns

TABLE 2 – COMBINATIONAL PROPAGATION DELAYS

(All in ns, C_L = 50 pF except output disable tests)

	To Output															
	Commercial								Military							
From Input	Y	F3	C_{n+4}	$\overline{G}, \overline{P}$	F = 0 R_L = 470	OVR	Shift Outputs RAM0 RAM3	Shift Outputs Q0 Q3	Y	F3	C_{n+4}	$\overline{G}, \overline{P}$	F = 0 R_L = 470	OVR	Shift Outputs RAM0 RAM3	Shift Outputs Q0 Q3
A, B	80	80	75	65	90	85	95	–	85	85	80	70	100	90	100	–
D (Arithmetic Mode)	45	45	45	35	60	55	65	–	50	50	50	40	65	60	70	–
D (I = X37)(Note 5)	40	40	–	–	55	–	60	–	45	45	–	–	60	–	65	–
C_n	30	35	20	–	50	30	50	–	35	35	25	–	55	35	55	–
I012	55	55	50	45	70	65	75	–	60	60	55	50	75	70	80	–
I345	55	55	55	50	70	65	75	–	60	60	60	55	75	70	80	–
I678	30	–	–	–	–	–	30	30	35	–	–	–	–	–	35	35
$\overline{OE}$ Enable/Disable	35/25	–	–	–	–	–	–	–	40/25	–	–	–	–	–	–	–
A Bypassing ALU (I = 2xx)	45	–	–	–	–	–	–	–	50	–	–	–	–	–	–	–
Clock ↓ (Note 6)	60	60	60	50	75	70	80	30	65	65	65	55	85	75	85	35

TABLE 3 – SET UP AND HOLD TIMES

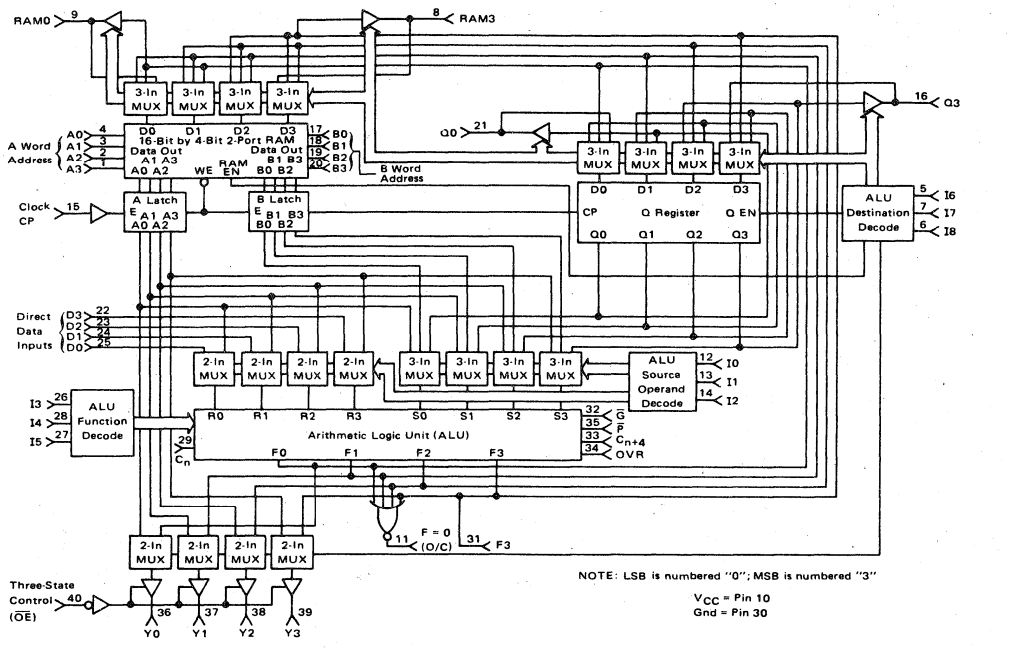
(All in ns. See Note 1)

From Input	Notes	Commercial		Military	
		Setup Time	Hold Time	Setup Time	Hold Time
A, B	2, 4	100	0	110	0
Source	3, 5	$t_{pw}L$ + 30		$t_{pw}L$ + 30	
B Destination	2, 4	$t_{pw}L$ + 15	0	$t_{pw}L$ + 15	0
D (Arithmetic Mode)		70	0	75	0
D (I = X37)(Note 5)		60	0	65	0
C_n		55	0	60	0
I012		80	0	85	0
I345		80	0	85	0
I678	4	$t_{pw}L$ + 30	0	$t_{pw}L$ + 30	0
RAM0, 3, Q0, 3		25	0	25	0

NOTES: 1. See Figure 11. All times relative to clock low-to-high transition.

2. If the B address is used as a source operand, allow for the A, B source setup time. If it is used only for the destination address, use the B Destination setup time.
3. Where two numbers are shown, both must be met.
4. $t_{pw}L$ is the clock low time.
5. D V 0 is the fastest way to load the RAM from the D inputs. This function is obtained with I = 337.
6. Using Q register as source operand in arithmetic mode. Clock is not normally in critical speed path when Q is not a source.

FIGURE 1 – DETAILED MC2901A MICROPROCESSOR BLOCK DIAGRAM



ARCHITECTURE

A detailed block diagram of the bipolar microprogrammable microprocessor structure is shown in Figure 1. The circuit is a four-bit slice cascadable to any number of bits. Therefore, all data paths within the circuit are four bits wide. The two key elements in the Figure 1 block diagram are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

Data in any of the 16 words of the Random Access Memory (RAM) can be read from the A-port of the RAM as controlled by the 4-bit A address field input. Likewise, data in any of the 16 words of the RAM, as defined by the B address field input, can be simultaneously read from the B-port of the RAM. The same code can be applied to the A select field and B select field; in which case, the identical file data will appear at both the RAM A-port and B-port outputs simultaneously.

When enabled by the RAM write enable (RAM-EN), new data is always written into the file (word) defined by the B address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output data (F) if desired. This three-input multiplexer scheme allows the data to be shifted up one bit position, shifted down one bit position, or not shifted in either direction.

The RAM A-port data outputs and RAM B-port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is low. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) can perform three binary arithmetic and five logic operations on the two 4-bit input words, R and S. The R input field is driven from a 2-input multiplexer, while the S input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

Referring to Figure 1, the ALU R-input multiplexer has the RAM A-port and the direct data inputs (D) connected as inputs. Likewise, the ALU S-input multiplexer has the RAM A-port, the RAM B-port and the Q register connected as inputs.

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q, and "0" inputs as source operands to the ALU. These five inputs, when taken two at a time, result in ten possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0, and Q0. It is apparent that AD, AQ, and A0 are somewhat redundant with BD,

BQ, and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only seven completely nonredundant source operand pairs for the ALU. The MC2901 microprocessor implements eight of these pairs. The microinstruction inputs used to select the ALU source operands are the I0, I1, and I2 inputs. The definition of I0, I1, and I2 for the eight source operand combinations are as shown in Figure 2. Also shown is the octal code for each selection.

The two source operands not fully described as yet are the D input and Q input. The D input is the four-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise, this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file intended primarily for multiplication and division routines, but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high-speed arithmetic/logic operator capable of performing three binary arithmetic and five logic functions. The I3, I4, and I5 microinstruction inputs are used to select the ALU function. The definition of these inputs is shown in Figure 3. The octal code is also shown for reference. The normal technique for cascading the ALU of several devices is in a look-ahead carry mode. Carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, are outputs of the device for use with a carry-look-ahead generator such as the MC2902. A carry-out, C_{n+4}, is also generated and is available as an output for use as the carry flag in a status register. Both carry-in (C_n) and carry-out (C_{n+4}) are active high.

The ALU has three other status-oriented outputs. These are F3, F = 0, and overflow (OVR). The F3 output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F3 is noninverted with respect to the sign bit output, Y3. The F = 0 output is used for zero detect. It is an open-collector output and can be wire-OR'ed between microprocessor slices. F = 0 is high when all F outputs are low. The overflow output (OVR) is high when overflow exists. That is, when C_{n+3} and C_{n+4} are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device. It can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available as defined by the I6, I7, and I8 microinstruction inputs. These combinations are shown in Figure 4.

FIGURE 2 – ALU SOURCE OPERAND CONTROL

Micro Code				ALU Source Operands	
Pin 14 I2	Pin 13 I1	Pin 12 I0	Octal Code	R	S
L	L	L	0	A	Q
L	L	H	1	A	B
L	H	L	2	O	Q
L	H	H	3	O	B
H	L	L	4	O	A
H	L	H	5	D	A
H	H	L	6	D	Q
H	H	H	7	D	O

FIGURE 3 – ALU FUNCTION CONTROL

Micro Code				ALU	
Pin 27 I5	Pin 28 I4	Pin 26 I3	Octal Code	Function	Symbol
L	L	L	0	R Plus S	R + S
L	L	H	1	S Minus R	S – R
L	H	L	2	R Minus S	R – S
L	H	H	3	R OR S	$R \vee S$
H	L	L	4	R AND S	$R \wedge S$
H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
H	H	L	6	R EX-OR S	$R \forall S$
H	H	H	7	R EX-NOR S	$\overline{R \forall S}$

FIGURE 4 – ALU DESTINATION CONTROL

Micro Code				RAM Function		Q-Reg Function		Y	RAM Shifter		Q Shifter	
Pin 6 I8	Pin 7 I7	Pin 5 I6	Octal Code	Shift	Load	Shift	Load	Output	RAM0	RAM3	Q0	Q3
L	L	L	0	X	None	None	F → Q	F	X	X	X	X
L	L	H	1	X	None	X	None	F	X	X	X	X
L	H	L	2	None	F → B	X	None	A	X	X	X	X
L	H	H	3	None	F → B	X	None	F	X	X	X	X
H	L	L	4	Down	F/2 → B	Down	Q/2 → Q	F	F0	IN3	Q0	IN3
H	L	H	5	Down	F/2 → B	X	None	F	F0	IN3	Q0	X
H	H	L	6	Up	2F → B	Up	2Q → Q	F	IN0	F3	IN0	Q3
H	H	H	7	Up	2F → B	X	None	F	IN0	F3	X	Q3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
B = Register Addressed by B inputs.
Up is toward MSB; Down is toward LSB.

The four-bit data output field (Y) features three-state outputs and can be directly bus-organized. An output control ($\overline{OE}$) is used to enable the three-state outputs. When $\overline{OE}$ is high, the Y outputs are in the high-impedance state.

A two-input multiplexer is also used at the data output such that either the A-port of the RAM or the ALU outputs (F) are selected at the device Y outputs. This selection is controlled by the I6, I7, and I8 microinstruction inputs. Refer to Figure 4 for the selected output for each microinstruction code combination.

As was discussed previously, the RAM inputs are driven from a three-input multiplexer. This allows the ALU outputs to be entered nonshifted, shifted up one position (X2) or shifted down one position (÷2). The shifter has two ports: one is labeled RAM0 and the other is labeled RAM3. Both of these ports consist of a buffer-driver with a three-state output and an input to the multiplexer. Thus, in the shift up mode, the RAM3 buffer is enabled and the RAM0 multiplexer input is enabled. Likewise, in the shift down mode, the RAM0 buffer and RAM3 input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the multiplexer inputs are not selected. This shifter is controlled from the I6, I7, and I8 microinstruction inputs as defined in Figure 4.

Similarly, the Q register is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter also has two ports: one is labeled Q0 and the other is Q3. The operation of these two ports is similar to the RAM shifter and is also controlled from I6, I7, and I8 as shown in Figure 4.

The clock input to the MC2901A controls the RAM, the Q register, and the A and B data latches. When enabled, data is clocked into the Q register on the low-to-high transition of the clock. When the clock input is high, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is low, the latches are closed and will retain the last data entered. If the RAM-EN is enabled, new data will be written into the RAM file (word) defined by the B address field when the clock input is low.

SOURCE OPERANDS AND ALU FUNCTIONS

There are eight source operand pairs available to the ALU as selected by the I0, I1, and I2 instruction inputs. The ALU can perform eight functions: five logic and three arithmetic. The I3, I4, and I5 instruction inputs control this function selection. The carry input, C_n, also affects the ALU results when in the arithmetic mode. The C_n input has no effect in the logic mode. When I0 through I5 and C_n are viewed together, the matrix of Figure 5 results. This matrix fully defines the ALU/source operands function for each state.

The ALU functions can also be examined on a "task" basis, i.e., add, subtract, AND, OR, etc. In the arithmetic mode, the carry will affect the function performed while in the logic mode, the carry will have no bearing on the ALU output. Figure 6 defines the various logic operations that the MC2901A can perform and Figure 7 shows the arithmetic functions of the device. Both carry-in low (C_n = 0) and carry-in high (C_n = 1) are defined in these operations.

FIGURE 5 – SOURCE OPERAND AND ALU FUNCTION MATRIX

		I210 Octal							
		0	1	2	3	4	5	6	7
I543 Octal	ALU Function	ALU Source							
		A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	C_n = L R Plus S C_n = H	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C_n = L S Minus R C_n = H	Q – A – 1 Q – A	B – A – 1 B – A	Q – 1 Q	B – 1 B	A – 1 A	A – D – 1 A – D	Q – D – 1 Q – D	–D – 1 –D
2	C_n = L R Minus S C_n = H	A – Q – 1 A – Q	A – B – 1 A – B	–Q – 1 –Q	–B – 1 –B	–A – 1 –A	D – A – 1 D – A	D – Q – 1 D – Q	D – 1 D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ∀ Q	A ∀ B	Q	B	A	D ∀ A	D ∀ Q	D
7	R EX-NOR S	$\overline{A \forall Q}$	$\overline{A \forall B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \forall A}$	$\overline{D \forall Q}$	$\overline{D}$

+ = Plus; – = Minus; ∨ = OR; ∧ = AND; ∀ = EX-OR

LOGIC FUNCTIONS FOR G, P, C_{n+4}, AND OVR

The four signals—G, P, C_{n+4}, and OVR—are designed to indicate carry and overflow conditions when the MC2901A is in the add or subtract mode. Figure 8 indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Figure 2.

FIGURE 6 – ALU LOGIC MODE FUNCTIONS
(C_n Irrelevant)

Octal I543, I210	Group	Function
4 0	AND	$A \wedge Q$
4 1		$A \wedge B$
4 5		$D \wedge A$
4 6		$D \wedge Q$
3 0	OR	$A \vee Q$
3 1		$A \vee B$
3 5		$D \vee A$
3 6		$D \vee Q$
6 0	EX-OR	$A \forall Q$
6 1		$A \forall B$
6 5		$D \forall A$
6 6		$D \forall Q$
7 0	EX-NOR	$\overline{A \forall Q}$
7 1		$\overline{A \forall B}$
7 5		$\overline{D \forall A}$
7 6		$\overline{D \forall Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A} \wedge Q$
5 1		$\overline{A} \wedge B$
5 5		$\overline{D} \wedge A$
5 6		$\overline{D} \wedge Q$

Definitions (+ = OR)

$P0 = R0 + S0$ $\quad G0 = R0S0$

$P1 = R1 + S1$ $\quad G1 = R1S1$

$P2 = R2 + S2$ $\quad G2 = R2S2$

$P3 = R3 + S3$ $\quad G3 = R3S3$

$C4 = G3 + P3G2 + P3P2G1 + P3P2P1G0 + P3P2P1P0C_n$

$C3 = G2 + P2G1 + P2P1G0 + P2\,P1P0C_n$

FIGURE 7 – ALU ARITHMETIC MODE FUNCTIONS

Octal	C_n = 0 (Low)		C_n = 1 (High)	
I543, I210	Group	Function	Group	Function
0 0	ADD	A + Q	ADD plus one	A + Q + 1
0 1		A + B		A + B + 1
0 5		D + A		D + A + 1
0 6		D + Q		D + Q + 1
0 2	PASS	Q	Increment	Q + 1
0 3		B		B + 1
0 4		A		A + 1
0 7		D		D + 1
1 2	Decrement	Q – 1	PASS	Q
1 3		B – 1		B
1 4		A – 1		A
2 7		D – 1		D
2 2	1's Comp	–Q – 1	2's Comp (Negate)	–Q
2 3		–B – 1		–B
2 4		–A – 1		–A
1 7		–D – 1		–D
1 0	Subtract (1's Comp)	Q – A – 1	Subtract (2's Comp)	Q – A
1 1		B – A – 1		B – A
1 5		A – D – 1		A – D
1 6		Q – D – 1		Q – D
2 0		A – Q – 1		A – Q
2 1		A – B – 1		A – B
2 5		D – A – 1		D – A
2 6		D – Q – 1		D – Q

FIGURE 8 – LOGIC FUNCTIONS

I543	Function	Pin 35 $\overline{P}$	Pin 32 $\overline{G}$	Pin 33 C_{n+4}	Pin 34 OVR
0	R + S	$\overline{P3P2P1P0}$	$\overline{G3 + P3G2 + P3P2G1 + P3P2P1G0}$	C4	C3 ∀ C4
1	S – R	Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions			
2	R – S	Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions			
3	R ∨ S	Low	P3P2P1P0	$\overline{P3P2P1P0} + C_n$	$\overline{P3P2P1P0} + C_n$
4	R ∧ S	Low	$\overline{G3 + G2 + G1 + G0}$	$G3 + G2 + G1 + G0 + C_n$	$G3 + G2 + G1 + G0 + C_n$
5	$\overline{R} \wedge S$	Low	Same as R ∧ S equations, but substitute $\overline{R_i}$ for R_i in definitions		
6	R ∀ S	Same as $\overline{R \forall S}$, but substitute $\overline{R_i}$ for R_i in definitions			
7	$\overline{R \forall S}$	G3 + G2 + G1 + G0	G3 + P3G2 + P3P2G1 + P3P2P1P0	$\overline{G3 + P3G2 + P3P2G1 + P3P2P1P0(G0 + \overline{C_n})}$	See Note

+ = OR

NOTE: $[\overline{P2} + \overline{G2}\overline{P1} + \overline{G2}\overline{G1}\overline{P0} + \overline{G2}\overline{G1}\overline{G0}C_n] \forall [\overline{P3} + \overline{G3}\overline{P2} + \overline{G3}\overline{G2}\overline{P1} + \overline{G3}\overline{G2}\overline{G1}\overline{P0} + \overline{G3}\overline{G2}\overline{G1}\overline{G0}C_n]$

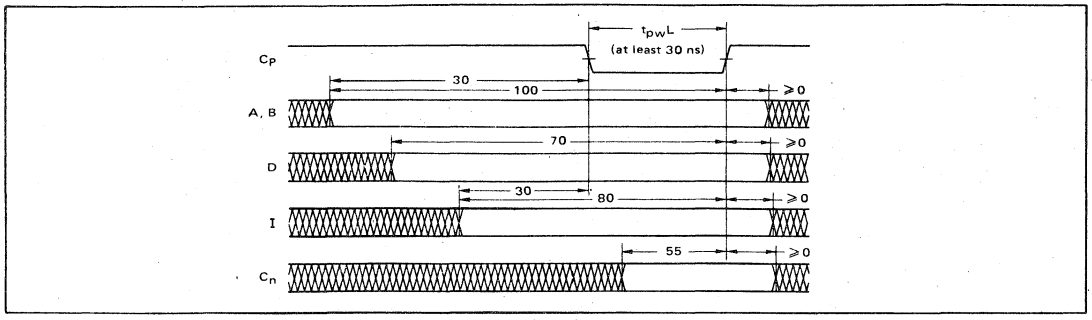
SETUP AND HOLD TIMES

(Minimum Cycles from Each Input)

Setup and hold times are defined relative to the clock low-to-high edge. Inputs must be steady at all times from the setup time prior to the clock, until the hold time after the clock. The setup times allow sufficient time to perform the correct operation on the correct data so that the correct ALU data can be written into one of the registers.

FIGURE 9 – MINIMUM CYCLE TIMES FROM INPUTS

(Numbers shown are minimum data stable times for MC2901ALC, in ns. See Table 3 for detailed information.)



PIN DEFINITIONS

A0–3 The four address inputs to the register stack used to select one register whose contents are displayed through the A-port.

B0–3 The four address inputs to the register stack used to select one register whose contents are displayed through the B-port and into which new data can be written when the clock goes low.

I0–8 The nine instruction control lines to the MC2901, used to determine what data sources will be applied to the ALU (I012), what function the ALU will perform (I345), and what data is to be deposited in the Q-register or the register stack (I678).

Q3 RAM3 A shift line at the MSB of the Q register (Q3) and the register stack (RAM3). Electrically, these lines are three-state outputs connected to TTL inputs internal to the MC2901A. When the destination code on I678 indicates an up shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the Q3 pin and the MSB of the ALU output is available on the RAM3 pin. Otherwise, the three-state outputs are off (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).

Q0 RAM0 Shift lines like Q3 and RAM3, but at the LSB of the Q-register and RAM. These pins are tied to the Q3 and RAM3 pins of the adjacent device to transfer data between devices for up and down shifts of the Q register and ALU data.

D0–3 Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the MC2901A. D0 is the LSB.

Y0–3 The four data outputs of the MC2901A. These are three-state output lines. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code I678.

$\overline{OE}$ $\overline{\text{Output Enable}}$. When $\overline{OE}$ is high, the Y outputs are off; when $\overline{OE}$ is low, the Y outputs are active (high or low).

$\overline{P}$, $\overline{G}$ The carry generate and propagate outputs of the MC2901A's ALU. These signals are used with the MC2902 for carry-look-ahead. See Figure 8 for the logic equations.

OVR Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit. See Figure 8 for logic equation.

F = 0 This is an open collector output which goes high (off) if the data on the four ALU outputs F0–3 are all low. In positive logic, it indicates the result of an ALU operation is zero.

C_n The carry-in to the MC2901A's ALU.

C_{n+4} The carry-out of the MC2901A's ALU. See Figure 8 for equations.

CP The clock to the MC2901A. The Q register and register stack outputs change on the clock low-to-high transition. The clock low time is internally the write enable to the 16 X 4 RAM which comprises the "master" latches of the register stack. While the clock is low, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.

FIGURE 10 – MC2901A INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

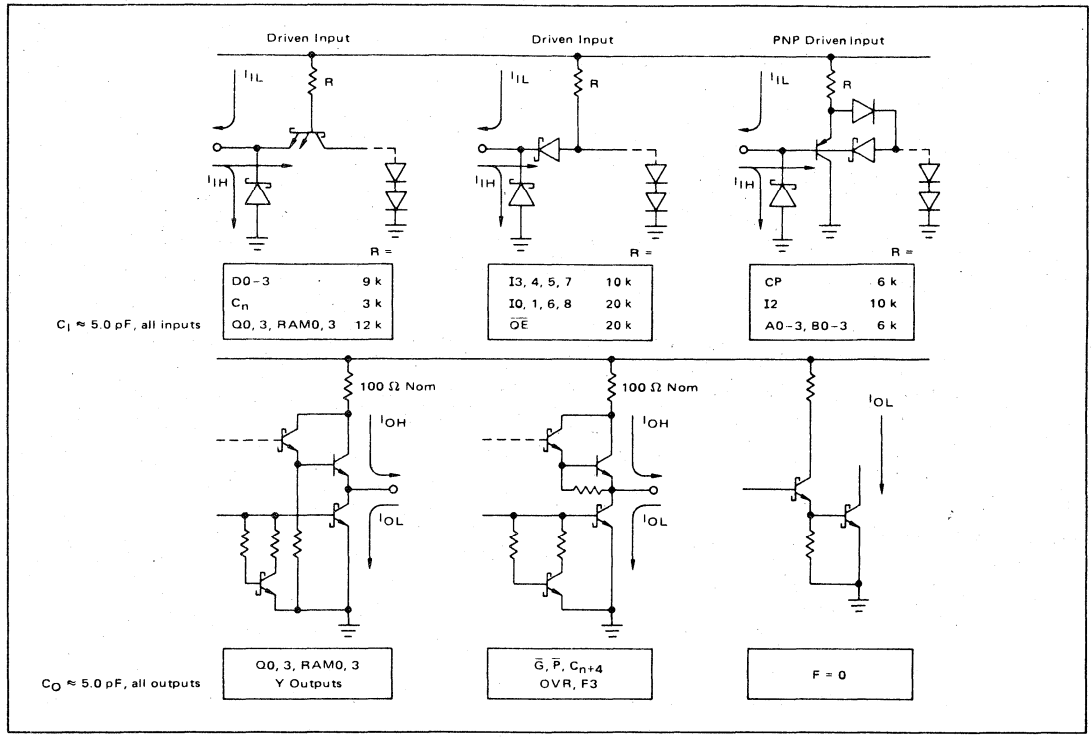
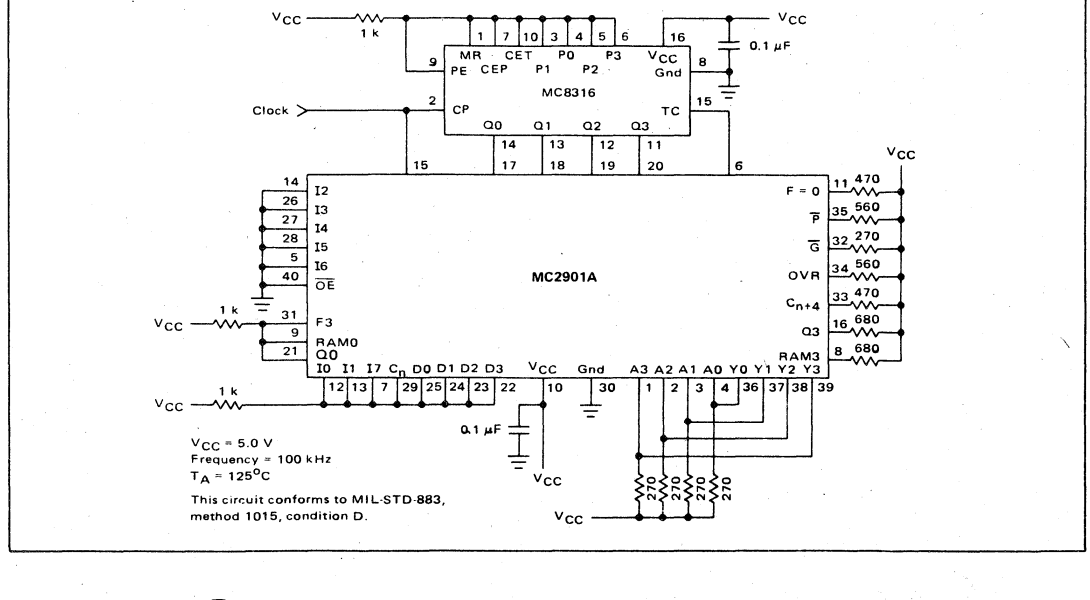
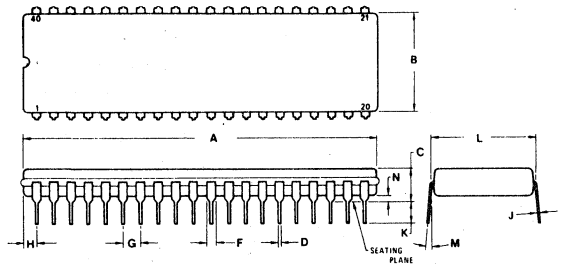


FIGURE 11 – MC2901A BURN-IN CIRCUIT



PACKAGE DIMENSIONS

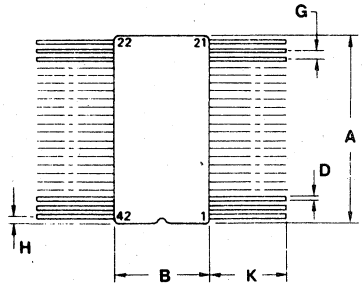


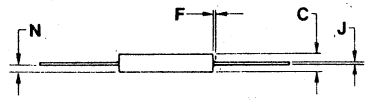
NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	52.32	53.09	2.060	2.090
B	12.70	13.72	0.500	0.540
C	5.08	5.84	0.200	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
H	2.03	2.41	0.080	0.095
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

L SUFFIX
CERAMIC PACKAGE
CASE 734

F SUFFIX
CERAMIC PACKAGE
CASE 735





	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	26.92	27.60	1.060	1.090
B	13.72	14.22	0.540	0.560
C	2.41	3.18	0.095	0.125
D	0.43	0.53	0.017	0.023
F	–	0.38	–	0.015
G	1.27 BSC		0.050 BSC	
H	0.89	1.14	0.035	0.045
J	0.20	0.30	0.008	0.012
K	–	11.94	–	0.470
N	–	1.27	–	0.050

NOTE:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

MC2902

High-Speed Look-Ahead Carry Generator

Distinctive Characteristics

- Provides look-ahead carries across a group of four MC2901 microprocessor ALUs
- Capability of multi-level look-ahead for high-speed arithmetic operation over large word lengths.
- Typical carry propagation delay of 6.0 ns

FUNCTIONAL DESCRIPTION

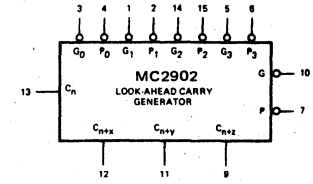
The MC2902 is a high-speed, look-ahead carry generator which accepts up to four pairs of carry propagate and carry generate signals and a carry input and provides anticipated carries across four groups of binary ALUs. The device also has carry propagate and carry generate outputs which may be used for further levels of look-ahead.

The MC2902 is generally used with the bipolar microprocessor unit to provide look-ahead over word lengths of more than four bits. The look-ahead carry generator can be used with binary ALUs in an active LOW or active HIGH input operand mode by reinterpreting the carry functions. The connections to and from the ALU to the look-ahead carry generator are identical in both cases.

The logic equations provided at the outputs are:

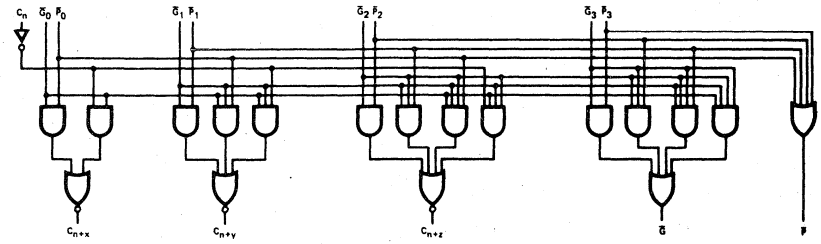
$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$G = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$$
$$P = P_3P_2P_1P_0$$

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

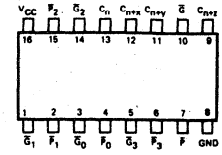
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	MC2902PC
Hermetic DIP	0°C to +70°C	MC2902LC
Dice	0°C to +70°C	MCC2902C
Hermetic DIP	-55°C to +125°C	MC2902LM
Hermetic Flat Pack	-55°C to +125°C	MC2902FM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

MC2902XC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
MC2902XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.50V MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8mA V_{IN} = V_{IH} or V_{IL}		2.4	3.0		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −12mA				−1.5	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	C_n			−3.2	mA
			$\overline{P}_3$			−4.8	
			$\overline{P}_2$			−6.4	
			$\overline{P}_0, \overline{P}_1, \overline{G}_3$			−8.0	
			$\overline{G}_0, \overline{G}_2$			−14.4	
			$\overline{G}_1$			−16	
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V	C_n			80	µA
			$\overline{P}_3$			120	
			$\overline{P}_2$			160	
			$\overline{P}_0, \overline{P}_1, \overline{G}_3$			200	
			$\overline{G}_0, \overline{G}_2$			360	
			$\overline{G}_1$			400	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short-Circuit (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. All Outputs LOW	MIL		62	99	mA
			COM'L		58	94	
		V_{CC} = MAX. All Ouputs HIGH	MIL		37		mA
			COM'L		35		

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current X Input Load Factor (see Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS V_{CC} = 5.0V, T_A = 25°C, C_L = 15pF, R_L = 400Ω

Parameter	From (Input)	To (Output)	Test Figure	Test Conditions	Min	Typ	Max	Units
t_{PLH}	C_n	C_{n+j}	2	$\overline{P}_0 = \overline{P}_i = \overline{P}_2 = 0$ V $\overline{G}_0 = \overline{G}_i = \overline{G}_2 = 4.5$ V		11	14	ns
t_{PHL}						11	14	
t_{PLH}	$\overline{P}_i$	C_{n+j}	3	$\overline{P}_i = 0$ V (j > i) $C_n = \overline{G}_0 = \overline{G}_i = \overline{G}_2 = 4.5$ V		6.0	8.0	ns
t_{PHL}						6.0	8.0	
t_{PLH}	$\overline{G}_i$	C_{n+j}	3	$\overline{G}_i = 0$ V (j > i) $C_n = \overline{P}_0 = \overline{P}_i = \overline{P}_2 = 4.5$ V		8.0	10	ns
t_{PHL}						8.0	10	
t_{PLH}	$\overline{P}_i$	$\overline{G}$ or $\overline{P}$	2	$\overline{P}_i = 0$ V (j > i) $C_n = \overline{G}_0 = \overline{G}_i = \overline{G}_2 = 4.5$ V		11	14	ns
t_{PHL}						11	14	
t_{PLH}	$\overline{G}_i$	$\overline{G}$ or $\overline{P}$	2	$\overline{G}_i = 0$ V (j > i) $C_n = \overline{P}_0 = \overline{P}_i = \overline{P}_2 = 4.5$ V		12	14	ns
t_{PHL}						12	14	

DEFINITION OF FUNCTIONAL TERMS

C_n Carry-in. The carry-in input to the look-ahead generator. Also the carry-in input to the nth MC2901 microprocessor ALU input.

C_{n+j} Carry-out. (j = x, y, z). The carry-out output to be used at the carry-in inputs of the n+1, n+2, and n+3 microprocessor ALU slices.

G_i P_i Generate and propagate inputs, respectively (i = 0, 1, 2, 3). The carry generate and carry propagate inputs from the n, n+1, n+2 and n+3 microprocessor ALU slices.

G, P Generate and propagate outputs, respectively. The carry generate and carry propagate outputs that can be used with the next higher level of carry look-ahead if used.

TRUTH TABLE

Inputs									Outputs			
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+z}	C_{n+y}	C_{n+x}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	H	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	X	X	H	X					L		
X	X	X	X	L	X	L					H		
X	X	X	L	X	L	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	H	H	H				H	
	X		X	X	H	H	H	X				H	
	X		X	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				H	
	X		X	X	L	X	X	L				H	
	X		X	L	X	L	X	L				H	
	L		X	L	X	L	X	L				H	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

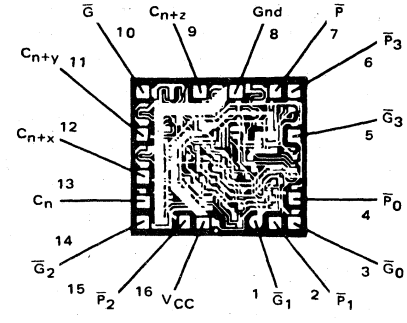
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LOADING RULES (In Unit Loads)

Input/Output	Pin No.	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{G}_1$	1	8.0	–	–
$\overline{P}_1$	2	4.0	–	–
$\overline{G}_0$	3	7.2	–	–
$\overline{P}_0$	4	4.0	–	–
$\overline{G}_3$	5	4.0	–	–
$\overline{P}_3$	6	2.4	–	–
$\overline{P}$	7	–	16	8
GND	8	–	–	–
C_{n+z}	9	–	16	8
$\overline{G}$	10	–	16	8
C_{n+y}	11	–	16	8
C_{n+x}	12	–	16	8
C_n	13	1.6	–	–
$\overline{G}_2$	14	7.2	–	–
$\overline{P}_2$	15	3.2	–	–
V_{CC}	16	–	–	–

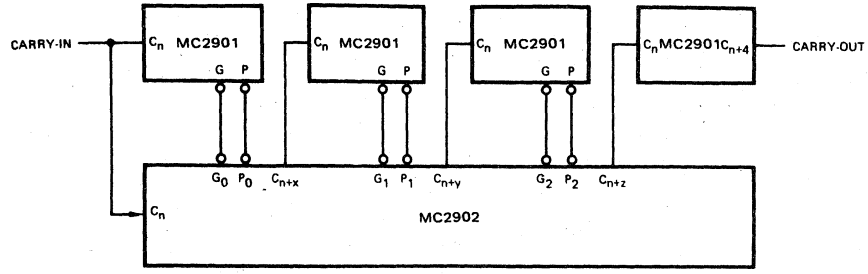
A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

Metallization and Pad Layout

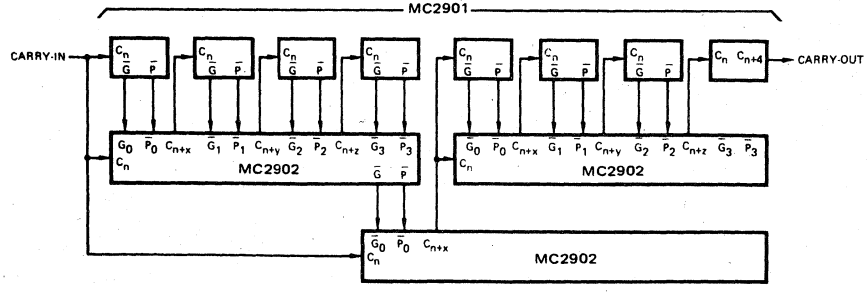


DIE SIZE 0.062" X 0.055"

APPLICATIONS



16-BIT CARRY LOOK-AHEAD CONNECTION.



32-BIT ALU, THREE LEVEL CARRY LOOK-AHEAD.

MOTOROLA Semiconductors

MC2903

Product Preview

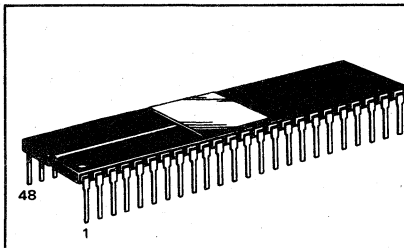
TTL

FOUR-BIT BIPOLAR MICROPROCESSOR SLICE

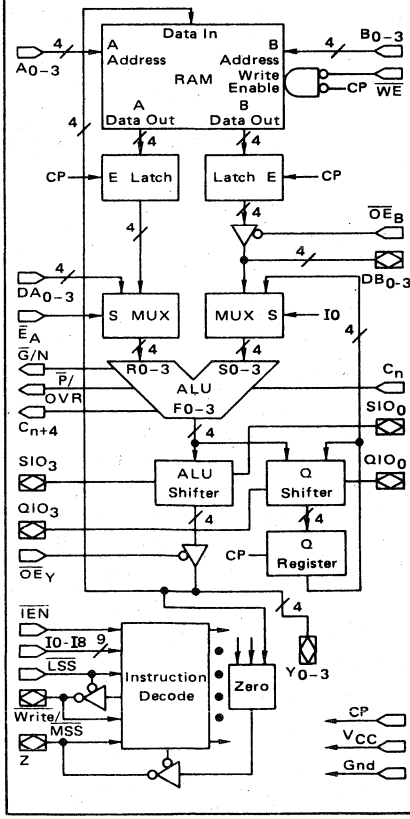
FOUR-BIT BIPOLAR MICROPROCESSOR SLICE

The MC2903 is a four-bit expandable bipolar microprocessor slice. The MC2903 performs all functions performed by the industry standard MC2901A and, in addition, provides a number of significant enhancements that are especially useful in arithmetic-oriented processors. Infinitely expandable memory and three-port, three-address architecture are provided by the MC2903. In addition to its complete arithmetic and logic instruction set, the MC2903 provides a special set of instructions which facilitate the implementation of multiplication, division, normalization, and other previously time-consuming operations. The MC2903 is supplied in a 48 pin dual in-line package.

- **Built-in Parity Generation Circuitry**
  The MC2903 can supply parity across the entire ALU output for use in error detection and CRC code generation.
- **Built-in Sign Extension Circuitry**
  To facilitate operation on different length two's complement numbers, the MC2903 provides the capability to extend the sign at any slice boundary.
- **Expandable Register File**
  Like the MC2901A, the MC2903 contains 16 internal working registers arranged in a two-address architecture. But the MC2903 includes the necessary "hooks" to expand the register file externally to any number of registers.
- **Built-in Multiplication Logic**
  Performing multiplication with the MC2901A requires a few external gates—these gates are contained on-chip in the MC2903. Three special instructions are used for unsigned multiplication, two's complement multiplication, and the last cycle of a two's complement multiplication.
- **Built-in Division Logic**
  The MC2903 contains all logic and interconnects for execution of a non-restoring, multiple-length division with correction of the quotient.
- **Built-in Normalization Logic**
  The MC2903 can simultaneously shift the Q Register and count in a working register. Thus, the mantissa and exponent of a floating point number can be developed using a single microcycle per shift. Status flags indicate when the operation is complete.



BLOCK DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	0°C to +70°C	MC2903LC
Hermetic DIP	-55°C to +125°C	MC2903LM

This is advance information and specifications are subject to change without notice.

ARCHITECTURE OF THE MC2903

The MC2903 is a high performance, cascadable, 4-bit bipolar microprocessor slice designed for use in CPUs, peripheral controllers, microprogrammable machines, and numerous other applications. The microinstruction flexibility of the MC2903 allows the efficient emulation of almost any digital computing machine. The 9-bit microinstruction selects the ALU sources, function, and destination. The MC2903 is cascadable with full look-ahead or ripple carry, has three-state outputs, and provides various ALU status flag outputs. Advanced low-power Schottky processing is used to fabricate this 48-pin LSI circuit.

All data paths within the device are four bits wide. As shown in the block diagram, the device consists of a 16-word by 4-bit, two-port RAM with latches on both output ports, a high-performance ALU and shifter, a multipurpose Q Register with shifter input, and a 9-bit instruction decoder.

Two-Port RAM

Any two RAM words addressed at the A and B address ports can be read simultaneously at the respective RAM A and B output ports. Identical data appear at the two output ports when the same address is applied to both address ports. The latches at the RAM output ports are transparent when the clock input, CP, is High and they hold the RAM output data when CP is Low. Under control of the $\overline{OE}_B$ three-state output enable, RAM data can be read directly at the MC2903 DB I/O port.

External data at the MC2903 Y I/O port can be written directly into the RAM, or ALU shifter output data can be enabled onto the Y I/O port and entered into the RAM. Data is written into the RAM at the B address when the write enable input, $\overline{WE}$, is Low and the clock input, CP, is Low.

Arithmetic Logic Unit

The MC2903 high performance ALU can perform seven arithmetic and nine logic operations on two 4-bit operands. Multiplexers at the ALU inputs provide the capability to select various pairs of ALU source operands. The E_A input selects either the DA external data input or RAM output port A for use as one ALU operand and the OE_B and $I0$ inputs select RAM output port B, DB external data input, or the Q Register content for use as the second ALU operand. Also, during some ALU operations, zeroes are forced at the ALU operand inputs. Thus, the MC2903 ALU can operate on data from two external sources, from an internal and external source, or from two internal sources. Table 1 shows all possible pairs of ALU source operands as a function of the E_A, OE_B, and $I0$ inputs.

When instruction bits $I4$, $I3$, $I2$, $I1$, and $I0$ are Low, the MC2903 executes special functions. Table 4 defines these special functions and the operation which the ALU performs for each. When the MC2903 executes instructions other than the nine special functions, the ALU operation is determined by instruction bits $I4$, $I3$, $I2$, and $I1$. Table 2 defines the ALU operation as a function of these four instruction bits.

TABLE 1 – ALU OPERAND SOURCES

$\overline{E_A}$	I0	$\overline{OE_B}$	ALU Operand R	ALU Operand B
L	L	L	RAM Output A	RAM Output B
L	L	H	RAM Output A	DB_{0-3}
L	H	X	RAM Output A	Q Register
H	L	L	DA_{0-3}	RAM Output B
H	L	H	DA_{0-3}	DB_{0-3}
H	H	X	DA_{0-3}	Q Register

L = Low, H = High, X = don't care.

TABLE 2 – ALU FUNCTIONS

I4	I3	I2	I1	Hex Code	ALU Functions	
L	L	L	L	0	I0 = L	Special Functions
					I0 = H	F_i = High
L	L	L	H	1	F = S minus R minus 1 plus C_n	
L	L	H	L	2	F = R minus S minus 1 plus C_n	
L	L	H	H	3	F = R plus S plus C_n	
L	H	L	L	4	F = S plus C_n	
L	H	L	H	5	F = $\overline{S}$ plus C_n	
L	H	H	L	6	F = R plus C_n	
L	H	H	H	7	F = $\overline{R}$ plus C_n	
H	L	L	L	8	F_i = Low	
H	L	L	H	9	$F_i = \overline{R}_i$ AND S_i	
H	L	H	L	A	$F_i = R_i$ EXCLUSIVE NOR S_i	
H	L	H	H	B	$F_i = R_i$ EXCLUSIVE OR S_i	
H	H	L	L	C	$F_i = R_i$ AND S_i	
H	H	L	H	D	$F_i = R_i$ NOR S_i	
H	H	H	L	E	$F_i = R_i$ NAND S_i	
H	H	H	H	F	$F_i = R_i$ OR S_i	

L = Low, H = High, i = 0 to 3.

MC2903s may be cascaded in either a ripple carry or lookahead carry fashion. When a number of MC2903s are cascaded, each slice must be programmed to be a most significant slice (MSS), intermediate slice (IS), or least significant slice (LSS) of the array. The carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, signals required for a lookahead carry scheme are generated by the MC2903 and are available as outputs of the least signficant and intermediate slices.

The MC2903 also generates a carry-out signal, C_{n+4}, which is generally available as an output of each slice. Both the carry-in, C_n, and carry-out, C_{n+4}, signals are

active High. The ALU generates two other status outputs. These are negative, N, and overflow, OVR. The N output is generally the most significant (sign) bit of the ALU output and can be used to determine positive or negative results. The OVR output indicates that the arithmetic operation being performed exceeds the available two's complement number range. The N and OVR signals are available as outputs of the most significant slice. Thus, the multipurpose $\overline{G}$/N and $\overline{P}$/OVR outputs indicate $\overline{G}$ and $\overline{P}$ at the least significant and intermediate slices, and sign and overflow at the most significant slice. To some extent, the meaning of the C_{n+4}, $\overline{P}$/OVR, and $\overline{G}$/N signals vary with the ALU function being performed. Refer to Table 5 for an exact definition of these four signals as a function of the MC2903 instruction.

ALU Shifter

Under instruction control, the ALU shifter passes the ALU output (F) non-shifted, shifts it up one bit position (2F), or shifts it down one bit position (F/2). Both arithmetic and logical shift operations are possible. An arithmetic shift operation shifts data around the most significant (sign) bit position of the most significant slice, and a logical shift operation shifts data through this bit position (see Figure A). SIO_0 and SIO_3 are bidirectional serial shift inputs/outputs. During a shift-up operation, SIO_0 is generally a serial shift input and SIO_3 a serial shift output. During a shift-down operation, SIO_3 is generally a serial shift input and SIO_0 a serial shift output.

To some extent, the meaning of the SIO_0 and SIO_3 signals is instruction dependent. Refer to Tables 3 and 4 for an exact definiction of these pins.

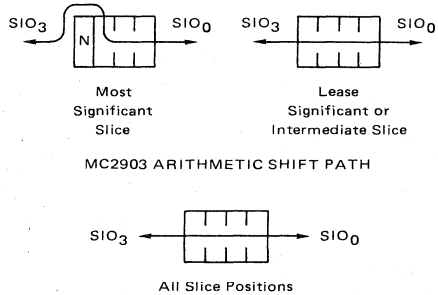


FIGURE A

The ALU shifter also provides the capability to sign extend at slice boundaries. Under instruction control, the SIO_0 (sign) input can be extended through Y0, Y1, Y2, Y3, and propagated to the SIO_3 output.

A cascadable, 5-bit parity generator/checker is designed into the MC2903 ALU shifter and provides ALU error detection capability. Parity for the F0, F1, F2, F3 ALU outputs and SIO_3 input is generated and, under instruction control, is made available at the SIO_0 output. Refer to the MC2903 applications section for a more detailed description of the MC2903 sign extension and parity generation/checking capability.

The instruction inputs determine the ALU shifter operation. Table 4 defines the special functions and the operation the ALU shifter performs for each. When the MC2903 executes instructions other than the nine special functions, the ALU shifter operation is determined by instruction bits I8, I7, I6, I5. Table 3 defines the ALU shifter operations as a function of these four bits.

Q Register

The Q Register is an auxiliary 4-bit register which is clocked on the Low-to-High transition of the CP input. It is intended primarily for use in multiplication and division operations; however, it can also be used as an accumulator or holding register for some applications. The ALU output, F, can be loaded into the Q Register, and/or the Q Register can be selected as the source for the ALU S operand. The shifter at the input to the Q Register provides the capability to shift the Q Register contents up one bit position (2Q) or down one bit position (Q/2). Only logical shifts are performed. QIO_0 and QIO_3 are bidirectional shift serial inputs/outputs. During a Q Register shift-up operation, QIO_0 is a serial shift input and QIO_3 is a serial shift output. During a shift-down operation, QIO_3 is a serial shift inputs and QIO_0 is a serial shift ouptut.

Double-length arithmetic and logical shifting capability is provided by the MC2903. The double-length shift is performed by connecting QIO_3 of the most significant slice to SIO_0 of the least significant slice, and executing an instruction which shifts both the ALU output and the Q Register.

The Q Register and shifter are controlled by the instruction inputs. Table 4 defines the MC2903 special functions and the operations which the Q Register and shifter perform for each. When the MC2903 executes instructions other than the nine special functions, the Q Register and shifter operation is controlled by instruction bits I8, I7, I6, I5. Table 3 defines the Q Register and shifter operation as a function of these four bits.

TABLE 3 – ALU DESTINATION CONTROL FOR I0 OR I1 OR I2 OR I3 OR I4 = High, $\overline{IEN}$ = Low

I8 I7 I6 I5	Hex Code	ALU Shifter Function	SIO_3		Y3		Y2		Y1	Y0	SIO_0	$\overline{Write}$	Q Reg and Shifter Function	QIO_3	QIO_0
			Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices							
L L L L	0	Arith F/2 → Y	Input	Input	F3	SIO_3	SIO_3	F3	F2	F1	F0	L	Hold	Hi-Z	Hi-Z
L L L H	1	Log F/2 → Y	Input	Input	SIO_3	SIO_3	F3	F3	F2	F1	F0	L	Hold	Hi-Z	Hi-Z
L L H L	2	Arith F/2 → Y	Input	Input	F3	SIO_3	SIO_3	F3	F2	F1	F0	L	Log Q/2 → Q	Input	Q0
L L H H	3	Log F/2 → Y	Input	Input	SIO_3	SIO_3	F3	F3	F2	F1	F0	L	Log Q/2 → Q	Input	Q0
L H L L	4	F → Y	Input	Input	F3	F3	F2	F2	F1	F0	Parity	L	Hold	Hi-Z	Hi-Z
L H L H	5	F → Y	Input	Input	F3	F3	F2	F2	F1	F0	Parity	H	Log Q/2 → Q	Input	Q0
L H H L	6	F → Y	Input	Input	F3	F3	F2	F2	F1	F0	Parity	H	F → Q	Hi-Z	Hi-Z
L H H H	7	F → Y	Input	Input	F3	F3	F2	F2	F1	F0	Parity	L	F → Q	Hi-Z	Hi-Z
H L L L	8	Arith 2F → Y	F2	F3	F3	F2	F1	F1	F0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H L L H	9	Log 2F → Y	F3	F3	F2	F2	F1	F1	F0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H L H L	A	Arith 2F → Y	F2	F3	F3	F2	F1	F1	F0	SIO_0	Input	L	Log 2Q → Q	Q3	Input
H L H H	B	Log 2F → Y	F3	F3	F2	F2	F1	F1	F0	SIO_0	Input	L	Log 2Q → Q	Q3	Input
H H L L	C	F → Y	F3	F3	F3	F3	F2	F2	F1	F0	Hi-Z	H	Hold	Hi-Z	Hi-Z
H H L H	D	F → Y	F3	F3	F3	F3	F2	F2	F1	F0	Hi-Z	H	Log 2Q → Q	Q3	Input
H H H L	E	SIO_0 → Y0, Y1, Y2, Y3	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H H H H	F	F → Y	F3	F3	F3	F3	F2	F2	F1	F0	Hi-Z	L	Hold	Hi-Z	Hi-Z

Parity = F3 ∀ F2 ∀ F1 ∀ F0 ∀ SIO_3

∀ = Exclusive OR

L = Low H = High Hi-Z = High Impedance

Output Buffers

The DB and Y ports are bidirectional I/O ports driven by three-state output buffers with external output enable controls. The Y output buffers are enabled when the $\overline{OE_Y}$ input is Low and are in the high-impedance state when $\overline{OE_Y}$ is High. Likewise, the DB output buffers are enabled when the $\overline{OE_B}$ input is Low and in the high-impedance state when $\overline{OE_B}$ is High.

The zero, Z, pin is an open collector input/output that can be wire-ORed between slices. As an output it can be used as a zero detect status flag and generally indicates that the Y0–3 pins are all Low, whether they are driven from teh Y output buffers or from an external source connected to the Y0–3 pins. To some extent the meaning of this signal varies with the instruction being performed. Refer to Table 5 for an exact definition of this signal as a function of the MC2903 instruction.

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the nine instruction inputs, I0–8: the Instruction Enable input, $\overline{IEN}$, the $\overline{LSS}$ input, and the $\overline{Write}/\overline{MSS}$ input/output.

The $\overline{Write}$ output is Low when an instruction which writes data into the RAM is being executed. Refer to Tables 3 and 4 for a definition of the $\overline{Write}$ output as a function of the MC2903 instruction inputs.

When $\overline{IEN}$ is High, the $\overline{Write}$ output is forced High and the Q Register and Sign Compare Flip-Flop contents are preserved. When $\overline{IEN}$ is Low, the $\overline{Write}$ output is enabled and the Q Register and Sign Compare Flip-Flop can be written according to the MC2903 instruction. The Sign Compare Flip-Flop is an on-chip flip-flop which is used during an MC2903 divide operation (see Figure B).

Programming the MC2903 Slice Position

Tying the $\overline{LSS}$ input Low programs the slice to operate as a least signficant slice (LSS) and enables the $\overline{Write}$ output signal onto the $\overline{Write}/\overline{MSS}$ bidirectional I/O pin. When $\overline{LSS}$ is tied High, the $\overline{Write}/\overline{MSS}$ pin becomes an input pin; tying the $\overline{Write}/\overline{MSS}$ pin High programs the slice to operate as an intermediate slice (IS) and tying it Low programs the slice to operate as a most significant slice (MSS).

TABLE 4. SPECIAL FUNCTIONS: $I0 = I1 = I2 = I3 = I4$ = Low, $\overline{IEN}$ = Low

$I8$ $I7$ $I6$ $I5$	Hex Code	Special Function	ALU Function	ALU Shifter Function	SIO_3 Most Sig. Slice	SIO_3 Other Slices	SIO_0	Q Reg and Shifter Function	QIO_3	QIO_0	$\overline{Write}$
L L L L	0	Unsigned Multiply	$F = S + C_n$ if $Z = L$ $F = R + S + C_n$ if $Z = H$	Log $F/2 \rightarrow Y$ (Note 1)	Hi-Z	Input	F0	Log $Q/2 \rightarrow Q$	Input	Q0	L
L L H L	2	Two's Complement Multiply	$F = S + C_n$ if $Z = L$ $F = R + S + C_n$ if $Z = H$	Log $F/2 \rightarrow Y$ (Note 2)	Hi-Z	Input	F0	Log $Q/2 \rightarrow Q$	Input	Q0	L
L H L L	4	Increment by One or Two	$F = S + 1 + C_n$	$F \rightarrow Y$	Input	Input	Parity	Hold	Hi-Z	Hi-Z	L
L H L H	5	Sign/Magnitude-Two's Complement	$F = S + C_n$ if $Z = L$ $F = \overline{S} + C_n$ if $Z = H$	$F \rightarrow Y$ (Note 3)	Input	Input	Parity	Hold	Hi-Z	Hi-Z	L
L H H L	6	Two's Complement Multiply, Last Cycle	$F = S + C_n$ if $Z = L$ $F = S - R - 1 + C_n$ if $Z = H$	Log $F/2 \rightarrow Y$ (Note 2)	Hi-Z	Input	F0	Log $Q/2 \rightarrow Q$	Input	Q0	L
H L L L	8	Single Length Normalize	$F = S + C_n$	$F \rightarrow Y$	F3	F3	Hi-Z	Log $2Q \rightarrow Q$	Q3	Input	L
H L H L	A	Double Length Normalize and First Divide Op	$F = S + C_n$	Log $2F \rightarrow Y$	R3 ∀ F3	F3	Input	Log $2Q \rightarrow Q$	Q3	Input	L
H H L L	C	Two's Complement Divide	$F = S + R + C_n$ if $Z = L$ $F = S - R - 1 + C_n$ if $Z = H$	Log $2F \rightarrow Y$	$\overline{R3 \forall F3}$	F3	Input	Log $2Q \rightarrow Q$	Q3	Input	L
H H H L	E	Two's Complement Divide, Correction and Remainder	$F = S + R + C_n$ if $Z = L$ $F = S - R - 1 + C_n$ if $Z = H$	$F \rightarrow Y$	F3	F3	Hi-Z	Log $2Q \rightarrow Q$	Q3	Input	L

NOTES 1. At the most significant slice only, the C_{n+4} signal is internally gated to the Y3 output.
2. At the most significant slice only, F3 ∀ OVR is internally gated to the Y3 output.
3. At the most significant slice only, S3 ∀ F3 is generated at the Y3 output.
4. Op codes 1, 3, 7, 9, B, D, and F are reserved for future use.

L = Low, H = High, X = Don't Care, Hi-Z = High Impedance, ∀ = Exclusive OR, Parity = $SIO_3 \forall F3 \forall F2 \forall F1 \forall F0$

MC2903 SPECIAL FUNCTIONS

The MC2903 provides nine special functions which facilitate the implementation of the following operations:

- Single- and double-length normalization
- Two's complement division
- Unsigned and two's complement multiplication
- Conversion between two's complement and sign/magnitude representation
- Incrementation by one or two

Table 4 defines these special functions.

The single-length and double-length normalization functions can be used to adjust a single-precision or double-precision floating point number in order to bring its mantissa within a specified range.

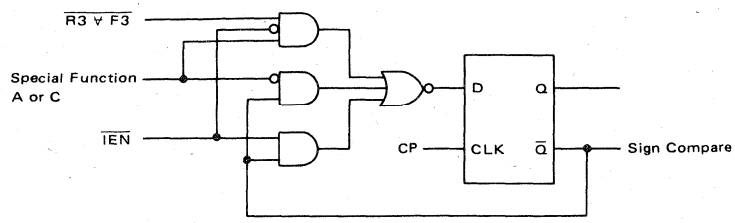
Three special functions which can be used to perform a two's complement, non-restoring divide operation are provided by the MC2903. These functions provide both single- and double-precision divide operations and can be performed in "n" clock cycles, where n is the number of bits in the quotient.

The unsigned multiply special function and the two two's complement multiply special functions can be used to multiply two n-bit, unsigned or two's complement numbers, respectively, in n clock cycles. These functions utilize the conditional add and shift algorithm. During the last cycle of the two's complement multiplication, a conditional subtraction, rather than addition, is performed because the sign bit of the multiplier carries negative weight.

The sign/magnitude-two's complement special function can be used to convert number representation systems. A number expressed in sign/magnitude representation can be converted to the two's complement representation, and vice-versa, in one clock cycle.

The increment-by-one-or-two special function can be used to increment an unsigned or two's complement number by one or two. This is useful in 16-bit word, byte-addressable machines, where the word addresses are multiples of two.

Refer to MC2903 applications section for a more detailed description of these special functions.



The sign compare signal appears at the Z output of the most significant slice during special functions C, D and E, F. Refer to Table 5.

FIGURE B – SIGN COMPARE FLIP-FLOP

TABLE 5 – MC2903 STATUS OUTPUTS

Hex I8I7I6I5	Hex I4I3I2I1	I0	Gi (i = 0 to 3)	Pi (i = 0 to 3)	C_{n+4}	$\overline{P}$/OVR Most Sig. Slice	$\overline{P}$/OVR Other Slices	$\overline{G}$/N Most Sig. Slice	$\overline{G}$/N Other Slices	Z Most Sig. Slice	Z Intermediate Slice	Z Least Sig. Slice
X	0	H	0	1	0	0	0	F3	$\overline{G}$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$
X	1	X	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F3	$\overline{G}$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$
X	2	X	$R_i \wedge \overline{S}_i$	$R_i \vee \overline{S}_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F3	$\overline{G}$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$
X	3	X	$R_i \wedge S_i$	$R_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F3	$\overline{G}$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$
X	4	X	0	S_i	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F3	$\overline{G}$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$
X	5	X	0	$\overline{S}_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F3	$\overline{G}$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$
X	6	X	0	R_i	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F3	$\overline{G}$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$
X	7	X	0	$\overline{R}_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F3	$\overline{G}$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$
X	8	X	0	1	0	0	0	F3	$\overline{G}$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$
X	9	X	$\overline{R}_i \wedge S_i$	1	0	0	0	F3	$\overline{G}$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$
X	A	X	$R_i \wedge S_i$	$R_i \vee S_i$	0	0	0	F3	$\overline{G}$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$
X	B	X	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	0	0	0	F3	$\overline{G}$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$
X	C	X	$R_i \wedge S_i$	1	0	0	0	F3	$\overline{G}$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$
X	D	X	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F3	$\overline{G}$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$
X	E	X	$R_i \wedge S_i$	1	0	0	0	F3	$\overline{G}$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$
X	F	X	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F3	$\overline{G}$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$
0	0	L	0 if Z = L $R_i \wedge S_i$ if Z = H	S_i if Z = L $R_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F3	$\overline{G}$	Input	Input	Q0
2	0	L	0 if Z = L $R_i \wedge S_i$ if Z = H	S_i if Z = L $R_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+4} \forall C_{n+4}$	$\overline{P}$	F3	$\overline{G}$	Input	Input	Q0
4	0	L	See Note 1	See Note 2	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F3	$\overline{G}$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$	$\overline{Y}0\overline{Y}1\overline{Y}2\overline{Y}3$
5	0	L	0	S_i if Z = L $\overline{S}_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$		F3 if Z = L F3 ∀ S3 if Z = H	$\overline{G}$	S3	Input	Input
6	0	L	0 if Z = L $\overline{R}_i \wedge S_i$ if Z = H	S_i if Z = L $\overline{R}_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F3	$\overline{G}$	Input	Input	Q0
8	0	L	0	S_i	See Note 3	Q2 ∀ Q1	$\overline{P}$	Q3	$\overline{G}$	$\overline{Q}0\overline{Q}1\overline{Q}2\overline{Q}3$	$\overline{Q}0\overline{Q}1\overline{Q}2\overline{Q}3$	$\overline{Q}0\overline{Q}1\overline{Q}2\overline{Q}3$
A	0	L	0	S_i	See Note 4	F2 ∀ F1	$\overline{P}$	F3	$\overline{G}$	See Note 5	See Note 5	See Note 5
C	0	L	$R_i \wedge S_i$ if Z = L $\overline{R}_i \wedge S_i$ if Z = H	$R_i \vee S_i$ if Z = L $\overline{R}_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F3	$\overline{G}$	Sign Compare FF Output	Input	Input
E	0	L	$R_i \wedge S_i$ if Z = L $\overline{R}_i \wedge S_i$ if Z = H	$R_i \vee S_i$ if Z = L $\overline{R}_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F3	$\overline{G}$	Sign Compare FF Output	Input	Input

NOTES 1. If $\overline{LSS}$ is Low, G0 = S0 and G1,2,3 = 0. If $\overline{LSS}$ is High, G0,1,2,3 = 0.
2. If $\overline{LSS}$ is Low, P0 = 1 and P1,2,3 = S1,2,3. If $\overline{LSS}$ is High, $P_i = S_i$.
3. At the most significant slice, $C_{n+4} = Q3 \forall Q2$. At other slices, $C_{n+4} = G \vee PC_n$.
4. At the most significant slice, $C_{n+4} = F3 \forall F2$. At other slices, $C_{n+4} = G \vee PC_n$.
5. $Z = \overline{Q}0\overline{Q}1\overline{Q}2\overline{Q}3\overline{F}0\overline{F}1\overline{F}2\overline{F}3$.

L = Low = 0. H = High = 1. $\vee$ = OR. $\wedge$ = AND. $\forall$ = Exclusive OR.
$P = P3P2P1P0$
$G = G3 \vee G2P3 \vee G1P2P3 \vee G0P1P2P3$
$C_{n+3} = G2 \vee G1P2 \vee G0P1P2 \vee C_n P0P1P2$

PIN DEFINITIONS

A0–3 Four RAM address inputs which contain the address of the RAM word appearing at the RAM A output port.

B0–3 Four RAM address inputs which contain the address of the RAM word appearing at the RAM B output port and into which new data is written when the $\overline{WE}$ input and the CP input are Low.

$\overline{WE}$ The RAM write enable input. If $\overline{WE}$ is Low, data at the Y I/O port is written into the RAM when the CP input is Low. When $\overline{WE}$ is High, writing data into the RAM is inhibited.

DA_{0-3} A four-bit external data input which can be selected as one of the MC2903 ALU operand sources; DA_0 is the least significant bit.

$\overline{EA}$ A control input which, when High, selects DA_{0-3}, and, when Low, selects RAM output A as the ALU R operand.

DB_{0-3} A four-bit external data input/output. Under control of the $\overline{OE_B}$ input, RAM output port B can be directly read on these lines, or input data on these lines can be selected as the ALU S operand.

$\overline{OE_B}$ A control input which, when Low, enables RAM output B onto the DB_{0-3} lines and, when High, disables the RAM output B three-state buffers.

C_n The carry-in input to the MC2903 ALU.

I0–8 The nine instruction inputs used to select the MC2903 operation to be performed.

$\overline{IEN}$ The instruction enable input which, when Low, enables the $\overline{Write}$ output and allows the Q Register and the Sign Compare flip-flop to be written. When $\overline{IEN}$ is High, the $\overline{Write}$ output is forced High and the Q Register and Sign Compare flip-flop are in the hold mode.

C_{n+4} This output generally indicates the carry-out of the MC2903 ALU. Refer to Table 5 for an exact definition of this pin.

$\overline{G}$/N A multipurpose pin which indicates the carry generate, $\overline{G}$, function at the least significant and intermediate slices, and generally indicates the sign, N, of the ALU result at the most significant slice. Refer to Table 5 for an exact definition of this pin.

$\overline{P}$/OVR A multipurpose pin which indicates the carry propagate, $\overline{P}$, function at the least significant and intermediate slices, and indicates the conventional two's complement overflow, OVR, signal at the most significant slice. Refer to Table 5 for an exact definition of this pin.

Z An open-collector input/output pin which, when High, generally indicates the Y0–3 outputs are all Low. For some special functions, Z is used as an input pin. Refer to Table 5 for an exact definition of this pin.

SIO_0, SIO_3 Bidirectional serial shift inputs/outputs for the ALU shifter. During a shift-up operation, SIO_0 is an input and SIO_3 an output. During a shift-down operation, SIO_3 is an input and SIO_0 is an output. Refer to Tables 3 and 4 for an exact definition of these pins.

QIO_0, QIO_3 Bidirectional serial shift inputs/outputs for the Q shifter which operate like SIO_0 and SIO_3. Refer to Tables 3 and 4 for an exact definition of these pins.

$\overline{LSS}$ An input pin which, when tied Low, programs the chip to act as the least significant slice (LSS) of an MC2903 array and enables the $\overline{Write}$ output onto the $\overline{Write}$/$\overline{MSS}$ pin. When $\overline{LSS}$ is tied High, the chip is programmed to operate as either an intermediate or most significant slice and the $\overline{Write}$ output buffer is disabled.

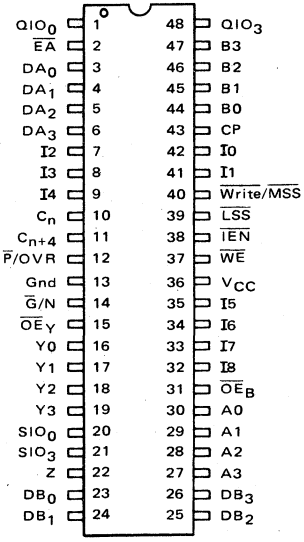
$\overline{Write}$/$\overline{MSS}$ When $\overline{LSS}$ is tied Low, the $\overline{Write}$ output signal appears at this pin; the $\overline{Write}$ signal is Low when an instruction which writes data into the RAM is being executed. When $\overline{LSS}$ is tied High, $\overline{Write}$/$\overline{MSS}$ is an input pin; tying it High programs the chip to operate as an intermediate slice (IS) and tying it Low programs the chip to operate as the most significant slice (MSS).

Y0–3 Four data inputs/outputs of the MC2903. Under control of the $\overline{OE_Y}$ input, the ALU shifter output data can be enabled onto these lines, or these lines can be used as data inputs when external data is written directly into the RAM.

$\overline{OE_Y}$ A control input which, when Low, enables the ALU shifter output data onto the Y0–3 lines and, when High, disables the Y0–3 three-state output buffers.

CP The clock input to the MC2903. The Q Register and Sign Compare flip-flop are clocked on the Low-to-High transition of the CP signal. When enabled by $\overline{WE}$, data is written in the RAM when CP is Low.

PIN ASSIGNMENT



MOTOROLA Semiconductors

MC2905

QUAD TWO-INPUT OC BUS TRANSCEIVER WITH THREE-STATE RECEIVER

The MC2905 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applicatons. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the Bus inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8 V maximum. The Bus input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is High, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

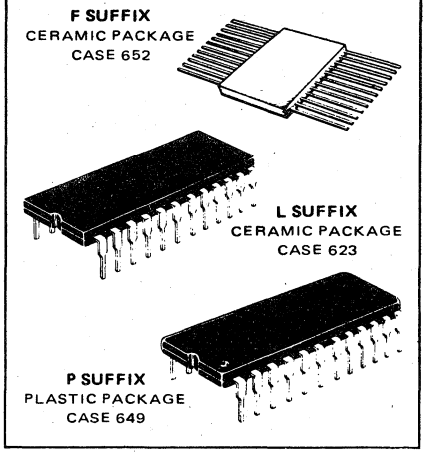
The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is Low, the A_n data is stored in the register and when S is High, the B_n data is stored. The buffered common clock (DRCP) enters the data into this driver register on the low-to-high transition.

Data from the A or B inputs is inverted at the Bus output. Likewise, data at the Bus input is inverted at the receiver output. Thus, data is noninverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is Low, the latch is open and the receiver outputs will follow the bus inputs (Bus data inverted and $\overline{OE}$ Low). When the $\overline{RLE}$ input is High, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is High, the receiver outputs are in the high-impedance state.

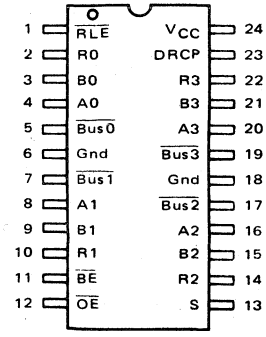
FEATURES

- Quad High-speed LSI Bus-transceiver
- Open-collector Bus Driver
- Two-port Input to D-type Register on Driver
- Bus Driver Output Can Sink 100 mA at 0.8 V Max
- Receiver Has Output Latch for Pipeline Operation
- Three-state Receiver Outputs Sink 12 mA
- Advanced Low-power Schottky Processing
- 100% Reliability Assurance Testing in Compliance With MIL-STD-883

TTL QUAD TWO-INPUT OC BUS TRANSCEIVER WITH THREE-STATE RECEIVER



PIN ASSIGNMENT



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	MC2905PC
Hermetic DIP	0°C to +70°C	MC2905LC
Hermetic DIP	-55°C to +125°C	MC2905LM
Hermetic Flat Pack	-55°C to +125°C	MC2905FM

DS9506

MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, into Outputs (Except Bus)	30 mA
DC Output Current, into Bus	200 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

MC2905XC − T_A = 0°C to +70°C, V_{CC} = 5.0 V ±5% (Commercial), Min = 4.75 V, Max = 5.25 V
MC2905XM − T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10% (Military), Min = 4.5 V, Max = 5.5 V

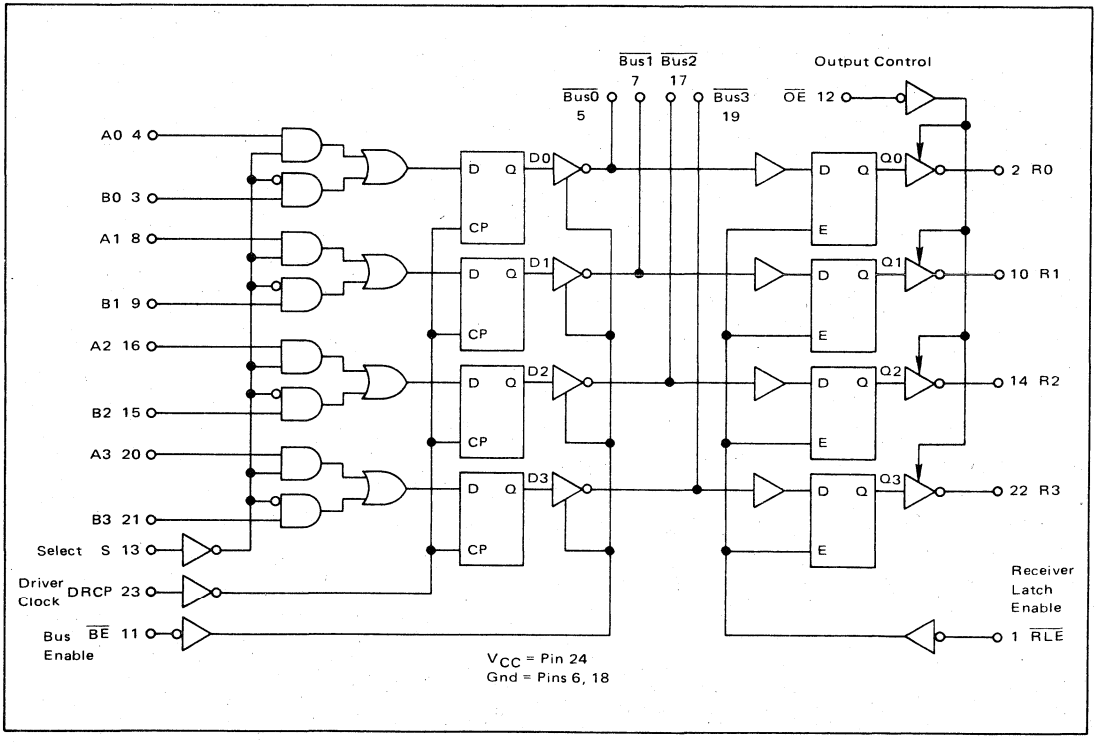
Parameter	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Unit
BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE								
V_{OL}	Bus Output Low Voltage	V_{CC} = Min	I_{OL} = 40 mA			0.32	0.5	Volts
			I_{OL} = 70 mA			0.41	0.7	
			I_{OL} = 100 mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = Max	V_O = 0.4 V				−50	μA
			V_O = 4.5 V	Military			200	
				Commercial			100	
I_{off}	Bus Leakage Current (Power off)	V_O = 4.5 V					100	μA
V_{TH}	Receiver Input High Threshold	Bus Enable = 2.4 V		Military	2.4	2.0		Volts
				Commercial	2.3	2.0		
V_{TL}	Receiver Input Low Threshold	Bus Enable = 2.4 V		Military		2.0	1.5	Volts
				Commercial		2.0	1.6	
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE								
V_{OH}	Receiver Output High Voltage	V_{CC} = Min, V_{in} = V_{IL} or V_{IH}	Military, I_{OH} = −1.0 mA		2.4	3.4		Volts
			Commercial, I_{OH} = −2.6 mA		2.4	3.4		
V_{OL}	Receiver Output Low Voltage	V_{CC} = Min, V_{in} = V_{IL} or V_{IH}	I_{OL} = 4.0 mA			0.27	0.4	Volts
			I_{OL} = 8.0 mA			0.32	0.45	
			I_{OL} = 12 mA			0.37	0.5	
V_{IH}	Input High Level (Except Bus)	Guaranteed input logical High for all inputs			2.0			Volts
V_{IL}	Input Low Level (Except Bus)	Guaranteed input logical Low for all inputs		Military			0.7	Volts
				Commercial			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = Min, I_{in} = −18 mA					−1.2	Volts
I_{IL}	Input Low Current (Except Bus)	V_{CC} = Max, V_{in} = 0.4 V					−0.36	mA
I_{IH}	Input High Current (Except Bus)	V_{CC} = Max, V_{in} = 2.7 V					20	μA
I_{in}	Input High Current (Except Bus)	V_{CC} = Max, V_{in} = 5.5 V					100	μA
I_O	Receiver Off-State Output Current	V_{CC} = Max	V_O = 2.4 V				20	μA
			V_O = 0.4 V				−20	
I_{SC}	Receiver Output Short Circuit Current	V_{CC} = Max			−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All inputs = Gnd				69	105	mA

NOTES: 1. For conditions shown as Min or Max, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

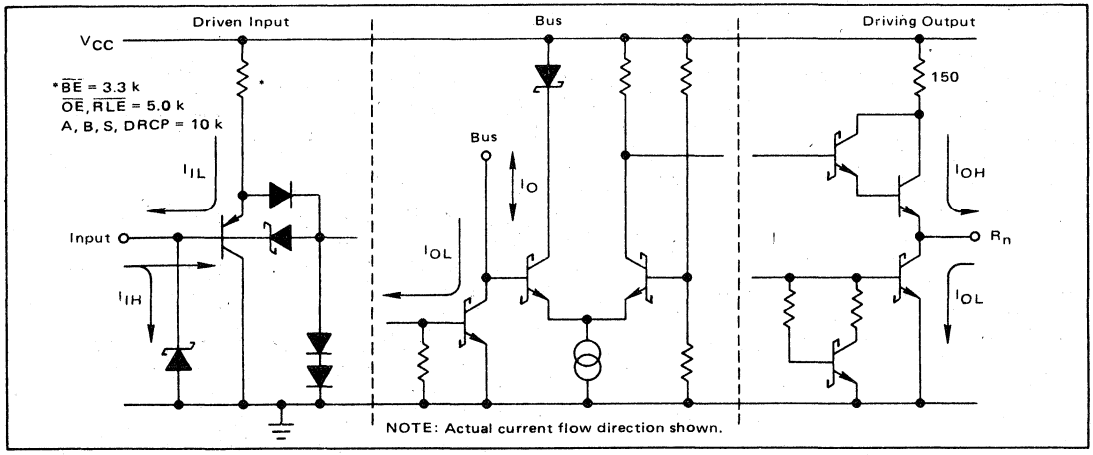
SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameter	Description	Test Conditions	MC2905XM			MC2905XC			Unit
			Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (Bus) = 50 pF	–	21	40	–	21	36	ns
t_{PLH}		R_L (Bus) = 50 Ω	–	21	40	–	21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus		–	13	26	–	13	23	ns
t_{PLH}			–	13	26	–	13	23	
t_s	Data Inputs (A or B)	C_L = 15 pF	25	–	–	23	–	–	ns
t_h		R_L = 2.0 k	8.0	–	–	7.0	–	–	
t_s	Select Input (S)		33	–	–	30	–	–	ns
t_h			8.0	–	–	7.0	–	–	
t_{PW}	Driver Clock (DRCP) Pulse Width (High)		28	–	–	25	–	–	ns
t_{PLH}	Bus to Receiver Output (Latch Enable)		–	18	37	–	18	34	ns
t_{PHL}			–	18	37	–	18	34	
t_{PLH}	Latch Enable to Receiver Output		–	21	37	–	21	34	ns
t_{PHL}			–	21	37	–	21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21	–	–	18	–	–	ns
t_h			7.0	–	–	5.0	–	–	
t_{ZH}	Output Control to Receiver Output		–	14	28	–	14	25	ns
t_{ZL}			–	14	28	–	14	25	
t_{HZ}	Output Control to Receiver Output	C_L = 5.0 pF	–	14	28	–	14	25	ns
t_{LZ}		R_L = 2.0 k	–	14	28	–	14	25	

LOGIC DIAGRAM



INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

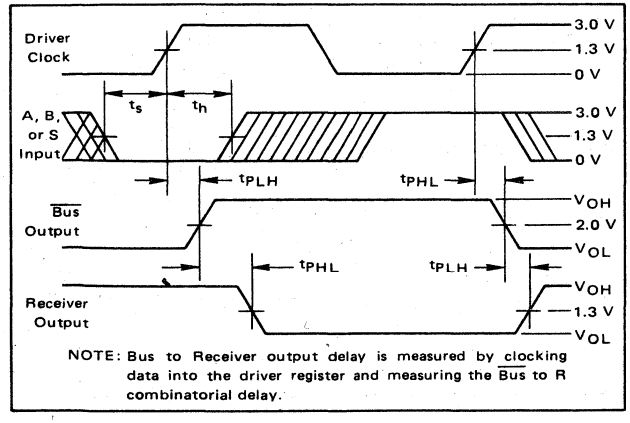


FUNCTION TABLE

Inputs							Internal to Device		Bus	Output	
S	A_n	B_n	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_n	Q_n	$\overline{Bus_n}$	R_n	Function
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	Z	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

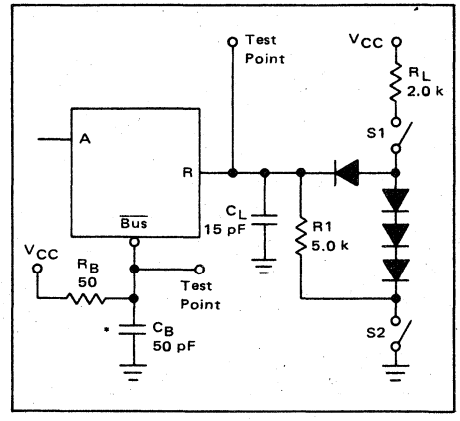
H = High Z = High impedance X = Don't care
L = Low NC = No change ↑ = Low-to-high transition

SWITCHING WAVEFORMS



NOTE: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{Bus}$ to R combinatorial delay.

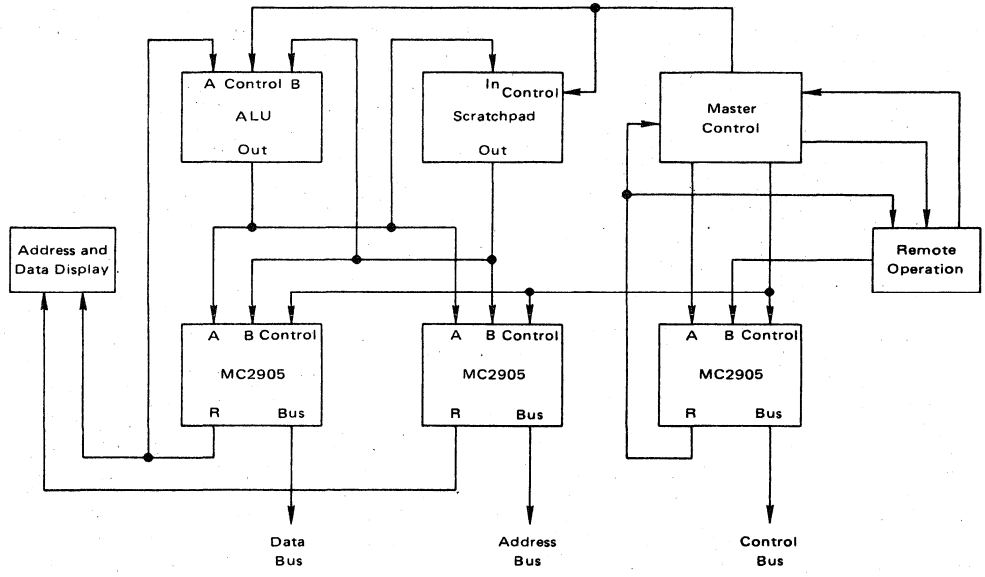
LOAD TEST CIRCUIT



DEFINITIONS OF FUNCTIONAL TERMS

A0, A1, A2, A3	The "A" word data input into the two input multiplexers of the driver register.
B0, B1, B2, B3	The "B" word data input into the two input multiplexers of the driver register.
S	Select. When the select input is Low, the A data word is applied to the driver register. When the select input is High, the B word is applied to the driver register.
DRCP	Driver Clock Pulse. Clock pulse for the driver register.
$\overline{BE}$	$\overline{\text{Bus Enable}}$. When the Bus Enable is High, the four drivers are in the high impedance state.
$\overline{Bus0}$, $\overline{Bus1}$, $\overline{Bus2}$, $\overline{Bus3}$	The four driver outputs and receiver inputs (data is inverted).
R0, R1 R2, R3	The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.
$\overline{RLE}$	$\overline{\text{Receiver Latch Enable}}$. When $\overline{RLE}$ is Low, data on the Bus inputs is passed through the receiver latches. When $\overline{RLE}$ is High, the receiver latches are closed and will retain the data independent of all other inputs.
$\overline{OE}$	$\overline{\text{Output Enable}}$. When the $\overline{OE}$ input is High, the four three-state receiver outputs are in the high impedance state.

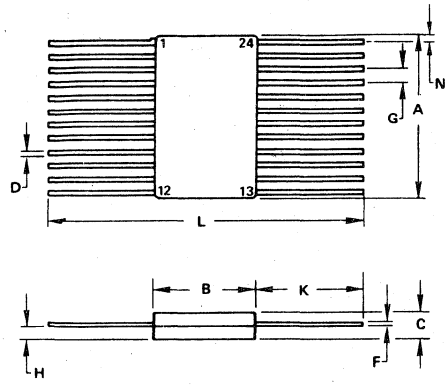
APPLICATIONS



The MC2905 is a universal Bus Transceiver useful for many system data, address, control, and timing input/output interfaces.

PACKAGE DIMENSIONS

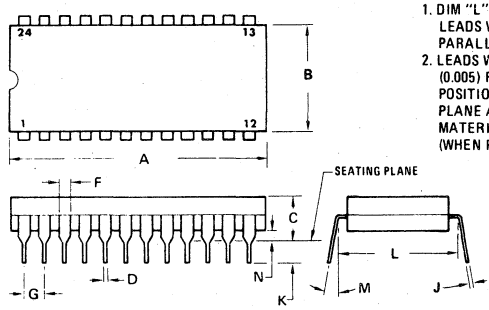
CASE 652



NOTES:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.99	15.49	0.590	0.610
B	9.27	9.91	0.365	0.390
C	1.27	2.03	0.050	0.080
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.69	1.02	0.027	0.040
K	6.35	9.40	0.250	0.370
L	21.97	–	0.865	–
N	0.25	0.63	0.010	0.025

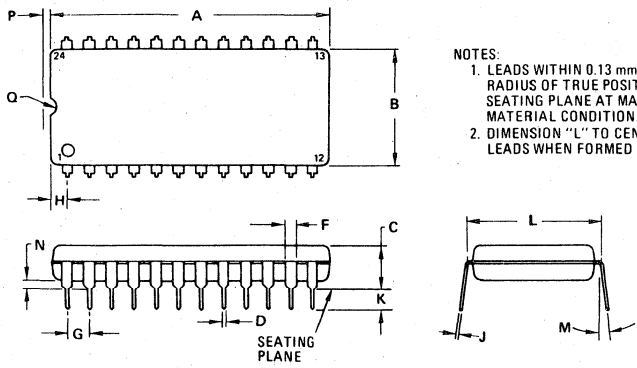
CASE 623



NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.29	4.06	0.090	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

CASE 649



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

MOTOROLA Semiconductors

MC2906

QUAD TWO-INPUT OC BUS TRANSCEIVER WITH PARITY

The MC2906 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the Bus inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8 V maximum. The Bus input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is High, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

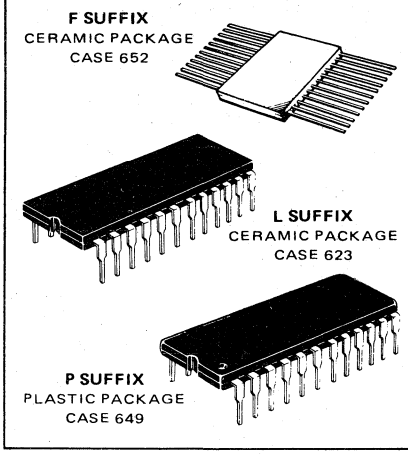
The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is Low, the A_n data is stored in the register and when S is High, the B_n data is stored. The buffered common clock (DRCP) enters the data into this driver register on the Low-to-High transition.

Data from the A or B inputs is inverted at the Bus output. Likewise, data at the Bus input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is Low, the latch is open and the receiver outputs will follow the bus inputs (Bus data inverted). When the $\overline{RLE}$ input is High, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is High, the receiver outputs are in the high-impedance state.

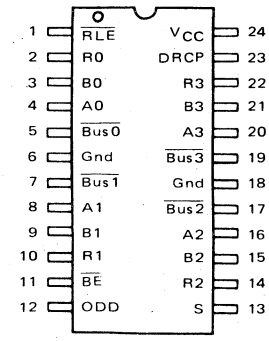
The MC2906 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is Low (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is High, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated; and, if the driver is in the high-impedance state, the Bus parity is checked.

- Quad High-speed LSI Bus Transceiver
- Open-collector Bus Driver
- Two-port Input to D-type Register on Driver
- Bus Driver Output Can Sink 100 mA at 0.8 V Max
- Internal Odd 4-bit Parity Checker/Generator
- Receiver Has Output Latch for Pipeline Operation
- Receiver Outputs Sink 12 mA
- Advanced Low-power Schottky Processing
- 100% Reliability Assurance Testing in Compliance With MIL-STD-883

TTL
QUAD TWO-INPUT
OC BUS TRANSCEIVER
WITH PARITY



PIN ASSIGNMENT



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	MC2906PC
Hermetic DIP	0°C to +70°C	MC2906LC
Hermetic DIP	−55°C to +125°C	MC2906LM
Hermetic Flat Pack	−55°C to +125°C	MC2906FM

DS9507

MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, into Outputs (Except Bus)	30 mA
DC Output Current, into Bus	200 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

MC2906XC — T_A = 0°C to +70°C, V_{CC} = 5.0 V ±5% (Commercial), Min = 4.75 V, Max = 5.25 V
MC2906XM — T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10% (Military), Min = 4.5 V, Max = 5.5 V

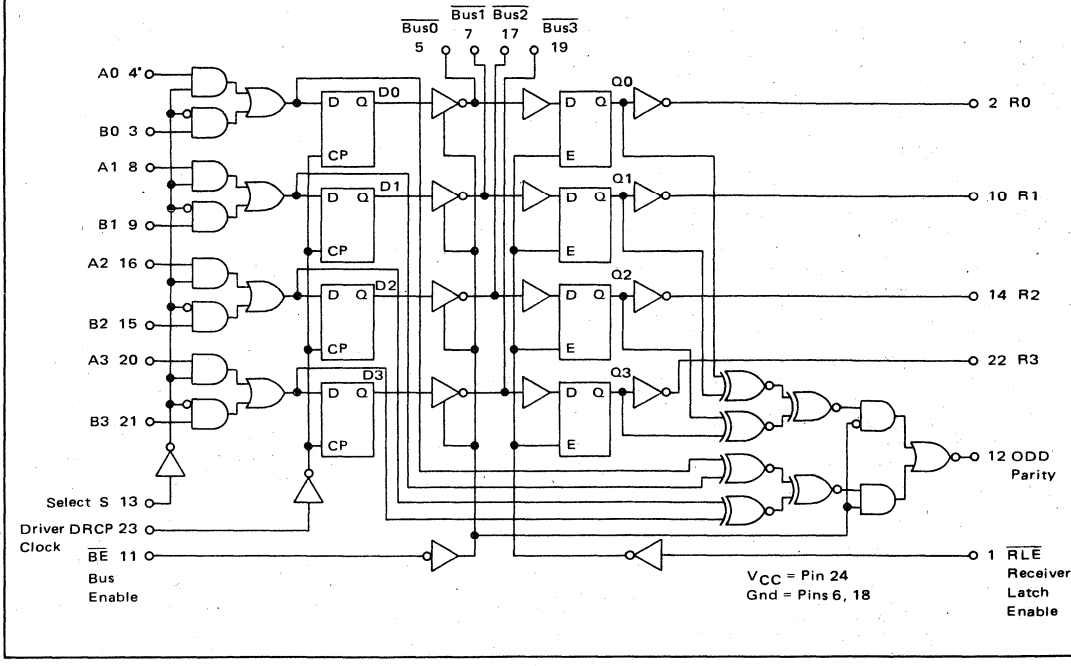
Parameter	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Unit
BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE								
V_{OL}	Bus Output Low Voltage	V_{CC} = Min	I_{OL} = 40 mA			0.32	0.5	Volts
			I_{OL} = 70 mA			0.41	0.7	
			I_{OL} = 100 mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = Max	V_O = 0.4 V				−50	μA
			V_O = 4.5 V	Military			200	
				Commercial			100	
I_{off}	Bus Leakage Current (Power off)	V_O = 4.5 V					100	μA
V_{TH}	Receiver Input High Threshold	Bus Enable = 2.4 V		Military	2.4	2.0		Volts
				Commercial	2.3	2.0		
V_{TL}	Receiver Input Low Threshold	Bus Enable = 2.4 V		Military		2.0	1.5	Volts
				Commercial		2.0	1.6	
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE								
V_{OH}	Receiver Output High Voltage	V_{CC} = Min, V_{in} = V_{IL} or V_{IH}	Military, I_{OH} = −1.0 mA		2.4	3.4		Volts
			Commercial, I_{OH} = −2.6 mA		2.4	3.4		
	Parity Output High Voltage	V_{CC} = Min, I_{OH} = −660 μA, V_{in} = V_{IH} or V_{IL}		Military	2.5	3.4		
				Commercial	2.7	3.5		
V_{OL}	Output Low Voltage (Except Bus)	V_{CC} = Min, V_{in} = V_{IL} or V_{IH}	I_{OL} = 4.0 mA			0.27	0.4	Volts
			I_{OL} = 8.0 mA			0.32	0.45	
			I_{OL} = 12 mA			0.37	0.5	
V_{IH}	Input High Level (Except Bus)	Guaranteed input logical High for all inputs			2.0			Volts
V_{IL}	Input Low Level (Except Bus)	Guaranteed input logical Low for all inputs		Military			0.7	Volts
				Commercial			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = Min, I_{in} = −18 mA					−1.2	Volts
I_{IL}	Input Low Current (Except Bus)	V_{CC} = Max, V_{in} = 0.4 V					−0.36	mA
I_{IH}	Input High Current (Except Bus)	V_{CC} = Max, V_{in} = 2.7 V					20	μA
I_{in}	Input High Current (Except Bus)	V_{CC} = Max, V_{in} = 5.5 V					100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = Max			−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All inputs = Gnd				72	105	mA

NOTES: 1. For conditions shown as Min or Max, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

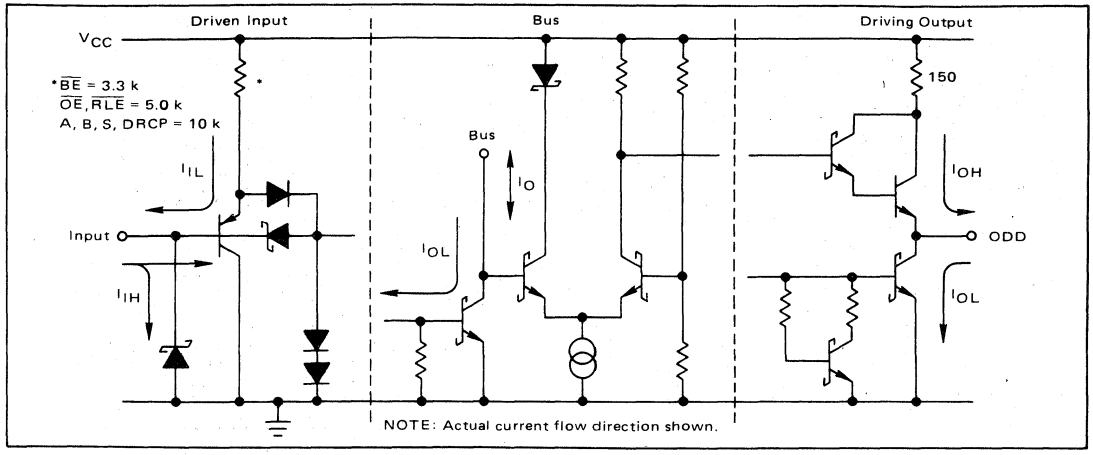
SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameter	Description	Test Conditions	MC2906XM			MC2906XC			Unit
			Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (Bus) = 50 pF	–	21	40	–	21	36	ns
t_{PLH}		R_L (Bus) = 50 Ω	–	21	40	–	21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus		–	13	26	–	13	23	ns
t_{PLH}			–	13	26	–	13	23	
t_s	Data Inputs (A or B)	C_L = 15 pF	25	–	–	23	–	–	ns
t_h		R_L = 2.0 k	8.0	–	–	7.0	–	–	
t_s	Select Input (S)		33	–	–	30	–	–	ns
t_h			8.0	–	–	7.0	–	–	
t_{PW}	Clock Pulse Width (High)		28	–	–	25	–	–	ns
t_{PLH}	Bus to Receiver Output (Latch Enable)		–	18	37	–	18	34	ns
t_{PHL}			–	18	37	–	18	34	
t_{PLH}	Latch Enable to Receiver Output		–	21	37	–	21	34	ns
t_{PHL}			–	21	37	–	21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21	–	–	18	–	–	ns
t_h			7.0	–	–	5.0	–	–	
t_{PLH}	A or B Data to Odd Parity (Driver Enabled)		–	21	40	–	21	36	ns
t_{PHL}			–	21	40	–	21	36	
t_{PLH}	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)		–	21	40	–	21	36	ns
t_{PHL}			–	21	40	–	21	36	
t_{PLH}	Latch Enable (RLE) to Odd Parity Output		–	21	40	–	21	36	ns
t_{PHL}			–	21	40	–	21	36	

LOGIC DIAGRAM



INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



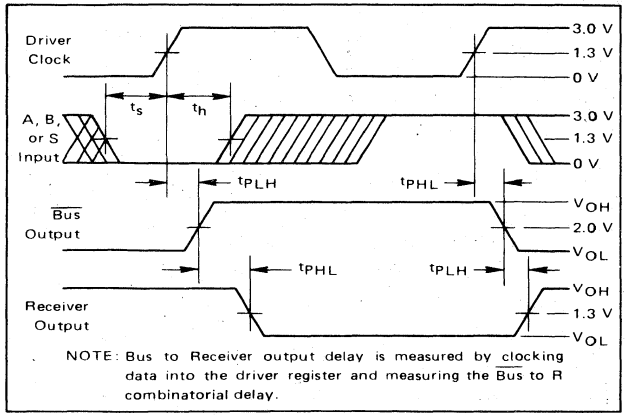
FUNCTION TABLE

Inputs						Internal to Device		Bus	Output	Parity	
S	A_n	B_n	DRCP	$\overline{BE}$	$\overline{RLE}$	D_n	Q_n	$\overline{Bus_n}$	R_n	ODD	Function
X	X	X	X	H	X	X	X	Z	X	Note 1	Driver output disable
X	X	X	X	H	L	X	L	L	H	Note 1	Driver output disable and receive data via Bus input
X	X	X	X	H	L	X	H	H	L		
X	X	X	X	X	H	X	NC	X	X	X	Latch received data
L	L	X	↑	X	X	L	X	X	X	X	Load driver register
L	H	X	↑	X	X	H	X	X	X	X	
H	X	L	↑	X	X	L	X	X	X	X	
H	X	H	↑	X	X	H	X	X	X	X	
X	X	X	L	X	X	NC	X	X	X	X	No driver clock restrictions
X	X	X	H	X	X	NC	X	X	X	X	
X	X	X	X	L	X	L	X	H	X	Note 2	Drive Bus
X	X	X	X	L	X	H	X	L	X		

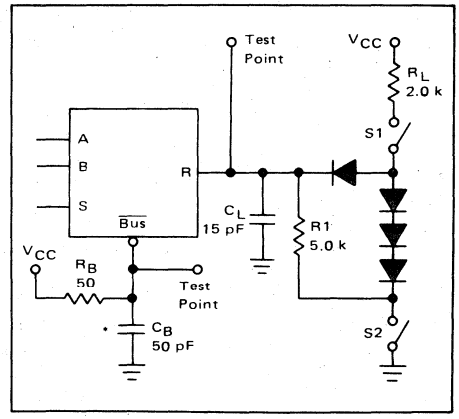
H = High
L = Low
Z = High impedance
NC = No change
X = Don't care
↑ = Low-to-high transition

NOTES:
1. ODD = Q0 ⊕ Q1 ⊕ Q2 ⊕ Q3 when $\overline{BE}$ = H
2. ODD = A0 ⊕ A1 ⊕ A2 ⊕ A3 when $\overline{BE}$ = L, S = L
   ODD = B0 ⊕ B1 ⊕ B2 ⊕ B3 when $\overline{BE}$ = L, S = H

SWITCHING WAVEFORMS



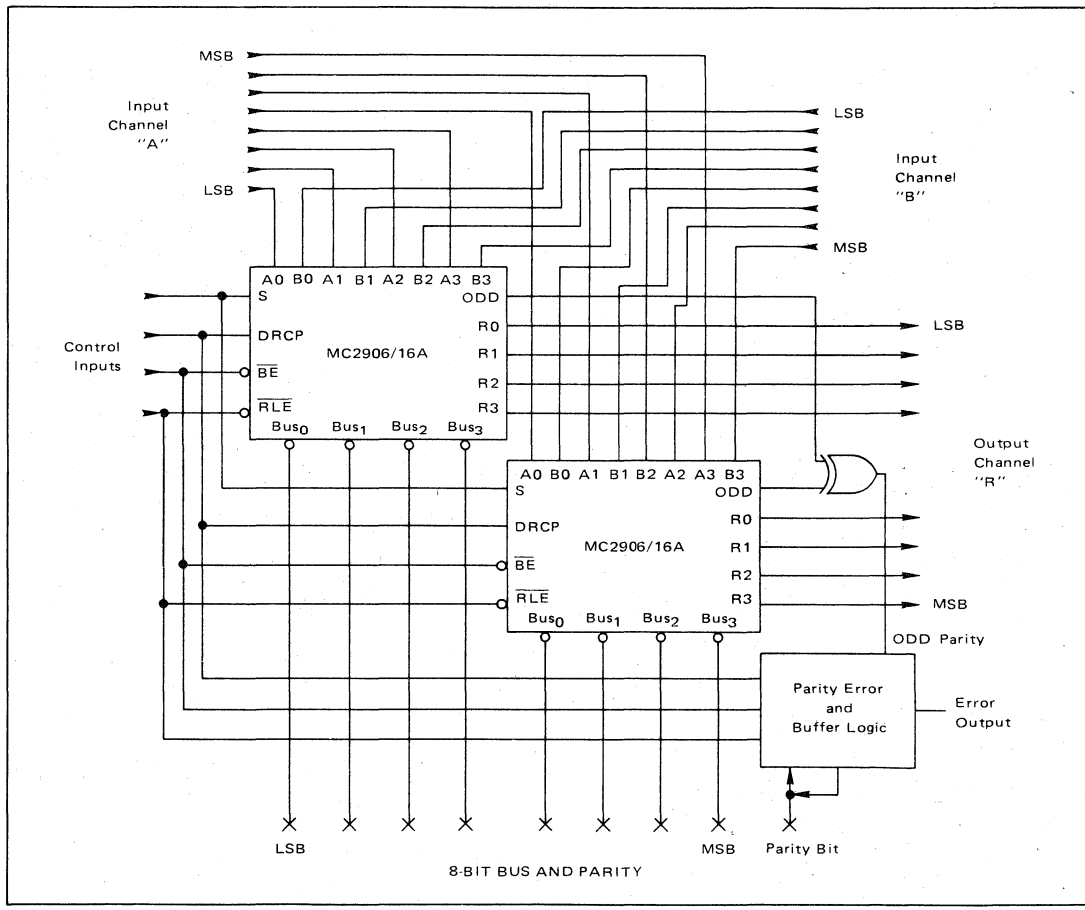
LOAD TEST CIRCUIT



DEFINITIONS OF FUNCTIONAL TERMS

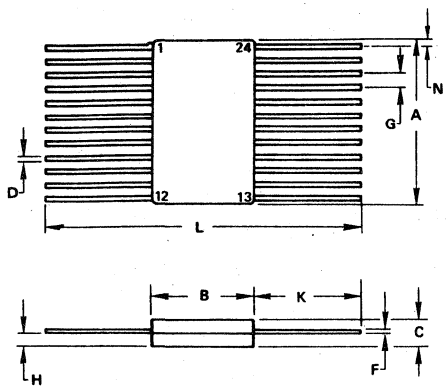
A0, A1, A2, A3	The "A" word data input into the two input multiplexers of the driver register.
B0, B1, B2, B3	The "B" word data input into the two input multiplexers of the driver register.
S	Select. When the select input is Low, the A data word is applied to the driver register. When the select input is High, the B word is applied to the driver register.
DRCP	Driver Clock Pulse. Clock pulse for the driver register.
$\overline{BE}$	$\overline{\text{Bus Enable}}$. When the Bus Enable is High, the four drivers are in the high impedance state.
$\overline{Bus0}$, $\overline{Bus1}$, $\overline{Bus2}$, $\overline{Bus3}$	The four driver outputs and receiver inputs (data is inverted).
R0, R1 R2, R3	The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.
$\overline{RLE}$	$\overline{\text{Receiver Latch Enable}}$. When RLE is Low, data on the Bus inputs is passed through the receiver latches. When RLE is High, the receiver latches are closed and will retain the data independent of all other inputs.
ODD	ODD Parity Output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

8-BIT PERIPHERAL INTERFACE



PACKAGE DIMENSIONS

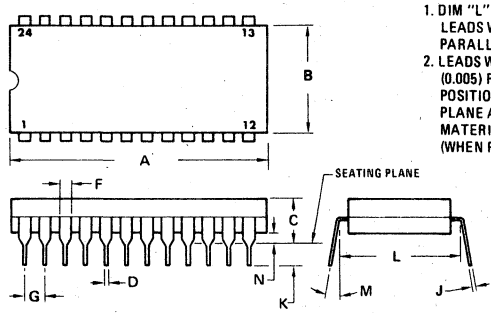
CASE 652



NOTES:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.99	15.49	0.590	0.610
B	9.27	9.91	0.365	0.390
C	1.27	2.03	0.050	0.080
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.69	1.02	0.027	0.040
K	6.35	9.40	0.250	0.370
L	21.97	–	0.865	–
N	0.25	0.63	0.010	0.025

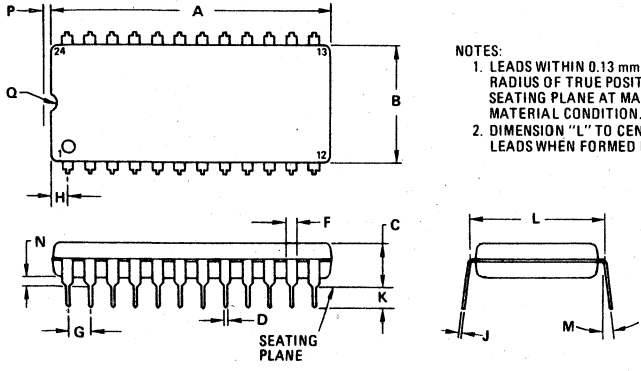
CASE 623



NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.29	4.06	0.090	0.160
L	15.24 BSC		0.600 BSC	
M	0^0	15^0	0^0	15^0
N	0.51	1.27	0.020	0.050

CASE 649



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

MC2907

QUAD BUS TRANSCEIVER WITH THREE-STATE RECEIVER AND PARITY

The MC2907 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier drive four D-type latches that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the Bus inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8 V maximum. The bus input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is High, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

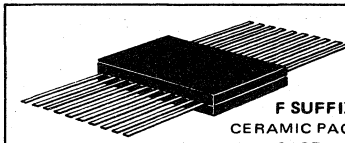
The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_n data into this driver register on the Low-to-High transition.

Data from the A input is inverted at the Bus output. Likewise, data at the Bus input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is Low, the latch is open and the receiver outputs will follow the bus inputs (Bus data inverted and $\overline{OE}$ Low). When the $\overline{RLE}$ input is High, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is High, the receiver outputs are in the high-impedance state.

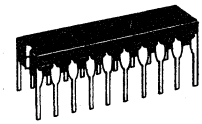
The MC2907 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is Low (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is High, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated; and, if the driver is in the high-impedance state, the Bus parity is checked.

- Quad High-speed LSI Bus Transceiver
- Open-collector Bus Driver
- D-type Register on Driver
- Bus Driver Output Can Sink 100 mA at 0.8 V Max
- Internal Odd 4-bit Parity Checker/Generator
- Receiver Has Output Latch for Pipeline Operation
- Three-state Receiver Outputs Sink 12 mA
- Advanced Low-power Schottky Processing
- 100% Reliability Assurance Testing in Compliance With MIL-STD-883

TTL QUAD BUS TRANSCEIVER WITH THREE-STATE RECEIVER AND PARITY

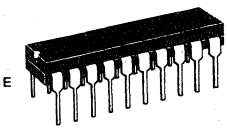


F SUFFIX
CERAMIC PACKAGE
CASE 737

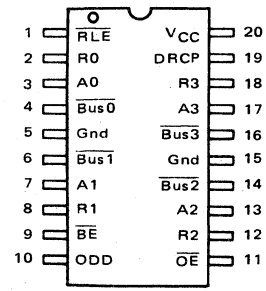


L SUFFIX
CERAMIC PACKAGE
CASE 732

P SUFFIX
PLASTIC PACKAGE
CASE 738



PIN ASSIGNMENT



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	MC2907PC
Hermetic DIP	0°C to +70°C	MC2907LC
Hermetic DIP	−55°C to +125°C	MC2907LM
Hermetic Flat Pack	−55°C to +125°C	MC2907FM

MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, into Outputs (Except Bus)	30 mA
DC Output Current, into Bus	200 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

MC2907XC − T_A = 0°C to +70°C, V_{CC} = 5.0 V ±5% (Commercial), Min = 4.75 V, Max = 5.25 V
MC2907XM − T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10% (Military), Min = 4.5 V, Max = 5.5 V

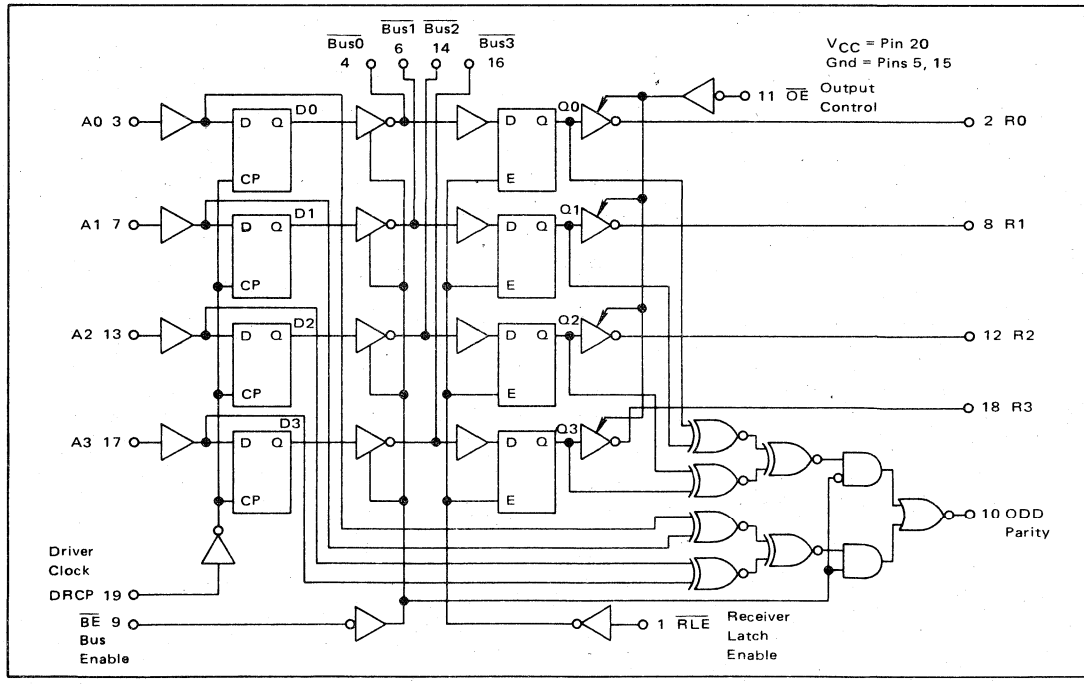
Parameter	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Unit
BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE								
V_{OL}	Bus Output Low Voltage	V_{CC} = Min	I_{OL} = 40 mA			0.32	0.5	Volts
			I_{OL} = 70 mA			0.41	0.7	
			I_{OL} = 100 mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = Max	V_O = 0.4 V				−50	μA
			V_O = 4.5 V	Military			200	
				Commercial			100	
I_{off}	Bus Leakage Current (Power off)	V_O = 4.5 V					100	μA
V_{TH}	Receiver Input High Threshold	Bus Enable = 2.4 V		Military	2.4	2.0		Volts
				Commercial	2.3	2.0		
V_{TL}	Receiver Input Low Threshold	Bus Enable = 2.4 V		Military		2.0	1.5	Volts
				Commercial		2.0	1.6	
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE								
V_{OH}	Receiver Output High Voltage	V_{CC} = Min, V_{in} = V_{IL} or V_{IH}	Military, I_{OH} = −1.0 mA		2.4	3.4		Volts
			Commercial, I_{OH} = −2.6 mA		2.4	3.4		
	Parity Output High Voltage	V_{CC} = Min, I_{OH} = −660 μA, V_{in} = V_{IH} or V_{IL}		Military	2.5	3.4		
				Commercial	2.7	3.4		
V_{OL}	Output Low Voltage (Except Bus)	V_{CC} = Min, V_{in} = V_{IL} or V_{IH}	I_{OL} = 4.0 mA			0.27	0.4	Volts
			I_{OL} = 8.0 mA			0.32	0.45	
			I_{OL} = 12 mA			0.37	0.5	
V_{IH}	Input High Level (Except Bus)	Guaranteed input logical High for all inputs			2.0			Volts
V_{IL}	Input Low Level (Except Bus)	Guaranteed input logical Low for all inputs		Military			0.7	Volts
				Commercial			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = Min, I_{in} = −18 mA					−1.2	Volts
I_{IL}	Input Low Current (Except Bus)	V_{CC} = Max, V_{in} = 0.4 V					−0.36	mA
I_{IH}	Input High Current (Except Bus)	V_{CC} = Max, V_{in} = 2.7 V					20	μA
I_{in}	Input High Current (Except Bus)	V_{CC} = Max, V_{in} = 5.5 V					100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = Max			−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All inputs = Gnd				75	110	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = Max	V_O = 2.4 V				20	μA
			V_O = 0.4 V				−20	

NOTES: 1. For conditions shown as Min or Max, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

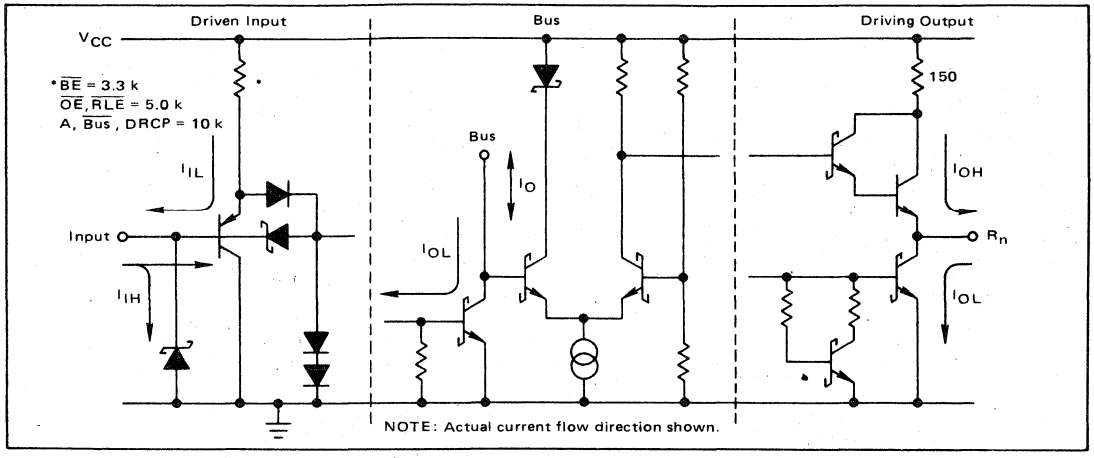
SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameter	Description	Test Conditions	MC2907XM			MC2907XC			Unit
			Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (Bus) = 50 pF	–	21	40	–	21	36	ns
t_{PLH}		R_L (Bus) = 50 Ω	–	21	40	–	21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus		–	13	26	–	13	23	ns
t_{PLH}			–	13	26	–	13	23	
t_s	A Data Inputs	C_L = 15 pF	25	–	–	23	–	–	ns
t_h		R_L = 2.0 k	8.0	–	–	7.0	–	–	
t_{PW}	Clock Pulse Width (High)		28	–	–	25	–	–	ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)		–	18	37	–	18	34	ns
t_{PHL}			–	18	37	–	18	34	
t_{PLH}	Latch Enable to Receiver Output		–	21	37	–	21	34	ns
t_{PHL}			–	21	37	–	21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21	–	–	18	–	–	ns
t_h			7.0	–	–	5.0	–	–	
t_{PLH}	A or B Data to Odd Parity (Driver Enabled)		–	21	40	–	21	36	ns
t_{PHL}			–	21	40	–	21	36	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibited)		–	21	40	–	21	36	ns
t_{PHL}			–	21	40	–	21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output		–	21	40	–	21	36	ns
t_{PHL}			–	21	40	–	21	36	
t_{ZH}	Output Control to Output		–	14	28	–	14	25	ns
t_{ZL}			–	14	28	–	14	25	
t_{HZ}	Output Control to Output	C_L = 5.0 pF	–	14	28	–	14	25	ns
t_{LZ}		R_L = 2.0 k	–	14	28	–	14	25	

LOGIC DIAGRAM



INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

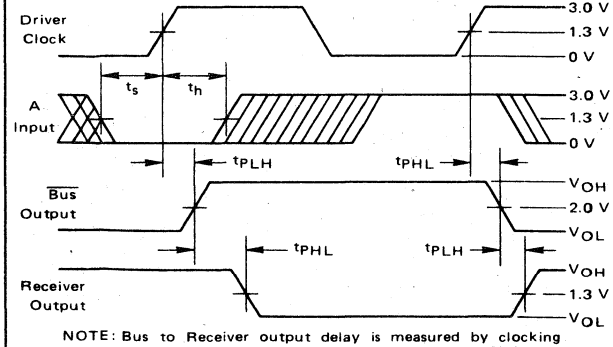


FUNCTION TABLE

		Inputs			Internal to Device		Bus	Output	
A_n	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_n	Q_n	B_n	R_n	Function
X	X	H	X	X	X	X	H	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = High Z = High impedance X = Don't care
L = Low NC = No change ↑ = Low-to-high transition

SWITCHING WAVEFORMS

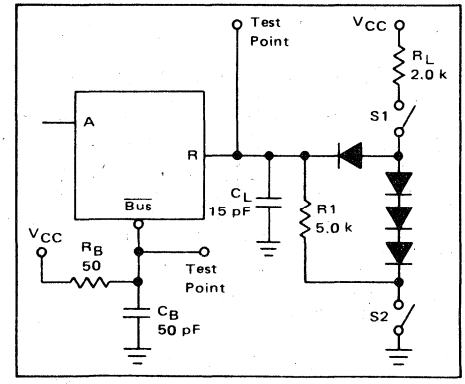


NOTE: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{Bus}$ to R combinatorial delay.

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD Parity Output
L	ODD = A0 ⊕ A1 ⊕ A2 ⊕ A3
H	ODD = Q0 ⊕ Q1 ⊕ Q2 ⊕ Q3

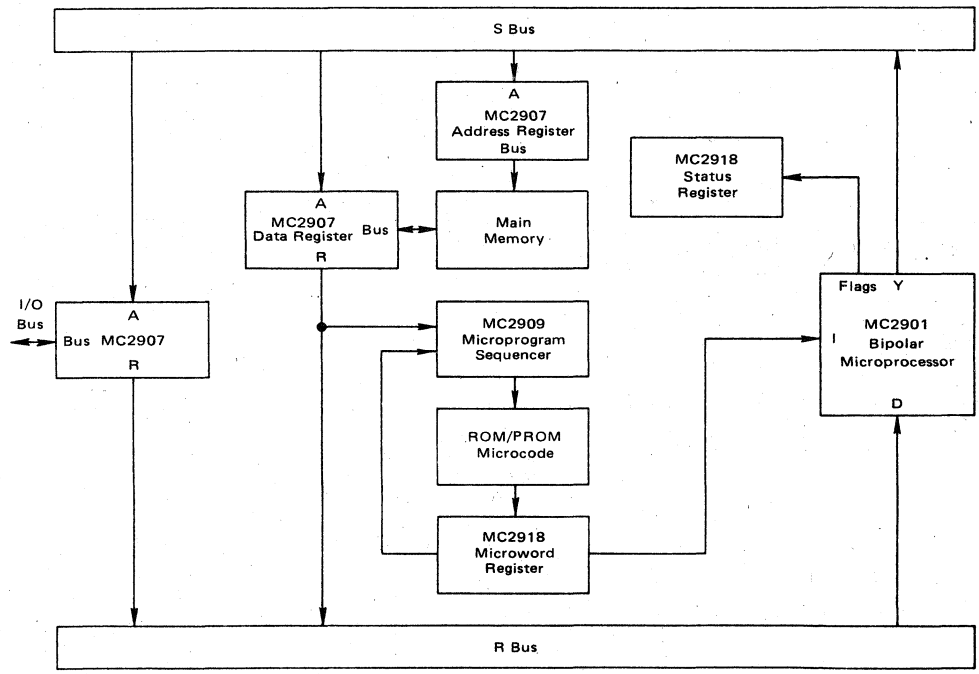
LOAD TEST CIRCUIT



DEFINITIONS OF FUNCTIONAL TERMS

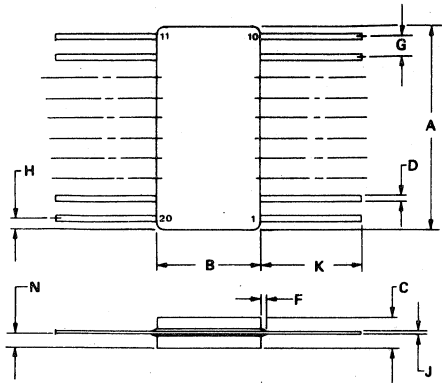
DRCP	Driver Clock Pulse. Clock pulse for the driver register.
$\overline{BE}$	$\overline{Bus\ Enable}$. When the Bus Enable is Low, the four drivers are in the high impedance state.
$\overline{Bus0}$, $\overline{Bus1}$, $\overline{Bus2}$, $\overline{Bus3}$	The four driver outputs and receiver inputs (data is inverted).
R0, R1, R2, R3	The four receiver outputs. Data from the bus is inverted while data from the A input is non-inverted.
$\overline{RLE}$	$\overline{Receiver\ Latch\ Enable}$. When $\overline{RLE}$ is Low, data on the Bus inputs is passed through the receiver latches. When $\overline{RLE}$ is High, the receiver latches are closed and will retain the data independent of all other inputs.
ODD	Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high impedance state.
$\overline{OE}$	$\overline{Output\ Enable}$. When the $\overline{OE}$ input is High, the four three-state receiver outputs are in the high impedance state.

APPLICATIONS



The MC2907 can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed microprocessor systems.

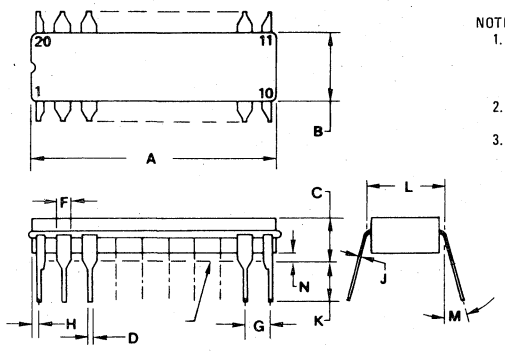
PACKAGE DIMENSIONS



NOTE:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

CASE 737

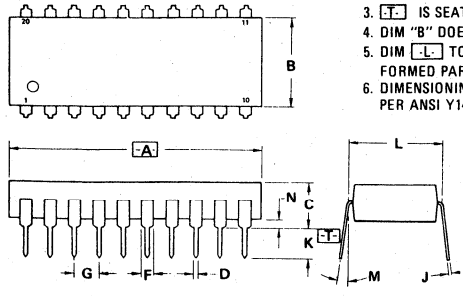
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	13.08	–	0.515
B	5.84	6.60	0.230	0.260
C	1.52	2.16	0.060	0.085
D	0.41	0.46	0.016	0.018
F	–	0.25	–	0.010
G	1.27 BSC		0.050 BSC	
H	1.14	1.40	0.045	0.055
J	0.08	0.13	0.003	0.005
K	–	9.14	–	0.360
N	–	1.02	–	0.040



NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

CASE 732

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	24.38	25.15	0.960	0.990
B	6.86	7.49	0.270	0.295
C	4.32	5.08	0.170	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	5°	15°	5°	15°
N	0.51	0.76	0.020	0.030



NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS;
   ⌖ ø 0.25 (0.010)Ⓜ T AⓂ
3. -T- IS SEATING PLANE.
4. DIM "B" DOES NOT INCLUDE MOLD FLASH.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

CASE 738

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.65	27.18	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.94	4.19	0.155	0.165
D	0.38	0.56	0.015	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	2.79	3.56	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

MOTOROLA Semiconductors

MC2909
MC2911

TTL
MICROPROGRAM SEQUENCER

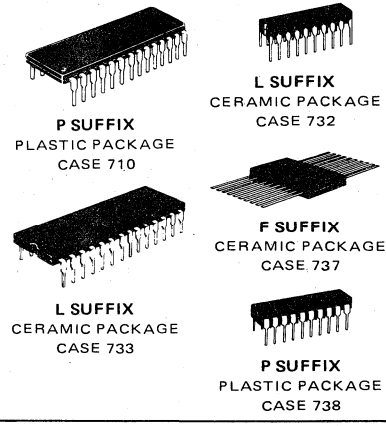
MICROPROGRAM SEQUENCER

The MC2909 is a four-bit-wide address controller intended for sequencing through a series of microinstructions contained in a ROM or PROM. Two MC2909s may be interconnected to generate a twelve-bit address (4K words).

The MC2909 can select an address from any of four sources. They are: 1) a set of external direct inputs (D); 2) external data from the R inputs, stored in an internal register; 3) a four-word-deep push/pop stack; or 4) a program counter register (which usually contains the last address plus one). The push/pop stack includes certain control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs can be OR'ed with an external input for conditional skip or branch instructions, and a separate line forces the outputs to all zeroes. The outputs are three-state.

The MC2911 is an identical circuit to the MC2909, except the four OR inputs are removed and the D and R inputs are tied together. The MC2911 is in a 20-pin, 0.3" centers package.

- 4-Bit Slice Cascadable to Any Number of Microwords
- Internal Address Register
- Branch Input for N-Way Branches
- Cascadable 4-Bit Microprogram Counter
- 4 X 4 File with Stack Pointer and Push/Pop Control for Nesting Microsubroutines
- Zero Input for Returning to the Zero Microcode Word
- Individual OR Input for Each Bit for Branching to Higher Microinstructions
- Three-State Outputs
- All Internal Registers Change State on the Low-to-High Transition of the Clock



P SUFFIX
PLASTIC PACKAGE
CASE 710

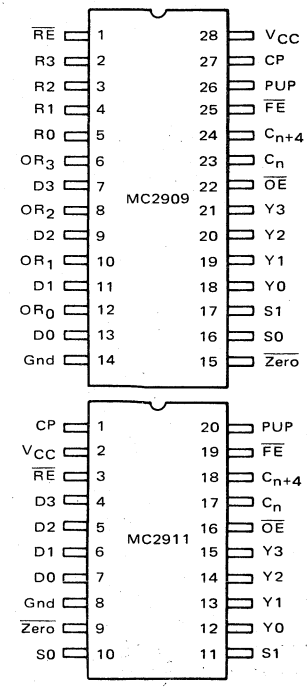
L SUFFIX
CERAMIC PACKAGE
CASE 732

F SUFFIX
CERAMIC PACKAGE
CASE 737

L SUFFIX
CERAMIC PACKAGE
CASE 733

P SUFFIX
PLASTIC PACKAGE
CASE 738

PIN ASSIGNMENTS



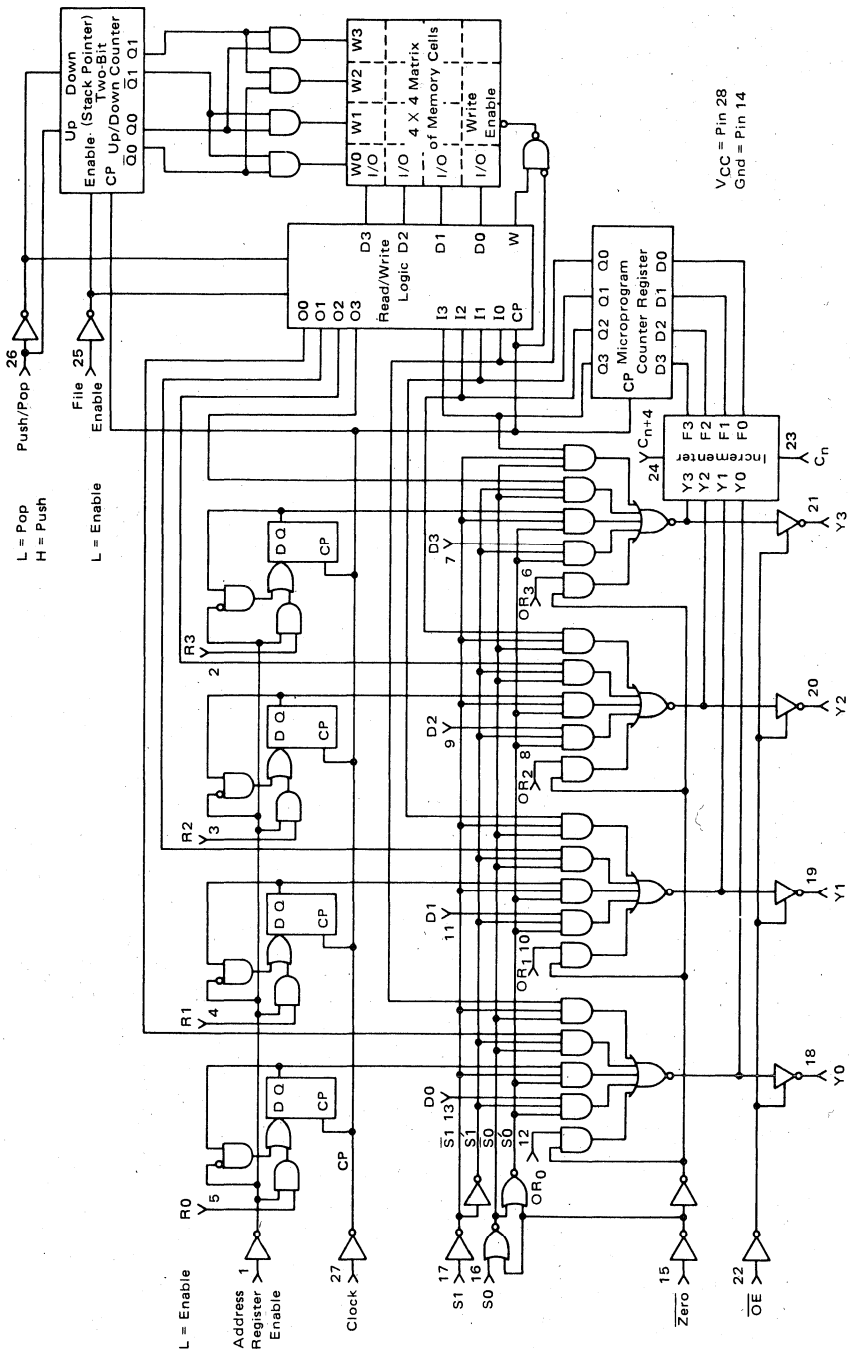
MAXIMUM RATINGS (above which the useful life may be impaired)	
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ORDERING INFORMATION

Package Type	Temperature Range	MC2909 Order Number	MC2911 Order Number
Molded DIP	0°C to +70°C	MC2909PC	MC2911PC
Hermetic DIP	0°C to +70°C	MC2909LC	MC2911LC
Hermetic DIP	−55°C to +125°C	MC2909LM	MC2911LM
Hermetic Flat Pak	−55°C to +125°C	–	MC2911FM

DS 9521

FIGURE 1 – MC2909 MICROPROGRAM SEQUENCER BLOCK DIAGRAM



The MC2911 is an IDENTICAL circuit to the MC2909, except the four OR inputs are removed and the D and R inputs are tied together. The MC2911 is in a 20-pin Dual-in-Line package. See Figure 11.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output High Voltage	V_{CC} = Min, V_{in} = V_{IH} or V_{IL}	Military	I_{OH} = −1.0 mA	2.4	–	–	Volts
			Commercial	I_{OH} = −2.6 mA	2.4	–	–	
V_{OL}	Output Low Voltage	V_{CC} = Min, V_{in} = V_{IH} or V_{IL}	I_{OL} = 4.0 mA		–	–	0.4	Volts
			I_{OL} = 8.0 mA		–	–	0.45	
			I_{OL} = 12 mA (Note 5)		–	–	0.5	
V_{IH}	Input High Level	Guaranteed input logical High voltage for all inputs			2.0	–	–	Volts
V_{IL}	Input Low Level	Guaranteed input logical Low voltage for all inputs		Military	–	–	0.7	Volts
				Commercial	–	–	0.8	
V_I	Input Clamp Voltage	V_{CC} = Min, I_{in} = −18 mA			–	–	−1.5	Volts
I_{IL}	Input Low Current	V_{CC} = Max, V_{in} = 0.4 V	C_n		–	–	−1.08	mA
			Push/Pop, OE		–	–	−0.72	
			Others (Note 6)		–	–	−0.36	
I_{IH}	Input High Current	V_{CC} = Max V_{in} = 2.7 V	C_n		–	–	40	μA
			Push/Pop		–	–	40	
			Others (Note 6)		–	–	20	
I_I	Input High Current	V_{CC} = Max V_{in} = 7.0 V	C_n, Push/Pop		–	–	0.2	mA
			Others (Note 6)		–	–	0.1	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = Max	Y0−Y3		−30	–	−100	mA
			C_{n+4}		−30		−85	
I_{CC}	Power Supply Current	V_{CC} = Max (Note 4)			–	80	130	mA
I_{OZL} I_{OZH}	Output Off Current	V_{CC} = Max, OE = 2.7 V	V_{Out} = 0.4 V		–	–	−20	μA
			V_{Out} = 2.7 V		–	–	20	

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Apply Gnd to C_n, R0, R1, R2, R3, OR_0, OR_1, OR_2, OR_3, D0, D1, D2, and D3. Other inputs open. All outputs open. Measured after a Low-to-High clock transition.
5. The 12 mA output applies only to Y0, Y1, Y2, and Y3.
6. For the MC2911, D_i and R_i are interanlly connected. Loading is doubled (to same values as Push/Pop).

Operating Range	Part Numbers	Power Supply	Temperature Range
Commercial	MC2909PC, LC MC2911PC, LC	5.0 V ± 5%	T_A = 0°C to +70°C
Military	MC2909LM MC2911LM MC2911FM	5.0 V ± 10%	T_C = −55°C to +125°C

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Tables 1, 2, and 3 define the timing characteristics of the MC2909 and MC2911 over the operating voltage and temperature range. The tables are divided into three types of parameters: clock characteristics, combinational delays from inputs to outputs, and setup and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e., clock Low-to-High transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5 V with V_{IL} = 0 V and V_{IH} = 3.0 V. For three-state disable tests, C_L = 5.0 pF and measurement is to 0.5 V change on output voltage level.

TABLE 1 – CYCLE TIME AND CLOCK CHARACTERISTICS

Time	Commercial	Military
Minimum Clock Low Time	30	35
Minimum Clock High Time	30	35

TABLE 2 – MAXIMUM COMBINATIONAL PROPAGATION DELAYS

All in ns, C_L = 50 pF (except output disable tests)

From Input	Commercial		Military	
	Y	C_{n+4}	Y	C_{n+4}
D_i	17	30	20	32
S0, S1	30	48	40	50
OR_i	17	30	20	32
C_n	–	14	–	16
$\overline{Zero}$	30	48	40	50
$\overline{OE}$ Low (Enable)	25	–	25	–
$\overline{OE}$ High (Disable)	25	–	25	–
Clock ↑ S1,S0 = LH	43	55	50	62
Clock ↑ S1,S0 = LL	43	55	50	62
Clock ↑ S1,S0 = HL	80	95	90	102

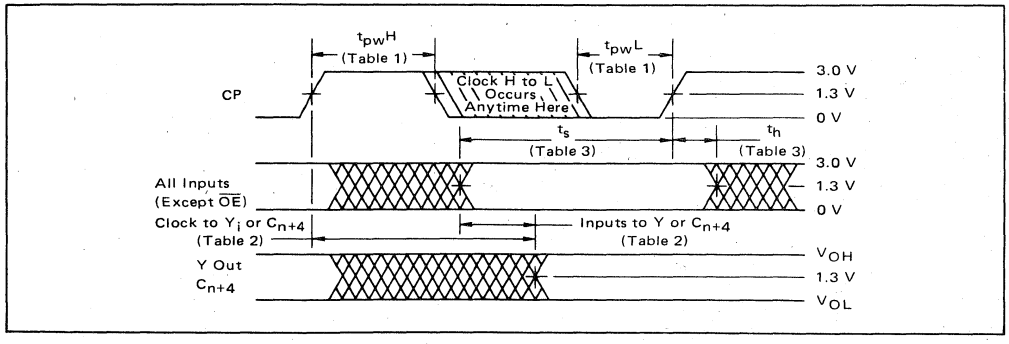
TABLE 3 – GUARANTEED SETUP AND HOLD TIMES

All in ns (Note 1)

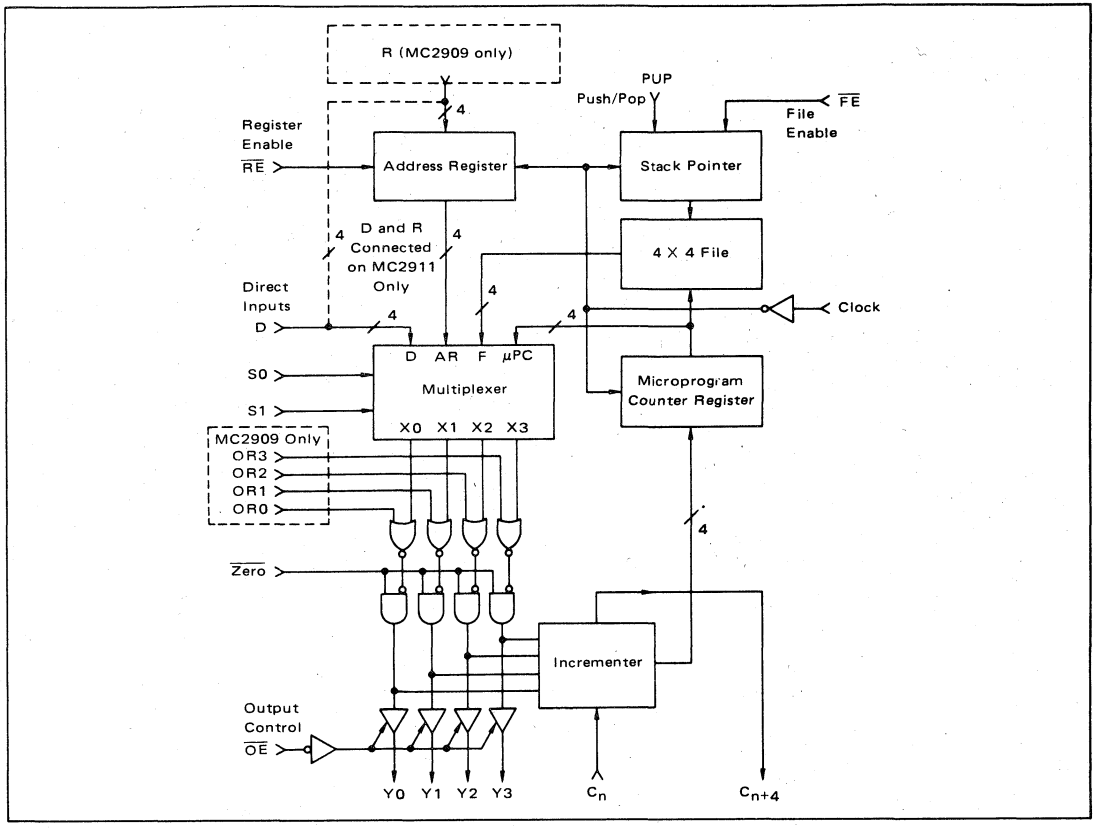
From Input	Notes	Commercial		Military	
		Setup Time	Hold Time	Setup Time	Hold Time
$\overline{RE}$		22	5	22	5
R_i	2	10	5	12	5
Push/Pop		26	6	30	7
$\overline{FE}$		26	5	30	5
C_n		28	5	30	5
D_i	2	30	0	35	3
OR_i		30	0	35	3
S0, S1		45	0	50	0
$\overline{Zero}$		45	0	50	0

NOTES: 1. All times relative to clock Low-to-High transition.
2. On MC2911, R_i and D_i are internally connected together and labeled D_i. Use R_i setup and hold times when D inputs are used to load register.

FIGURE 2 – SWITCHING WAVEFORMS
(See Tables for Specific Values)



MICROPROGRAM SEQUENCER



ARCHITECTURE OF THE MC2909/MC2911

The MC2909/MC2911 are bipolar microprogram sequencers intended for use in high-speed microprocessor applications. The device is a cascadable 4-bit slice such that two devices allow addressing of up to 256-words of microprogram and three devices allow addressing of up to 4K words of microprogram. A detailed logic diagram is shown in Figure 1.

The device contains a four-input multiplexer that is used to select either the address register, direct inputs, microprogram counter, or file as the source of the next microinstruction address. This multiplexer is controlled by the S0 and S1 inputs.

The address register consists of four D-type, edge-triggered flip-flops with a common clock enable. When the address register enable is Low, new data is entered into the register on the clock Low-to-High transition. The address register is available at the multiplexer as a source for the next microinstruction address. The direct input is a 4-bit field of inputs to the multiplexer and can be selected as the next microinstruction address. On the MC2911, the direct inputs are also used as inputs to the register. This allows an N-way branch where N is any word in the microcode.

The MC2902/MC2911 contains a microprogram counter (μPC) that is composed of a 4-bit incrementer followed by a 4-bit register. The incrementer has carry-in (C_n) and carry-out (C_{n+4}) such that cascading to larger word lengths is straightforward. The μPC can be used in either of two ways. When the least significant carry-in to the incrementer is High, the microprogram register is loaded on the next clock cycle with the current Y output word plus one (Y + 1 → μPC). Thus sequential microinstructions can be executed. If this least significant C_n is Low, the incrementer passes the Y output word unmodified and the microprogram reigster is loaded with the same Y word on the next clock cycle (Y → μPC). Thus, the same microinstruction can be executed any number of times by using the least significant C_n as the control.

The last source available at the multiplexer input is the 4 X 4 file (stack). The file is used to provide return address linkage when executing microsubroutines. The file contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a push or pop.

The stack pointer operates as an up/down counter with separate push/pop and file enable inputs. When the file enable input is Low and the push/pop input is High, the Push operation is enabled. This causes the stack pointer to increment and the file to be written with the required return linkage—the next microinstruction address following the subroutine jump which initiated the Push.

If the file enable input is Low and the push/pop control is Low, a Pop operation occurs. This implies the usage of the return linkage during this cycle and thus a return from subroutine. The next Low-to-High clock transition causes the stack pointer to decrement. If the file enable is High, no action is taken by the stack pointer regardless of any other input.

The stack pointer linkage is such that any combination of pushes, pops, or stack references can be achieved. One microinstruction subroutine can be performed. Since the stack is four words deep, up to four microsubroutines can be nested.

The $\overline{Zero}$ input is used to force the four outputs to the binary zero state. When the $\overline{Zero}$ input is Low, all Y outputs are Low regardless of any other inputs (except $\overline{OE}$). Each Y output bit also has a separate OR input such that a conditional logic one can be forced at each Y output. This allows jumping to different microinstructions on programmed conditions.

The MC2909/MC2911 feature three-state Y outputs. These can be particularly useful in military designs requiring external Ground Support Equipment (GSE) to provide automatic checkout of the microprocessor. The internal control can be placed in the high-impedance state, and preprogrammed sequences of microinstructions can be executed via external access to the control ROM/PROM.

OPERATION OF THE MC2902/MC2911

Table 4 lists the select codes for the multiplexer. The two bits applied from the microword register (and additional combinational logic for branching) determine which data source contains the address for the next microinstruction. The contents of the selected source will appear on the Y outputs. Table 4 also shows the truth table for the output control and for the control of the push/pop stack. Table 5 shows in detail the effect of S0, S1, $\overline{FE}$ and PUP on the MC2909. These four signals define what address appears on the Y outputs and what

TABLE 4

ADDRESS SELECTION

Octal	S1	S0	Source for Y Outputs	Symbol
0	L	L	Microprogram Counter	μPC
1	L	H	Address Register	AR
2	H	L	Push/Pop Stack	STK0
3	H	H	Direct Inputs	D_i

OUTPUT CONTROL

OR_i	$\overline{Zero}$	$\overline{OE}$	Y_i
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S0,S1

Z = High Impedance

SYNCHRONOUS STACK CONTROL

$\overline{FE}$	PUP	Push/Pop Stack Change
H	X	No Change
L	H	Incrementer Stack Pointer, then Push Current PC onto STK0
L	L	Pop Stack (Decrement Stack Pointer)

the state of all the internal registers will be following the clock Low-to-High edge. In this illustration, the microprogram counter is assumed to contain initially some word J, the address register some word K, and the four words in the push/pop stack contain R_a through R_d.

Table 6 illustrates the execution of a subroutine using the MC2909. The configuration of Figure 3 is assumed. The instruction being executed at any given time is the one contained in the microword register (μWR). The contents of the μWR also controls (indirectly, perhaps) the four signals S0, S1, $\overline{FE}$, and PUP. The starting address of the subroutine is applied to the D inputs of the MC2909 at the appropriate time.

In the columns on the left is the sequence of microinstructions to be executed. At address J+2, the sequence control portion of the microinstruction contains the command "Jump to the subroutine at A". At the time T2, this instruction is in the μWR and the MC2909 inputs are setup to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the μWR and appears on the Y outputs. The first instruction of the subroutine, I(A), is accessed and is at the inputs of the μWR. On the next clock transistion, I(A) is loaded into the μWR for execution, and the return address J+3 is pushed onto the stack. The return instruction is executed at T5. Table 7 is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction.

TABLE 5 – OUTPUT AND INTERNAL NEXT-CYCLE REGISTER STATES FOR MC2909/MC2911

Cycle	S1, S0, $\overline{FE}$, PUP	μPC	AR	STK0	STK1	STK2	STK3	Y_{Out}	Comment	Principal Use
N	0000	J	K	Ra	Rb	Rc	Rd	J	Pop Stack	End Loop
N+1	–	J+1	K	Rb	Rc	Rd	Ra	–		
N	0001	J	K	Ra	Rb	Rc	Rd	J	Push μPC	Setup Loop
N+1	–	J+1	K	J	Ra	Rb	Rc	–		
N	001X	J	K	Ra	Rb	Rc	Rd	J	Continue	Continue
N+1	–	J+1	K	Ra	Rb	Rc	Rd	–		
N	0100	J	K	Ra	Rb	Rc	Rd	K	Pop Stack; Use AR for Address	End Loop
N+1	–	K+1	K	Rb	Rc	Rd	Ra	–		
N	0101	J	K	Ra	Rb	Rc	Rd	K	Push μPC; Jump to Address in AR	JSR AR
N+1	–	K+1	K	J	Ra	Rb	Rc	–		
N	011X	J	K	Ra	Rb	Rc	Rd	K	Jump to Address in AR	JMP AR
N+1	–	K+1	K	Ra	Rb	Rc	Rd	–		
N	1000	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0; Pop Stack	RTS
N+1	–	Ra+1	K	Rb	Rc	Rd	Ra	–		
N	1001	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0; Push μPC	
N+1	–	Ra+1	K	J	Ra	Rb	Rc	–		
N	101X	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0	Stack Ref (Loop)
N+1	–	Ra+1	K	Ra	Rb	Rc	Rd	–		
N	1100	J	K	Ra	Rb	Rc	Rd	D	Pop Stack; Jump to Address on D	End Loop
N+1	–	D+1	K	Rb	Rc	Rd	Ra	–		
N	1101	J	K	Ra	Rb	Rc	Rd	D	Jump to Address on D; Push μPC	JSR D
N+1	–	D+1	K	J	Ra	Rb	Rc	–		
N	111X	J	K	Ra	Rb	Rc	Rd	D	Jump to Address on D	JMP D
N+1	–	D+1	K	Ra	Rb	Rc	Rd	–		

X = Don't Care, 0 = Low, 1 = High. Assume C_n = High.

TABLE 6 – SUBROUTINE EXECUTION

Control Memory		
Execute Cycle	Microprogram Address	Microprogram Instruction
	J–1	–
T0	J	–
T1	J+1	–
T2	J+2	JSR A
T6	J+3	–
T7	J+4	–
	–	–
	–	–
	–	–
	–	–
	–	–
T3	A	I(A)
T4	A+1	–
T5	A32	RTS
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–

Execute Cycle		T0	T1	T2	T3	T4	T5	T6	T7	T8	T9
Clock											
Signals											
MC2909 Inputs (from μWR)	S1, S0	0	0	3	0	0	2	0	0		
	$\overline{FE}$	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	J+4	J+5		
	STK0	–	–	–	J+3	J+3	J+3	–	–		
	STK1	–	–	–	–	–	–	–	–		
	STK2	–	–	–	–	–	–	–	–		
	STK3	–	–	–	–	–	–	–	–		
MC2909 Output	Y	J+1	J+2	A	A+1	A+2	J+3	J+4	J+5		
ROM Output	(Y)	I(J+1)	**JSR A**	I(A)	I(A+1)	**RTS**	I(J+3)	I(J+4)	I(J+5)		
Contents of μWR (Instruction Being Executed)	μWR	I(J)	I(J+1)	**JSR A**	I(A)	I(A+1)	**RTS**	I(J+3)	I(J+4)		

C_n = High

TABLE 7 – TWO NESTED SUBROUTINES

Routine B is Only One Instruction.

Control Memory		
Execute Cycle	Microprogram Address	Microprogram Instruction
	J–1	–
T0	J	–
T1	J+1	–
T2	J+2	JSR A
T9	J+3	–
	–	–
	–	–
	–	–
	–	–
T3	A	–
T4	A+1	–
T5	A+2	JSR B
T7	A+3	–
T8	A+4	RTS
	–	–
	–	–
	–	–
	–	–
T6	B	RTS
	–	–

Execute Cycle		T0	T1	T2	T3	T4	T5	T6	T7	T8	T9
Clock		⊓	⊓	⊓	⊓	⊓	⊓	⊓	⊓	⊓	⊓
Signals											
MC2909 Inputs (from μWR)	S1, S0	0	0	3	0	0	3	2	0	2	0
	$\overline{FE}$	H	H	L	H	H	L	L	H	L	H
	PUP	X	X	H	X	X	H	L	X	L	X
	D	X	X	Z	X	X	B	X	X	X	X
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	B+1	A+4	A+5	J+4
	STK0	–	–	–	J+3	J+3	J+3	A+3	J+3	J+3	–
	STK1	–	–	–	–	–	–	J+3	–	–	–
	STK2	–	–	–	–	–	–	–	–	–	–
	STK3	–	–	–	–	–	–	–	–	–	–
MC2909 Output	Y	J+1	J+2	A	A+1	A+2	B	A+3	A+4	J+3	J+4
ROM Output	(Y)	I(J+1)	**JSR A**	I(A)	I(A+1)	**JSR B**	**RTS**	I(A+3)	**RTS**	I(J+3)	I(J+4)
Contents of μWR (Instruction Being Executed)	μWR	I(J)	I(J+1)	**JSR A**	I(A)	I(A+1)	**JSR B**	**RTS**	I(A+3)	**RTS**	I(J+3)

C_n = High

DEFINITION OF TERMS

A set of symbols is used in this data sheet to represent various internal and external registers and signals used with the MC2909/MC2911. Since its principle application is as a controller for a microprogram store, it is necessary to define some signals associated with the microcode itself. Figure 3 illustrates the basic interconnection of MC2909, memory, and microinstruction register. The definitions here apply to this architecture.

Inputs to MC2909/MC2911

S1, S0 Control lines for address source selection

$\overline{FE}$, PUP Control lines for push/pop stack

$\overline{RE}$ Enable line for internal address register

OR_i Logic OR inputs on each address output line

$\overline{Zero}$ Logic AND input on the output lines

$\overline{OE}$ Output Enable. When $\overline{OE}$ is High, the Y outputs are Off (high impedance)

C_n Carry-in to the incrementer

R_i Inputs to the internal address register

D_i Direct inputs to the multiplexer

CP Clock input to the AR and μPC register and Push/Pop stack

Outputs from the MC2909/MC2911

Y_i Address outputs from MC2909. (Address inputs to control memory.)

C_{n+4} Carry out from the incrementer

Internal Signals

μPC Contents of the microprogram counter

AR Contents of the address register

STK0–STK3 Contents of the push/pop stack. By definition, the word in the four-by-four file, addressed by the stack pointer is STK0. Conceptually, data is pushed into the stack at STK0; a subsequent push moves STK0 to STK1; a pop implies STK3 → STK2 → STK1 → STK0. Physically, only the stack pointer changes when a push or pop is performed. The data does not move. I/O occurs at STK0.

SP Contents of the stack pointer

External to the MC2909/MC2911

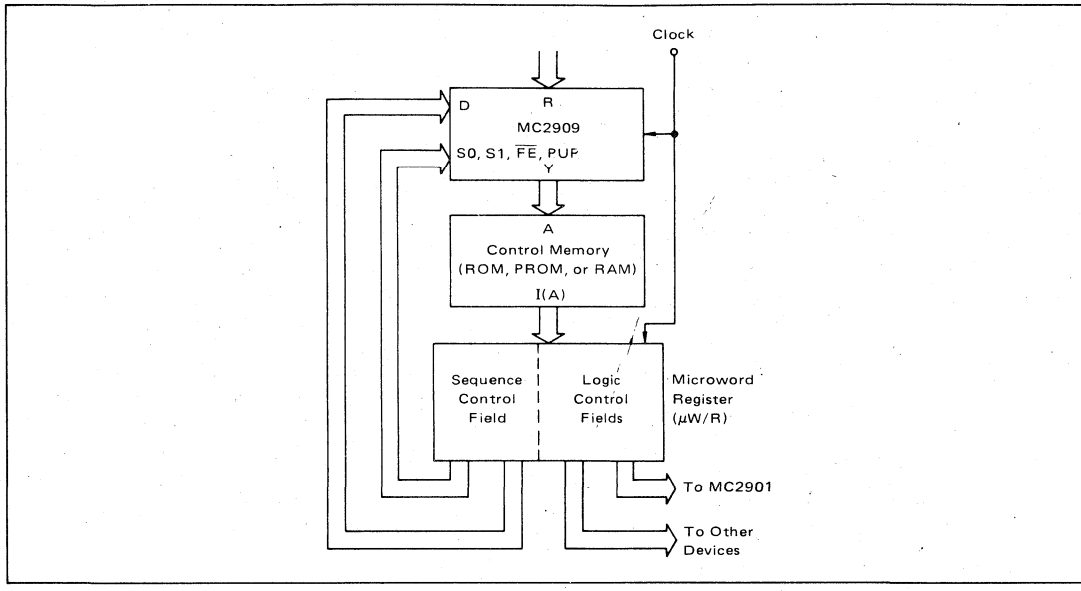
A Address to the control memory

I(A) Instruction in control memory at address A

μWR Contents of the microword register (at output of control memory). The microword register contains the instruction currently being executed.

T_n Time period (cycle) n

FIGURE 3 – MICROPROGRAM SEQUENCER CONTROL



USING THE MC2909/11

The computer control unit (CCU) is generally the single most complicated subsystem in today's digital computer. A CCU is complicated from the conceptualization, design, and implementation viewpoints, because it is the subsystem that controls the internal buses and subsystems of the processor, synchronizes internal and external events, and grants or denies permission to external systems. The MC2909 Microprogram Sequencer is an excellent mechanism for simplifying the CCU design task.

Computer Architecture

A classical computer architecture is shown in Figure 4. The data bus is commonly used by all of the subsystems in the computer. Information, instructions, address operands, data and sometimes control signals are transmitted down the data bus under control of a microprogram. The microprogram selects the source of the data as well as the destination(s) of the data. In a more complicated system there may be a number of data buses.

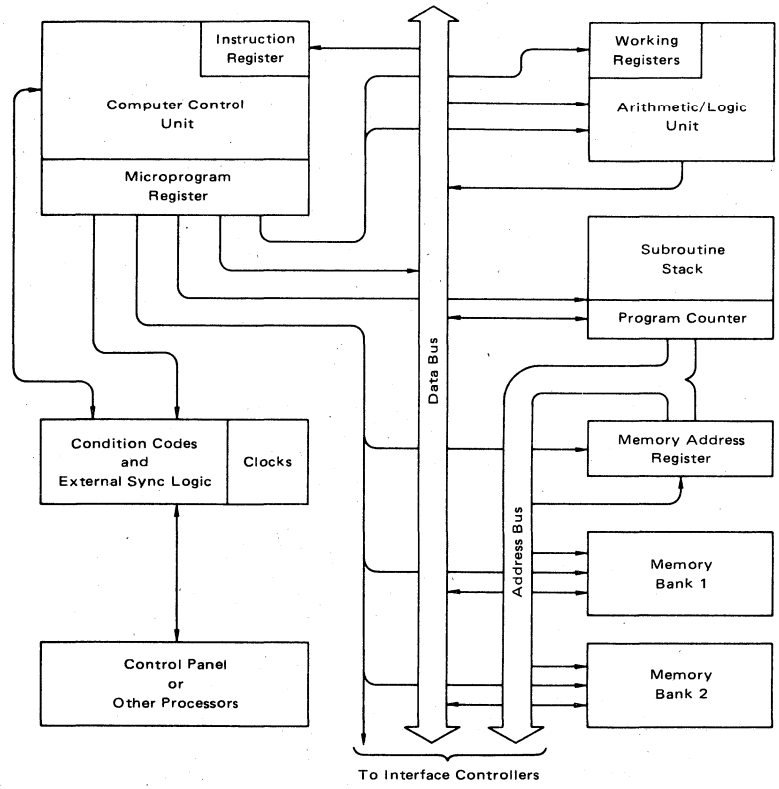
The address bus is typically used to select a word in memory for an internal computer function, or to select an input/output port for an external subsystem or peripheral function. Also selected by microprogram command, the source of the data for the address bus may be the program counter, the memory address reigster, a direct memory address controller, an interface controller, etc.

The arithmetic/logic unit (ALU) is actually that portion of the processor that computes. Depending upon the complexity of the ALU, a large number of different arithmetic functions can be accomplished in various number systems using different representations of those data. The most common minimum sets, however, are the functions (A plus B), (A minus B), and (B minus A) performed in fixed point, two's complement binary form where A and B are the ALU inputs. The logical functions are obtained from the same combinatorial logic array that is used for the arithmetic functions, but it is gated in a different manner. The minimum logical function capability will be (A OR B), (A AND B), and (A EXCLUSIVE-OR B). In addition to these combinatorial logic functions, there are sets of shift and rotate instructions that complete the basic instruction set.

The ALU provides a set of condition codes as a result of the current arithmetic or logical function. These condition codes include such variables as carry-out, A = B, the sign bit, result equals zero, etc. The condition codes, along with other computer status information, are stored in a register for later use by the programmer or computer control unit.

Third generation processors also provide for a general-purpose register set that is available to the programmer to be used to hold variables that are used often—passing arguments to subroutines, referencing memory indirectly,

FIGURE 4 – GENERALIZED COMPUTER ARCHITECTURE



etc. Depending on the architecture of the machine, the general-purpose registers may be selected directly from the operands in the instruction register from an address in the microprogram store, or one of the two sources as determined by a bit in the microprogram store.

The program counter and the memory address register are the two main sources of memory word and I/O address select data on the address bus. The program counter contains the address of the next instruction or instruction operand that is to be fetched from main memory, and the memory address register contains instruction address operands that are necessary to fetch the data required for the execution of the current instruction.

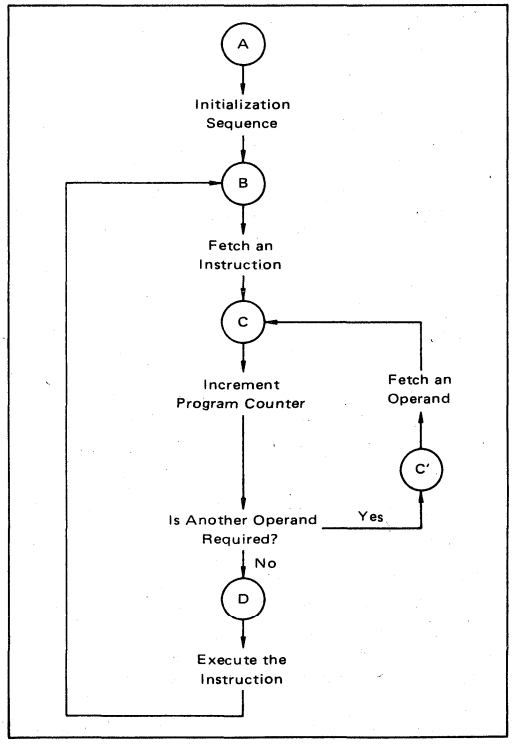
A subroutine address stack is provided to allow the return address linkage to the handled easily when exiting a subroutine. The address stack is a last-in, first-out stack that is controlled by a jump-to-subroutine, Push, or a return-from-subroutine, Pop, instruction from the CCU microprogram word.

Main memory poses an interesting set of problems to computer designers. Random access memory is typically slower than the computer control unit or arithmetic logic unit speed. And, on the other hand, read only memory may be much faster than the control process. The same set of problems is presented to the system by peripheral devices and processes. The computer control unit contends with these problems as well as the problems of synchronizing asynchronous events.

The Control Sequence

The computer control unit contains an instruction register, microprogram storage, and usually a microprogram register. Figure 5 presents a state diagram for a typical computer control unit. The first state of any processor must be an initialization sequence, regardless of its level of complexity or sophistication. The purpose of the initialization sequence is to place all of the system control storage elements in a known state such that control of the process can be started in an orderly manner. For example, registers, condition code, flag, and carry/link flip-flops are either preset to logic "1" or cleared to logic "0". Sometimes a sequence of events takes place such as the initialization of sets of register stacks or main memory. Also, because some peripheral equipment may be involved that may be damaged by randomly changing states at its interface, very close attention must be given to the initialization process within the CCU state machine. A further requirement of this initialization pocess is that clock pulses must be withheld from the initialized hardware in some manner until the initialization procedure is completed.

FIGURE 5 – SIMPLE COMPUTER CONTROL UNIT STATE TRANSITION DIAGRAM



The initialization sequence is usually started by one of three events: application of primary power to the system; either a programmed or operator generated "Master Reset" command; or, an error that the state machine cannot recover from, but can detect. In a power-up generated initialization sequence, care must be given to the circuit that detects the event and generates the timed reset signal. The various power supply filters and loads must be considered as the state machine sequence should not be allowed to start until the entire power system is stable. Furthermore, since some equipment and components may be damaged if they required multiple voltages that are not applied in the proper order, the computer control unit quite often is used to sequence the enabling of power supplies.

State "B" is the first computer minor cycle period. (A minor cycle is one primary clock period in length; characteristically, one microinsturction is executed. A major cycle is composed of one or more minor cycles and describes the completion of a macroinstruction or macroprocessors, i.e., "Add" or "Interrupt".) During this state, the processor may be interrupted, halted, paused, or—in the absence of any of these requests—the computer control unit will fetch a macroinstruction from main memory and load it into the instruction register.

Subsequently, during state "C", the Program Counter will be incremented and the instruction previously fetched will be decoded. If another operand is required for the current instruction, state "C" will be executed the necessary number of times, and the operands will be loaded into the appropriate registers until the requirements of the instruction have been satisfied.

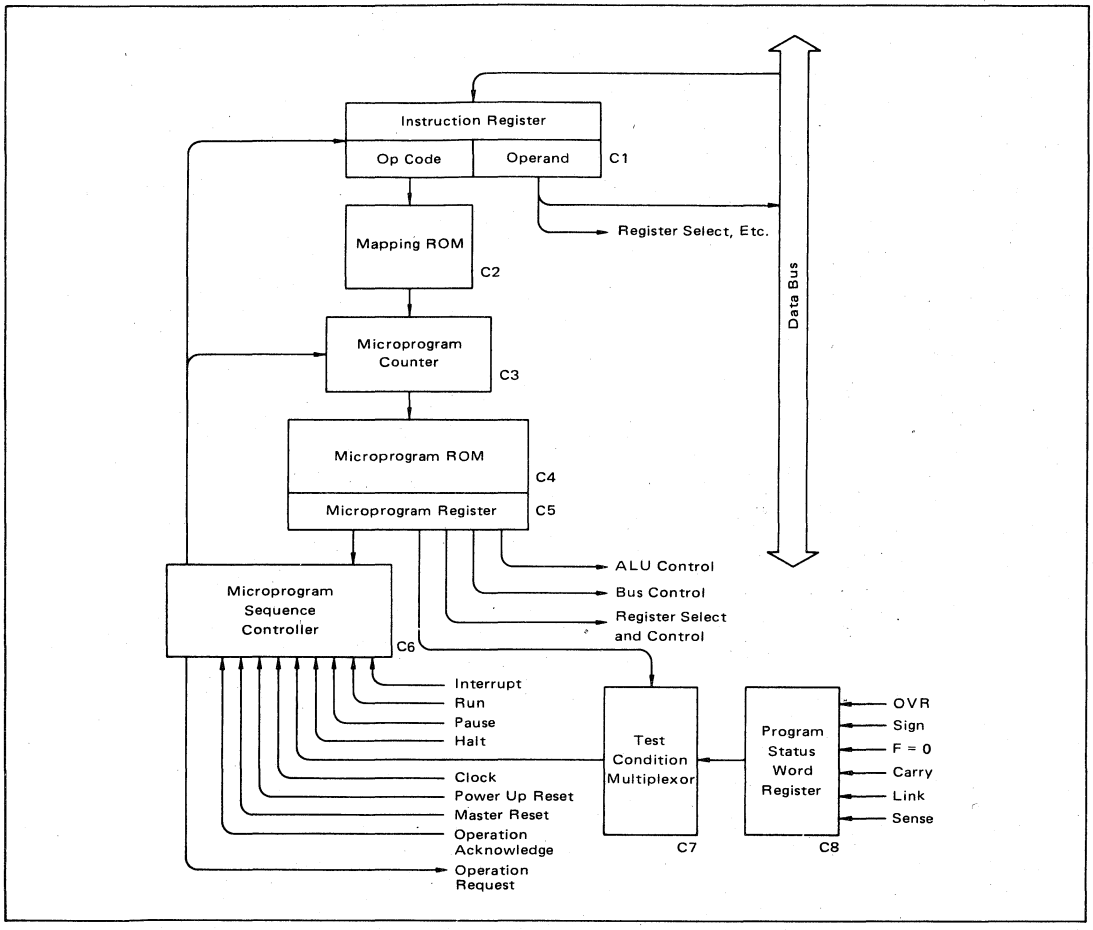
The last state, "D", is where the macroinstruction is executed. As in all of the other states in the process, the instruction execution state may require one or more microinstruction cycles. Having completed this state, control of the CCU will revert to state "B" microcode after a microinstruction branch to the beginning of that sequence has been effected.

CCU Architecture

A functional representation of a computer control unit is presented in Figure 6. To aid in the diagram reference process, the major subsystem components are labeled with the designations C1, to C8.

The instruction register, C1, receives the instruction from main memory via the data bus. The width of the register is generally the same as the memory word and data bus width to conserve processor overhead time. That is, if one clock period is necessary to fetch an instruction and one clock period is used to execute the instruction, that is a much more efficient use of computer time than requiring two or more clock periods to fetch the instruction and only one clock period to execute it. Any time

FIGURE 6 – COMPUTER CONTROL UNIT ARCHITECTURAL SCHEMATIC



required by the processor over and above the instruction execution time is considered overhead.

An instruction is broken down into two or more fields: the opcode, and one or more operands. An opcode (operation code) is the instruction itself. The operands are data used by the computer control unit the execution of the instruction. For example, an operand might be the number of a selected register, a variable to be compared to the accumulator, the address of an input/output port, etc.

Because the operand may be used as data, it must be presented to the data bus via an open collector or three-state transmitter. The operand and its subfields must also be distributed to the other computer subsystems that it serves such as the register selectors in the arithmetic/logic unit. The decoding and use of the opcode, however, is not as obvious conceptually or from an implementation standpoint.

There is usually more than one microinstruction per macroinstruction. And, different classes of macroinstructions almost always require a different number of microprogram steps. The designer that is interested in a computer with only a few instructions may eliminate some hardware by using the opcode from the instruction register, C1, directly as the starting address of the microprogram ROM, C4. This is not only wasteful of opcodes and inflexible, but it means that any change in the instruction set or microprogram perturbs the entire system. To avoid this problem, a mapping ROM may be used.

The output of the mapping ROM, C2, should be wider than the opcode field that is used as the address input. This allows a greater range of starting address for the microprogram ROM, C4. Because ROM/PROM field widths are typically four or eight bits wide, a reasonable choice of width for the mapping ROM with an 8-bit opcode is twelve bits. The starting address is loaded into the microprogram counter, C3, which points to the first microinstruction in the microprogram ROM. When the output of the microprogram ROM stabilizes, it is loaded into the microprogram register, C5.

The use of the microprogram register in this manner is called pipelining. A pipeline register speeds up a state machine of this sort because it allows the address of the microprogram ROM to be changed and its output to settle, while the current microinstruction is being presented to the computer hardware from the microprogram register.

The microprogram sequence controller, C6, has two basic functions: it synchronizes events external to the CCU with the CCU, and it uses the output of the test condition multiplexer to determine whether or not microprogram branches, jumps to subroutine, and returns from subroutine are to be made.

The external signals in the microprogram sequence controller can be classified into five categories: supervisory, condition codes, initialization, synchronization, interrupts, and clocks. Supervisory signals include Run, Halt, and Pause. Run is a latched signal that enables the clock to the entire computer system. Halt disables the clock from the system, but it is only recognized during the instruction fetch microcycle; it, too, is latched. Pause is a level provided to the controller from an outside processor to temporarily suspend CCU control so that the external processor has uncontended access to the computer's resources. Pause is also only recognized during an instruction fetch microcycle.

Condition codes are stored in the program status word register, C8, and presented to the test condition multiplexer, C7, where any of the codes may be selected by one of the microprogram fields in the microprogram register. If true, the output of the test condition multiplexer will enable a branch instruction in the microprogram. The condition codes are loaded into the program status word register after every ALU operation or interrupt request.

Initialization lines include Power-Up Reset and Master Reset. The use of these lines was covered in some detail above.

The synchronization lines include Operation Request and Operation Acknowledge, OPREQ and OPACK. These signals allow external events that may be slower than the CCU to be synchronized to the CCU. For example, when the CCU issues a memory reference instruction, an OPREQ is also generated, and, although the system clock continues to run, it is disabled from the CCU. When the addressed memory bank has achieved its access time and performed the read or write operation, it must generate an OPACK which will be synchronized with the system clock which will, in turn, enable the clock to the CCU. When the memory or I/O cycle times are known and can be controlled, the CCU clock period can be adjusted to preclude the requirement for synchronizing signals.

An interrupt may occur at any time; however, it is only recognized at an instruction fetch microcycle. At the time the interrupt is allowed, the priority encoded interrupt vector is jammed into the program status word register and the microprogram ROM address is forced to the interrupt service routine address. When the interrupt has been serviced, the microprogram counter is returned to instruction fetch minor cycle address and processing resumes.

CCU Instructions

As implied earlier, there are two types of instructions recognized within the CCU, machine language or macroinstructions, and random logic replacement or microinstructions. Macroinstructions reside in main memory, are fetched and loaded into the instruction register and then decoded into microinstructions which directly control the computer's resources.

An example of two different types of macroinstructions may be seen in Table 8a. A 16-bit instruction was defined with a constant length op code defined in the least significant eight bits of the instruction. The remainder of the instruction word, bits 8 through 15, will be defined as a function of instruction type.

The register-to-register instruction has two operand fields that select the source and destination register, Register A and Register B, respectively. That is, the result of an arithmetic/logic function with Registers A and B will be stored in Register B.

The branch instruction's operand is an 8-bit displacement address. With the condition of the branch implicit in the op code, the sum of the current program counter address and the displacement address will be stored in the program counter, if the selected condition is logically true.

A microinstruction word format is depicted in Table 8b. Four bits, b0–3, are used to define the type of microinstruction being executed. The second field of four bits, b4–7, selects the branch condition, if the microinstruction is a branch instruction; enables the interrupt and pause functions, if the microinstruction is a macroinstruction fetch command; and, disables the interrupts at all other times. The third microinstruction field is composed of two 3-bit subfields which are used to define the

TABLE 8 – EXAMPLE MACRO AND MICROINSTRUCTION FIELDS

a. Macroinstructions

REGISTER-TO-REGISTER

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OP CODE								REG B				REG A			

BRANCH-ON-CONDITION

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OP CODE								DISPLACEMENT							

b. Microinstructions

ALU AND BRANCH ADDRESS BITS											DATA BUS CONTROL					
Function			Source			Destination			External Gating			Source			Destination		
27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10

SYNCHRONIZATION LOGIC									
ALU EN	Op Req	Branch Condition				Sequencer Function			
9	8	7	6	5	4	3	2	1	0

source and the destination of data on the data bus. The remaining 12-bit field is defined either as an arithmetic logic unit control field or as a microprogram branch address field, depending on the microinstruction function. Although there are a number of methods for mapping various types of microinstruction control fields into a microinstruction, this straightforward approach will be followed, for the purpose of an implementation example and only one mapped field function will be assumed: ALU control and branch address.

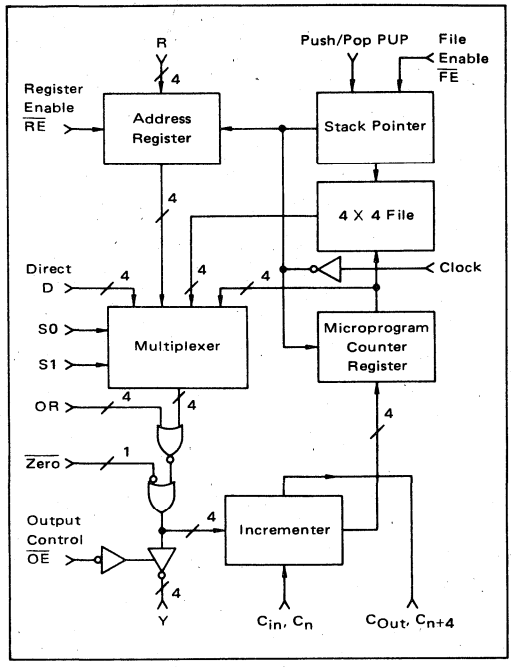
CCU Implementation Using MC2909

As an example, the computer control unit architectural schematic of Figure 6 will be reduced in practice to aid in the illustration of the MC2909 Microprogram Sequencer. The MC2909 is an extremely valuable subsystem component in that it allows the designer to take advantage of the latest microprogramming techniques: microbranching, microsubroutines, and repetitive microinstruction execution. Also, because of the architecture of the component itself, the CCU is inherently faster than a classical implementation of the same function. That is, the classical design may use sequential circuits which must be parallel loaded and sequentially incremented with separate clock pulses, while the MC2909 uses a combinational incrementor outside of the microprogram address bus which is transferred to the microprogram counter on the rising edge of the clock pulse. A detailed specification of the MC2909 is provided in the expanded data sheet and its internal architectural rendering is reproduced here in Figure 7.

The purpose of the MC2909 is to present an address to the microprogram ROM such that a microinstruction may be fetched and executed. In referencing Figure 7, there are four sources of address information available: an address register, a microprogram counter register, a direct or branch input, and a subroutine stack. The address source is chosen by using the one-of-four address multiplexer select lines, S0 and S1. The selected address may then be modified by the OR input lines or the $\overline{\text{Zero}}$ input function before it is presented at the Y address output lines through a three-state buffer.

The OR input lines may be used in one of two manners. Selected OR inputs may be placed at logic "1" which will provide the logical OR of the selected address source and the OR input lines at the Y output. This allows the address to be "masked". If a microprogram instruction of the Skip or Branch classes is being executed and the microinstruction is aligned on an even address microprogram ROM word (the least significant address bit is

FIGURE 7 – MC2909 MICROPROGRAM SEQUENCER ARCHITECTURE



"0"), then the least significant OR input may be controlled by an external test condition multiplexer. If the result of the conditional test was logically false, then the least significant bit may be modified to avoid the execution of the Branch or Skip instruction. All of the unused inputs must be tied to ground. Similarly, if the 2, 3, 4, or n least significant bits of the selected address are "0", the associated OR input lines may be modified for an extended address range skip capability.

Sometimes, in a state machine like a computer control unit, it is desirable to get easily to a predefined state, or address. For instance, if the machine has just been turned on and it is necessary to perform an initialization sequence, or a real-time event occurs where the processor control is required, but the on-going process information may not be destroyed such as an interrupt, the OR inputs may be used. All of the OR inputs must be connected to the output of a positive logic gate so that when the event occurs the output of the gate goes to logical "1", as does the Y output address lines. $\overline{\text{Zero}}$ provides a similar capability, but it must normally be held at logic "1" and only "pulled down" to "0" when the event occurs—causing all of the address output lines to go to "0".

The three-state output buffer that drives the Y-lines may be used nicely to allow automatic test of the memory and register system. That is, if the buffer output control, $\overline{\text{OE}}$, is disabled, the Y-lines go into a high-impedance condition allowing the automatic tester's output lines to be connected directly across the outputs. This capability also allows multiple processors to share the same memory by enabling only one processor's Y-bus at a time.

The address register, as well as all other storage devices on the MC2909, is parallel loaded from the R inputs when the register enable line, $\overline{\text{RE}}$, is low on a positive going clock transition. This is a good register to use when entering the starting address of a microprogram. If selected, the contents of the register are not only presented to the Y outputs, but also to the incrementer.

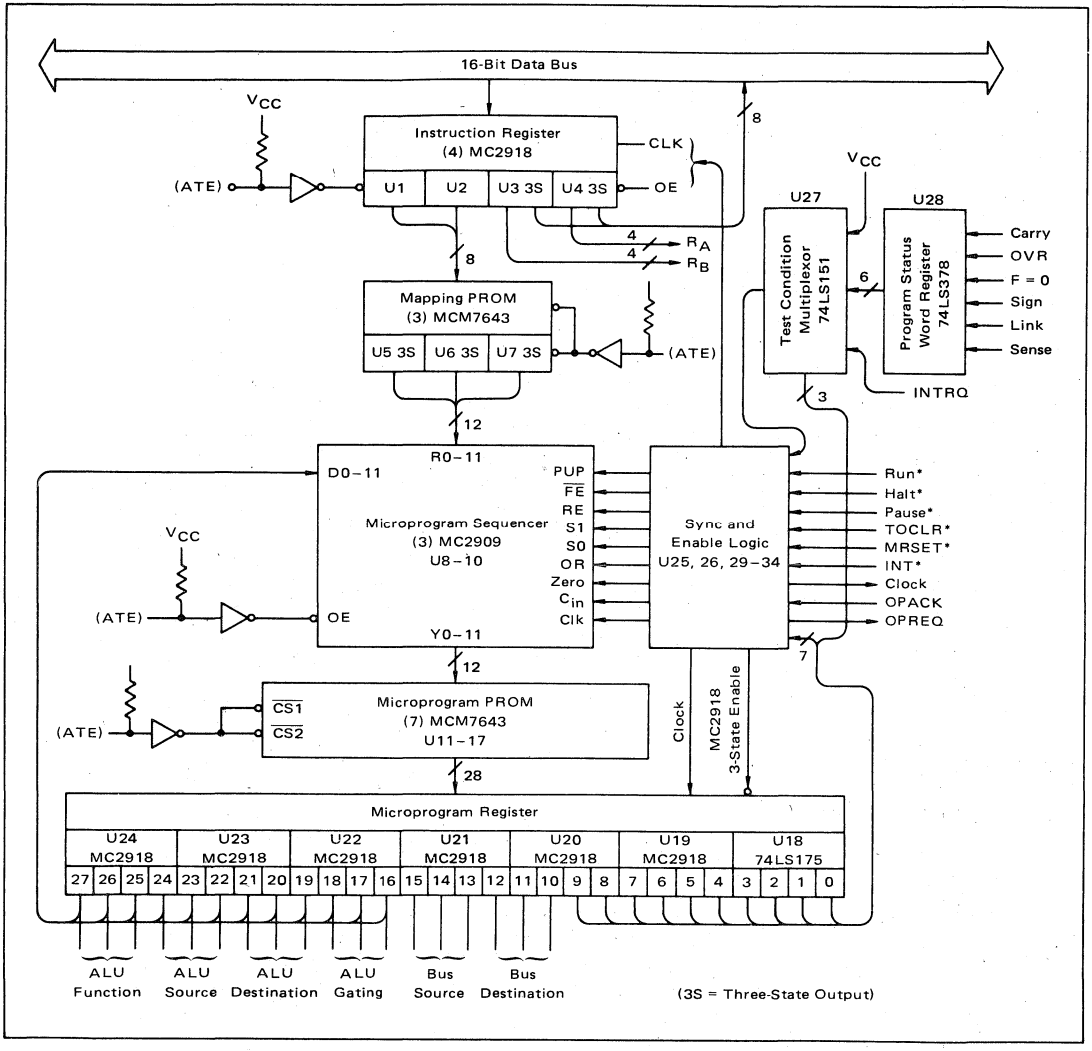
The incrementer is a full-adder provided with an off-chip carry-in signal, C_{in}, and an off-chip carry-out signal, C_{out}, allowing multiple MC2909s to be cascaded. The output from the incrementer is connected to a parallel load input on the microprogram counter register where it is loaded on the rising edge of the next clock pulse. If the microprogram counter is selected as the source address by subsequent microinstructions, it will be incremented by each succeeding clock pulse, thereby stepping through the microprogram.

As described above, it is often valuable to provide a branch instruction and a branch address in a microprogram instruction. The data lines from the branch address field in the microinstrucion may be feedback to the direct input, D, on the MC2909. The source address multiplexer may then select the branch input as the next microinstruction address. This address will be incremented and stored in the microprogram counter register on the next clock pulse which provides the address for the following instruction.

The push/pop, or last-in, first-out stack, allows the microprogrammer to have the same subroutine execution flexibility that machine language programmers have. Heretofore a luxury in almost all computers, microsubroutines may be nested four deep. There is a 4-bit wide by 4-word file whose address is controlled by a 2-bit up/down counter. A push/pop control signal, PUP, determines whether the function being performed is a jump to subroutine, Push, or a return from subroutine, Pop. When the file enable control line, $\overline{\text{FE}}$ is low, the push/pop command will be executed on the next clock pulse rising edge. After the subroutine has been completed, a return to the address immediately following the jump-to-subroutine instruction may be accomplished by selecting the stack as the source address and executing a Pop at the same time.

An example implementation of the computer control unit of Figure 6 using the macro and microinstruction form of Table 8 is depicted in Figure 8. A 16-bit data bus and memory word were assumed as reflected by the instruction register. Four MC2918 4-bit, TTL/three-state

FIGURE 8



output registers, U1–4, are used for the instruction register. The two least significant registers, U1 and U2, contain the op code, while U3 and U4 contain the operand field. The TTL output from the op code register pair is not used, but rather the three-state outputs are connected to the address input of the macroinstruction mapping PROM. If the output enable, OE, of the pair is held low by pulling up the input of an inverter, as shown, then the troubleshooting and automatic testing of the subsystem will be much simpler. In this way, the tester can gain control over the memory system. The three-state output buffers for the operand field are fed back to the eight least significant bits of the data bus so that they may be used to modify the contents of some other register in the system. For ALU functions, the operand field will most likely be used as two 4-bit subfields to specify a source register, R_A, and a source/ destination register, R_B. (In fact, this arrangement works extremely well, if the MC2901 Microprocessor is employed.) The TTL outputs are used for R_A and R_B data.

Selected for their speed and architecture, the mapping PROMs used are three MCM7643s in parallel. With a memory configuration of 256 words by 4 bits, each of the 256 potential op codes has a unique 12-bit starting address which provides the designer with a lot of flexibility for his initial design and an unusally easy task of adding more instructions at a later date.

In turn, the mapping PROM outputs are connected to the address register inputs, R0–11, of the three MC2909 Microprogram Sequencers. The Microprogram Sequencer outputs, Y0–11, provide the address inputs for seven MCM7643 microprogram PROMs. (The output enable lines of the MC2909s should be controlled in the same manner as the instruction register outputs.) Although only 1024 words of microprogram storage are shown, up to 4096 words may be implemented, if necessary. Furthermore, if more than 18-bit microinstruction words are required for the user's task, they may be added as necessary.

The microprogram register consists of one 74LS175 register, U18, and six MC2918 registers, U19–24. The ten least significant bits are used by the synchronization and enable logic. The most significant twelve bits are used for either microsequencer branch address (the TTL outputs of the MC2918s) or for control of the ALU. (The three-state lines are used.) As shown, the ALU control bit fields are specified to control four MC2901s and perform all of the necessary external gating and bit manipulation. The remaining six central bits are provided for data bus source and destination controls and the three-state outputs are used. Whenever the processor is running, the three-state output enable lines are held low, enabling the output. If the processor has been paused, ostensibly for direct memory access, the outputs are disabled so that an external or peripheral processor can gain access to the control line.

The Sync and Enable logic is relatively complex and may be shown better in Figure 9. The two least significant registers in the microprogram registers, U18 and U19, are at the top of the figure. In addition, the remaining two bits from the microprogram register that are used here, ALUEN* and OPREQ, are shown with rectangular boxes around them so that they are easy to see. The control and status bits that emanate from portions of the computer other than the CCU are shown enclosed in ovals. All other signals are generated or used with the CCU.

The four bits stored in microprogram register U18 provide the Microprogram Sequencer function instruction. A 74LS161 was selected for this register because it is synchronous, has an asynchronous clear (enabling power-up reset), and is low-power Schottky. These four bits provide the least significant address bits of an MCM5303 64-word by 8-bit PROM, as well as providing an external event synchronizing signal enable, XSYNC. With XSYNC at logic "1", the external processes that use Pause will be enabled, allowing direct memory access.

The MCM5303 PROM has eight open-collector outputs that must have pull-up resistors added. Seven of the output signals go directly to the three sets of MC2909 control lines. The eighth output line is fed back to enable a gate that drives the fifth PROM address line. The other signal at the AND-gate, U34, is the test condition enable line.

The test condition signal is the result of selecting one of eight processor condition signals using the 74LS151 multiplexer U27. U27 has two outputs, the selected signal and its complement. One of these two signals is selected using (1/2) 74LS51 U29 as the multiplexer. The 4-bit select signal is stored in microprogram register U19. Notice that one of the condition code multiplexer's inputs is tied to V_{CC} which provides for an unconditional branch, if the entire register, U19, is "0". Six of the condition codes (from the ALU) are stored in a 74LS157 register. Every time an ALU function is selected and clocked, as denoted by ALUEN*, the current value of the condition codes are clocked into U28. The eighth condition code bit is the interrupt request signal INTRQ, which is latched externally.

Before proceeding with the rest of the synchronization and enable circuitry, let us consider the programmability aspects of this portion of the state machine. A table of desirable Microprogram Sequencer functions is provided in Table 9. In fact, this table is also the memory map for the Microprogram Sequencer PROM U30. Entries are made in the table by U30 address value. The first 16 entries have the test condition address bit equal to "0". These are the primary instructions; they enable the MC2909 functions. Of the primary instructions, there are only four that have O7, the test condition enable bit set. Three of these are branch instructions and for these microinstructions any condition code may be specified in register U20, except interrupt request, INTRQ. The remaining instruction relates to the macroinstruction fetch process (Figure 5) and only during this microcycle may the CCU be interrupted or paused, as data or instructions moved to system registers under microprogram control may be lost if the microprocess is disturbed. Processed interrupts, by definition, disturb the microprocess and may usurp control of any of the computer's resources.

The only instance when there will be a secondary instruction defined is when bit O7 equals "1" such that, potentially, A5 equals "1". In the event that the condition code test is successful, the four secondary instructions defined in Table 9 will be executed.

If an interrupt was generated during an instruction fetch, the OR output U30,. O6 will assume logic "1". This signal will be logically ANDed by U34 to generate the interrupt acknowledge signal, INTAC. INTRQ or the

FIGURE 9 – SYNC AND ENABLE LOGIC DIAGRAM

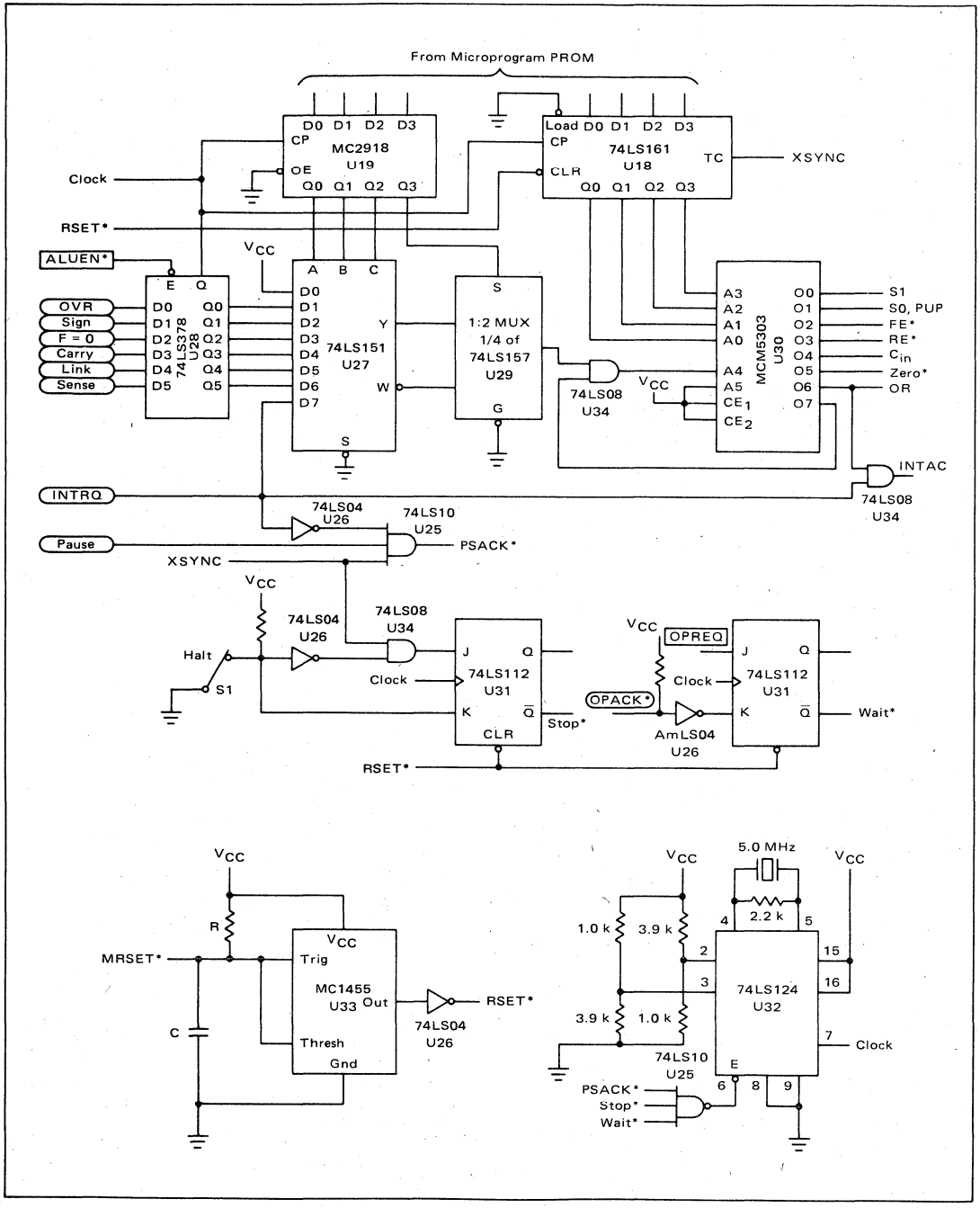


TABLE 9 – MICROSEQUENCER FUNCTION TABLE

Microprogram Sequencer Function						Microprogram Sequencer Control							
						O7	O6	O5	O4	O3	O2	O1	O0
A4	A3	A2	A1	A0	Function Description	Test Enable	OR	$\overline{Zero}$	C_{in}	$\overline{RE}$	$\overline{FE}$	S0, PUP	S1
0	0	0	0	0	Initialize System	L	X	L	H	H	H	X	X
0	0	0	0	1	Branch Test	H	L	H	H	H	H	L	L
0	0	0	1	0	Jump to Subroutine Test	H	L	H	H	H	H	L	L
0	0	0	1	1	Return from Subroutine	H	L	H	H	H	H	L	L
0	0	1	0	0	Execute Program	L	L	H	H	H	H	L	L
0	0	1	0	1	External Carry Control	L	L	H	*	H	H	L	L
0	0	1	1	0		L	L	H	H	H	H	L	L
0	0	1	1	1		L	L	H	H	H	H	L	L
0	1	0	0	0		L	L	H	H	H	H	L	L
0	1	0	0	1	This Group Undefined	L	L	H	H	H	H	L	L
0	1	0	1	0		L	L	H	H	H	H	L	L
0	1	0	1	1		L	L	H	H	H	H	L	L
0	1	1	0	0		L	L	H	H	H	H	L	L
0	1	1	0	1		L	L	H	H	H	H	L	L
0	1	1	1	0	Load Mapped (Starting) Address	L	L	H	H	L	H	H	L
0	1	1	1	1	Fetch Instruction	H	L	H	H	H	H	L	L
1	0	0	0	0	This State Undefined	L	–	–	–	–	–	–	–
1	0	0	0	1	Execute Branch	H	L	H	H	H	H	H	H
1	0	0	1	0	Execute Jump	H	L	H	H	H	L	H	H
1	0	0	1	1	Execute Return	H	L	H	H	H	L	L	H
1	0	1	0	0		L	–	–	–	–	–	–	–
1	0	1	0	1		L	–	–	–	–	–	–	–
1	0	1	1	0		L	–	–	–	–	–	–	–
1	0	1	1	1		L	–	–	–	–	–	–	–
1	1	0	0	0		L	–	–	–	–	–	–	–
1	1	0	0	1	This State Undefined	L	–	–	–	–	–	–	–
1	1	0	1	0		L	–	–	–	–	–	–	–
1	1	0	1	1		L	–	–	–	–	–	–	–
1	1	1	0	0		L	–	–	–	–	–	–	–
1	1	1	0	1		L	–	–	–	–	–	–	–
1	1	1	1	0		L	–	–	–	–	–	–	–
1	1	1	1	1	Service Interrupt or Pause	H	H	H	H	H	H	X	X

*Value of this Bit depends on Logic Implementation. See Text.

absence of the granting of the external synchronization signal, XSYNC, that is generated during the instruction fetch, will preclude the pause acknowledge signal, PSACK*.

An attempt to Halt the processor using an external switch S1 will also be denied unless the current micro-instruction cycle is a macroinstruction fetch. Starting the processor by moving switch S1 to the Run position will always be granted and synchronized by U31, because by definition the processor stopped previously at an instruction fetch cycle, which is also the first state which must be executed when the processor is turned on. If Stop, the Q output of U31 is logic "0", the processor will Halt.

Provision has been made to synchronize the relatively fast CCU with relatively slow memory or input/output functions. If a microinstruction causes memory or I/O reference, the microprogrammer must set the OPREQ bit true. This signal is latched up in the second half of flip-flop U31 and stops the processor (Wait = "0") until the address device acknowledges the operation is complete or the data is ready, by pulling down the OPACK* line. U31 synchronizes the event and restarts the processor.

We have discussed a "hard" processor interrupt event, INTRQ, a "soft" interrupt (one where the state of the processor is not disturbed, but operation is suspended), Pause, starting and stopping the processor, Run and Halt, and synchronizing the processor with external events, OPREQ/OPACK*. Let us consider the system clock and system initialization.

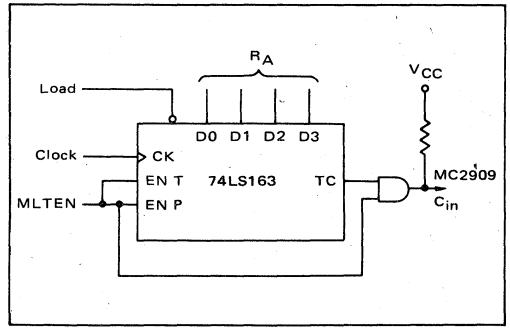
A good choice for a system oscillator is the 74LS124, U32. This device is a dual voltage-controlled oscillator whose timing may be derived by a series mode, fundamental frequency crystal or an RC timing circuit. For high-speed digital circuits, it is necessary to use a crystal.

The output of the oscillator is free running and is presented to an on-chip pulse synchronizer controlled by the enable line of the chip. No partial pulses can be passed by the synchronizer so that control of the oscillator's enable line may be asynchronous. A Pause, Halt, or OPREQ will cause the gated oscillator to shut off until the process is allowed to restart.

Initialization of a state machine is very important. When the power is applied to the system, the system must be disabled until all of the power supply filters have charged and the regulators stabilized. Also, critical storage devices must be preset to a known state. To accomplish this, an MC1455 timer circuit U33 with output buffer U26 is used. The RC value should yield a time-out circuit increment greater than 100 ms in most systems (t = 1.1 RC for this device). Also, by using an external switch or open collector gate to ground an MRSET*, the entire system may be master reset without cycling the power supply off and then on again. Other than clearing flip-flops, the output of the intialization circuit RSET* clears the microprogram register U19. By referring to Table 9 again, it can be seen that microsequencer function A0–3 = 0 provides system initiation, in that U30 output bit O5, Zero*, is low, thereby setting the initial microprogram address to zero and incrementing from there. This allows an initialization microprogram to be stored in the bottom of memory.

The ability to execute the same microinstruction a number of times was referred to previously. Generally, the value of this capability lies outside of the CCU. As an example, let us reconsider the macroinstruction format for a Register-to-Register instruction (Table 8). If the op code is a Shift or Rotate instruction, it would be desirable to allow the programmer to move the data word over a range of one to sixteen bit positions with a single instruction, rather than having to execute the same instruction many times. Since there are two operand subfields, R_A and R_B, let us define the 4-bit value in R_A as the number of bit positions we wish to move the data, and R_B as the general-purpose register that will be affected. (The additional hardware to implement the circuit is shown in Figure 10.)

FIGURE 10 – ITERATIVE MICROINSTRUCTION CONTROL CIRCUIT EXAMPLE



The value in R_A must be parallel loaded into a 4-bit binary counter that has a terminal count flag, TC (when Q0 = Q1 = Q2 = Q3 = 1, TC = 1), such as the 74LS163. The MC2909 control signal RE* that loads the address register must also be applied to the 74LS163 signal LOAD*. Clock is merely the system clock, and MLTEN is a signal that must be supplied by the microprogram to enable this function. MLTEN and TC are connected to an open-collector AND-gate which pulls downthe MC2909 carry-in line until terminal count has been achieved. As a result, the microprogram address does not change until TC equals "1" and then C_{in} equals "1", which increments the microprogram counter, causing the next instruction to be executed. The number of reasons for using this feature are almost unlimited, as are the means to implement the function.

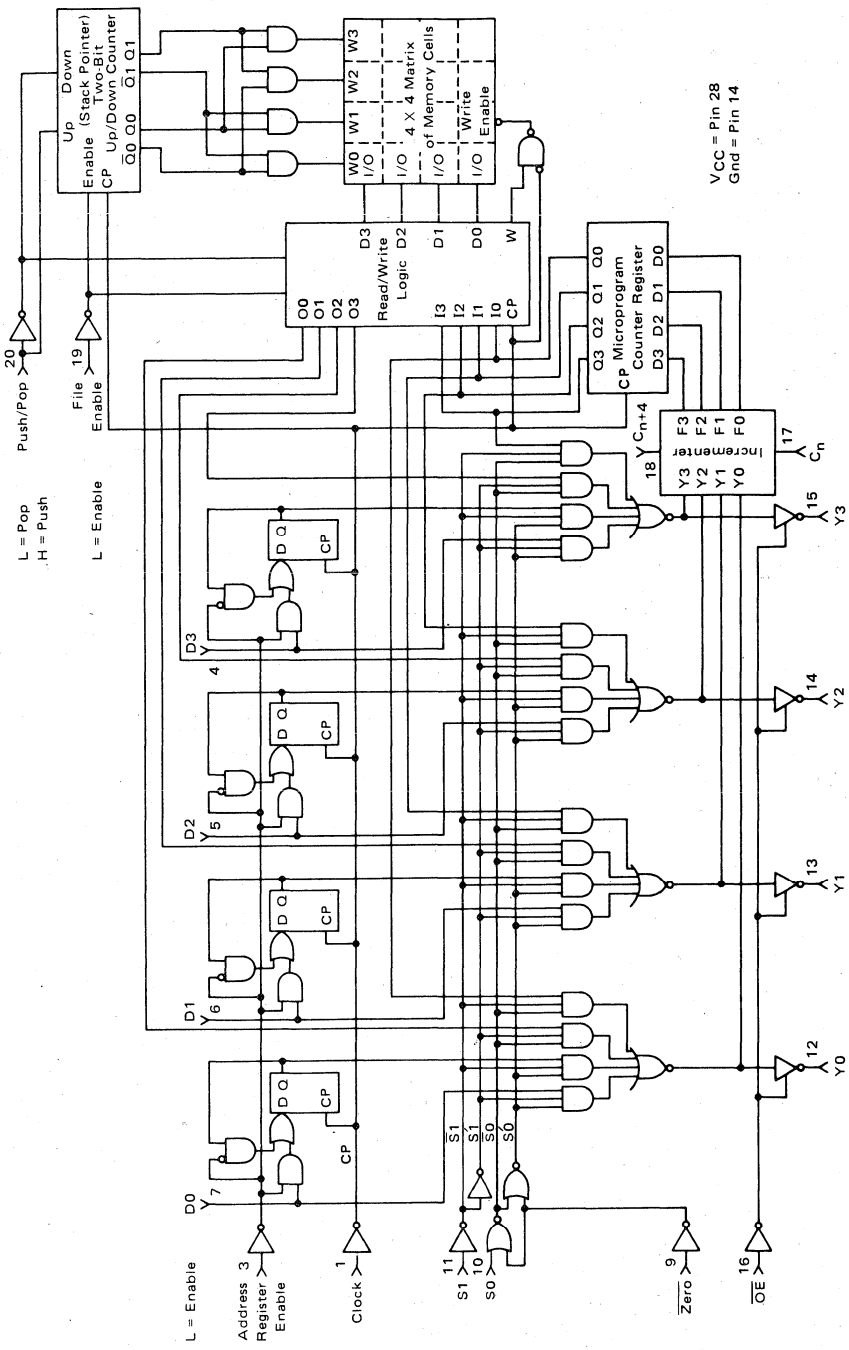
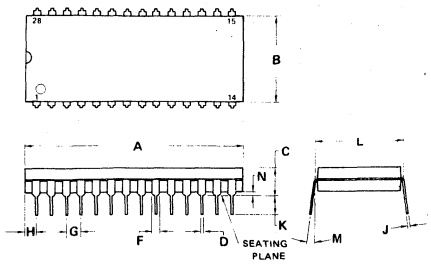


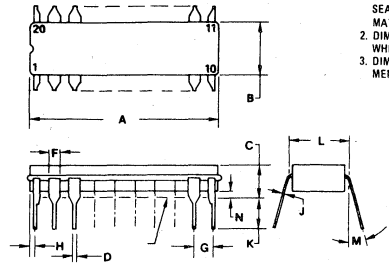
FIGURE 11 – MC2911 MICROPROGRAM SEQUENCER BLOCK DIAGRAM

PACKAGE DIMENSIONS



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	36.32	37.34	1.430	1.470
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

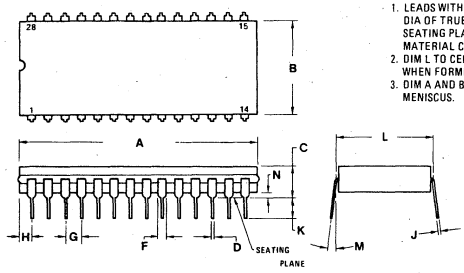
CASE 710-01



NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	24.38	25.15	0.960	0.990
B	6.86	7.49	0.270	0.295
C	4.32	5.08	0.170	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	5°	15°	5°	15°
N	0.51	0.76	0.020	0.030

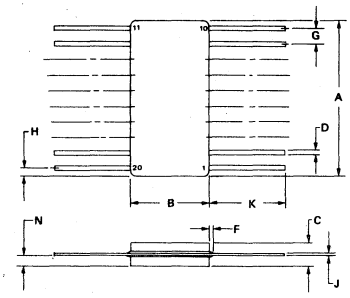
CASE 732-02



NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION OF SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	36.83	37.59	1.450	1.480
B	12.70	13.46	0.500	0.530
C	5.08	5.84	0.200	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54	BSC	0.100	BSC
H	2.03	2.29	0.080	0.090
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24	BSC	0.600	BSC
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

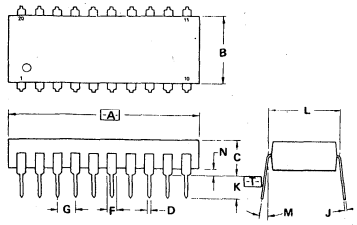
CASE 733-01



NOTE:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	–	13.08	–	0.515
B	5.84	6.60	0.230	0.260
C	1.52	2.16	0.060	0.085
D	0.41	0.46	0.016	0.018
F	–	0.25	–	0.010
G	1.27 BSC		0.050 BSC	
H	1.14	1.40	0.045	0.055
J	0.08	0.13	0.003	0.005
K	–	9.14	–	0.360
N	–	1.02	–	0.040

CASE 737-01



CASE 738-01

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	25.65	27.18	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.94	4.19	0.155	0.165
D	0.38	0.56	0.015	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	2.79	3.56	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. DIM [-A-] IS DATUM.
2. POSITIONAL TOL FOR LEADS;
   [⌖] ø 0.25 (0.010) Ⓜ T [A] Ⓜ
3. [-T-] IS SEATING PLANE.
4. DIM "B" DOES NOT INCLUDE MOLD FLASH.
5. DIM [-L-] TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

MOTOROLA *Semiconductor Products Inc.*

MOTOROLA Semiconductors

MC2910

Product Preview

TTL

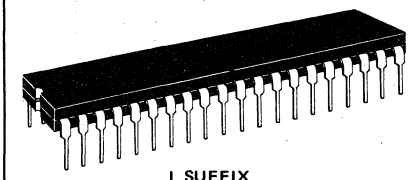
MICROPROGRAM CONTROLLER

MICROPROGRAM CONTROLLER

The MC2910 Microprogram Controller is an address sequencer intended for controlling the sequence of execution of microinstructions stored in microprogram memory. Besides the capability of sequential access, it provides conditional branching to any microinstruction within its 4096-microword range. A last-in, first-out stack provides microsubroutine return linkage and looping capability; there are five levels of nesting of microsubroutines. Microinstruction loop count control is provided with a count capacity of 4096.

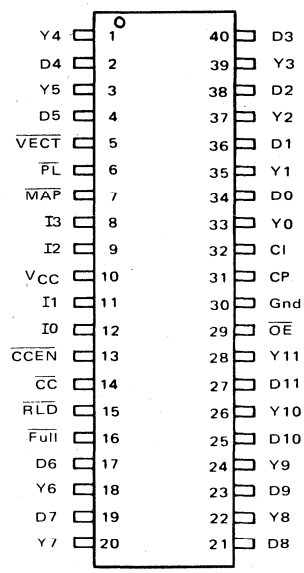
During each microinstruction, the Microprogram Controller provides a 12-bit address from one of four sources: 1) the microprogram address register, μPC, which usually contains an address one greater than the previous address; 2) an external (direct) input, D; 3) a register/counter, R, retaining data loaded during a previous microinstruction; or, 4) a five-deep last-in, first-out stack, F.

- **Twelve Bits Wide**
  Address up to 4096 words of microcode with one chip. All internal elements are a full 12 bits wide.
- **Internal Loop Counter**
  Pre-settable 12-bit down-counter for repeating instructions and counting loop iterations.
- **Four Address Sources**
  Microprogram address may be selected from microprogram counter, branch address bus, five-level push/pop stack, or internal holding register.
- **Sixteen Powerful Microinstructions**
  Executes 16 sequence control instructions, most of which are conditional on external condition input, state of internal loop counter, or both.
- **Output Enable Controls for Three Branch Address Sources**
  Built-in decoder function to enable external devices onto branch address bus. Eliminates external decoder.
- **All Registers Positive Edge-Triggered**
  Simplifies timing problems. Eliminates long setup times.
- **Fast Control from Condition Input**
  Delay from condition code input to address output only 27 ns typical.



L SUFFIX
CERAMIC PACKAGE
CASE 734

PIN ASSIGNMENT



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	0°C to +70°C	MC2910LC
Hermetic DIP	−55°C to +125°C	MC2910LM

This is advance information and specifications are subject to change without notice.

FIGURE 1 – BLOCK DIAGRAM

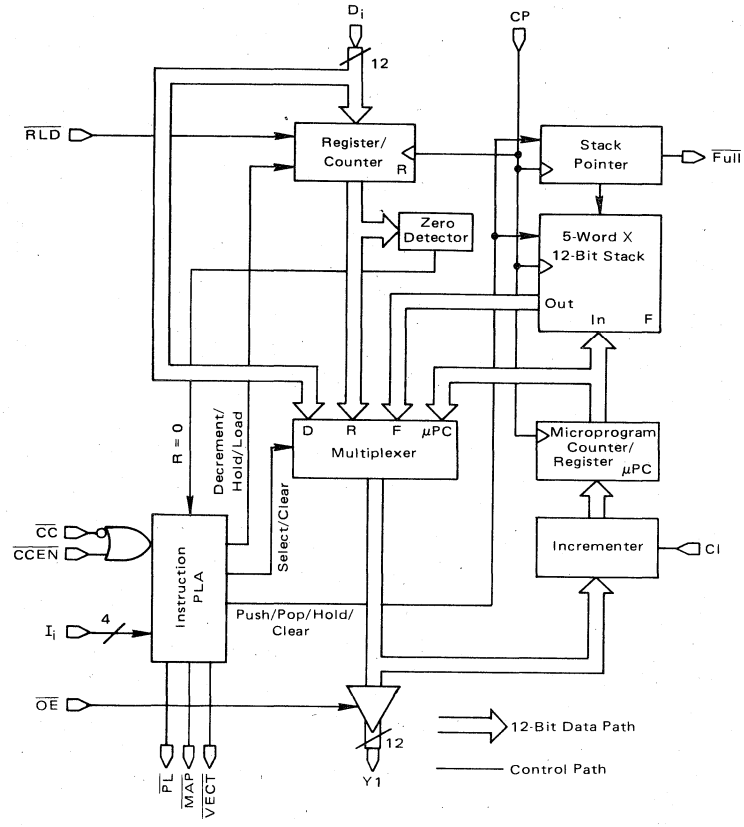


TABLE 1 – INSTRUCTIONS

Hex I3–I0	Mnemonic	Name	Reg/ CNTR Contents	Fail $\overline{CCEN}$ = Low and $\overline{CC}$ = High		Pass $\overline{CCEN}$ = High or $\overline{CC}$ = Low		Reg/ CNTR	Enable
				Y	Stack	Y	Stack		
0	JZ	JUMP ZERO	X	0	Clear	0	Clear	Hold	PL
1	CJS	COND JSB PL	X	PC	Hold	D	Push	Hold	PL
2	JMAP	JUMP MAP	X	D	Hold	D	Hold	Hold	MAP
3	CJP	COND JUMP PL	X	PC	Hold	D	Hold	Hold	PL
4	PUSH	PUSH/COND LD CNTR	X	PC	Push	PC	Push	Note 1	PL
5	JSRP	COND JSB R/PL	X	R	Push	D	Push	Hold	PL
6	CJV	COND JUMP VECTOR	X	PC	Hold	D	Hold	Hold	VECT
7	JRP	COND JUMP R/PL	X	R	Hold	D	Hold	Hold	PL
8	RFCT	REPEAT LOOP, CNTR ≠ 0	≠ 0	F	Hold	F	Hold	Dec	PL
			= 0	PC	Pop	PC	Pop	Hold	PL
9	RPCT	REPEAT PL, CNTR ≠ 0	≠ 0	D	Hold	D	Hold	Dec	PL
			= 0	PC	Hold	PC	Hold	Hold	PL
A	CRTN	COND RTN	X	PC	Hold	F	Pop	Hold	PL
B	CJPP	COND JUMP PL & POP	X	PC	Hold	D	Pop	Hold	PL
C	LDCT	LD CNTR & CONTINUE	X	PC	Hold	PC	Hold	Load	PL
D	LOOP	TEST END LOOP	X	F	Hold	PC	Pop	Hold	PL
E	CONT	CONTINUE	X	PC	Hold	PC	Hold	Hold	PL
F	TWB	THREE-WAY BRANCH	≠ 0	F	Hold	PC	Pop	Dec	PL
			= 0	D	Pop	PC	Pop	Hold	PL

NOTE 1: If $\overline{CCEN}$ = Low and $\overline{CC}$ = High, hold, otherwise load. X = Don't Care

TABLE 2 – PIN FUNCTIONS

Abbreviation	Name	Function
D_i	Direct Input Bit i	Direct input to register/counter and multiplexer. D0 is LSB.
I_i	Instruction Bit i	Selects one of sixteen instructions.
$\overline{CC}$	Condition Code	Used as test criterion. Pass test is a Low on $\overline{CC}$.
$\overline{CCEN}$	Condition Code Enable	Whenever the signal is High, $\overline{CC}$ is ignored and the part operates as through $\overline{CC}$ were true (Low).
CI	Carry-In	Low order carry input to incrementer for microprogram counter.
$\overline{RLD}$	Register Load	When Low forces loading of register/counter, regardless of instruction or condition.
$\overline{OE}$	Output Enable	Three-state control of Y_i outputs.
CP	Clock Pulse	Triggers all internal state changes at Low-to-High edge.
V_{CC}	+5 Volts	
Gnd	Ground	
Y_i	Microrogram Address Bit i	Address to microprogram memory. Y0 is LSB, Y11 is MSB.
$\overline{Full}$	Full	Indicates that five items are on the stack.
$\overline{PL}$	Pipeline Address Enable	Can select #1 source (usually pipeline register) as direct input source.
$\overline{MAP}$	Map Address Enable	Can select #2 source (usually mapping PROM or PLA) as direct input source.
$\overline{VECT}$	Vector Address Enable	Can select #3 source (for example, Interrupt Starting Address) as direct input source.

ARCHITECTURE OF THE MC2910

The MC2910 is a bipolar microprogram controller intended for use in high-speed microprocessor applications. It allows addressing of up to 4K words of microprogram. A block diagram is shown in Figure 1.

The controller contains a four-input multiplexer that is used to select either the register/counter, direct input, microprogram counter, or stack as the source of the next microinstruction address.

The register/counter consists of 12 D-type, edge-triggered flip-flops, with a common clock enable. When its load control, $\overline{RLD}$, is Low, new data is loaded on a positive clock transition. A few instructions include load; in most systems, these instructions will be sufficient, simplifying the microcode. The output of the register/counter is available to the multiplexer as a source for the next microinstruction address. The direct input furnishes a source of data for loading the register/counter.

The MC2910 contains a microprogram counter (μPC) that is composed of a 12-bit incrementer followed by a 12-bit register. The μPC can be used in either of two ways. When the carry-in to the incrementer is High, the microprogram register is loaded on the next clock cycle with the current Y output word plus one ($Y + 1 \rightarrow \mu PC$). Sequential microinstructions are thus executed. When the carry-in is Low, the incrementer passes the Y output word unmodified so that μPC is reloaded with the same Y word on the next clock cycle ($Y \rightarrow \mu PC$). The same microinstruction is thus executed any number of times.

The third source for the multiplexer is the direct (D) input. This source is used for branching.

The fourth source available at the multiplexer input is a 5-word by 12-bit stack (file). The stack is used to provide return address linkage when executing microsubroutines or loops. The stack contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a pop.

The stack pointer operates as an up/down counter. During microinstructions 2, 4, and 5, the PUSH operation is performed. This causes the stack pointer to increment and the file to be written with the required return linkage. On the cycle following the PUSH, the return data is at the new location pointed to by the stack pointer.

During five microinstructions, a POP operation may occur. The stack pointer decrements at the next rising clock edge following a POP, effectively removing old information from the top of the stack.

The stack pointer linkage is such that any sequence of pushes, pops, or stack references can be achieved. At RESET (instruction 0), the depth of nesting becomes zero. For each PUSH, the nesting depth increases by one; for each POP, the depth decreases by one. The depth can grow to five. After a depth of five is reached, $\overline{FULL}$ goes Low. Any further PUSHes onto a full stack overwrite information at the top of the stack, but leave the stack pointer unchanged. This operation will usually destroy useful information and is normally avoided. A POP from an empty stack may place non-meaningful data on the Y outputs, but is otherwise safe. The stack pointer remains at zero whenever a POP is attempted from a stack already empty.

The register/counter is operated during three microinstructions (8, 9, 15) as a 12-bit down counter, with result = zero available as a microinstruction branch test criterion. This provides efficient iteration of microinstructions. The register/counter is arranged such that if it is preloaded with a number N and then used as a loop termination counter, the sequence will be executed exactly N + 1 times. During instruction 15, a three-way branch under combined control of the loop counter and the condition code is available.

The device provides three-state Y outputs. These can be particularly useful in designs requiring automatic checkout of the processor. The microprogram controller outputs can be forced into the high-impedance state, and preprogrammed sequences of microinstructions can be executed via external access to the address lines.

OPERATION

Table 1 shows the result of each instruction in controlling the multiplexer which determines the Y outputs, and in controlling the three enable signals, $\overline{PL}$, $\overline{MAP}$, and $\overline{VECT}$. The effect on the register/counter and the stack after the next positive-going clock edge is also shown. The multiplexer determines which internal source drives the Y outputs. The value loaded into μPC is either identical to the Y output, or else one greater, as determined by CI. For each instruction, one and only one of the three outputs PL, MAP, and VECT is Low. If these outputs control three-state enables for the primary source of microprogram jumps (usually part of a pipeline register), a PROM which maps the instruction to a microinstruction starting location, and an optional third source (often a vector from a DMA or interrupt source), respectively, the three-state sources can drive the D inputs without further logic.

Several inputs, as shown in Table 2, can modify instruction execution. The combination CC High and $\overline{CCEN}$ Low is used as a test in 10 of the 16 instructions. $\overline{RLD}$, when Low, causes the D input to be loaded into the register/counter, overriding any HOLD or DEC operation specified in the instruction. $\overline{OE}$, normally Low, may be forced High to remove the Am2910 Y outputs from a three-state bus.

The stack, a 5-word last-in, first-out 12-bit memory, has a pointer which addresses the value presently on the top of the stack. Explicit control of the stack pointer occurs during instruction 0 (RESET), which makes the stack empty by resetting the SP to zero. After a RESET, and whenever else the stack is empty, the contents of the top of stack is undefined until a PUSH occurs. Any POPs performed while the stack is empty put undefined data on the F outputs and leave the stack pointer at zero.

Any time the stack is full (five more PUSHes than POPs have occurred since the stack was last empty), the $\overline{FULL}$ warning output occurs. This signal first appears on the microcycle after a fifth PUSH. No additional PUSH should be attempted onto a full stack; if tried, information within the stack will be overwritten and lost.

MOTOROLA Semiconductors

MC2915A

QUAD THREE-STATE BUS TRANSCEIVER WITH INTERFACE LOGIC

The MC2915A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the Bus inputs) are one LS unit load. The three-state bus output can sink up to 48 mA at 0.5 V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is High, the driver is disabled. The V_{OH} and V_{OL} of the bus driver are selected for compatibility with standard and low-power Schottky inputs.

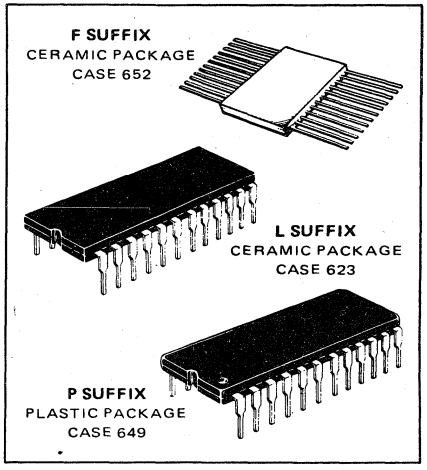
The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is Low, the A_n data is stored in the register and when S is High, the B_n data is stored. The buffered common clock (DRCP) enters the data into this driver register on the Low-to-High transition.

Data from the A or B inputs is inverted at the Bus output. Likewise, data at the Bus input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is Low, the latch is open and the receiver outputs will follow the bus inputs (Bus data inverted and OE Low). When the $\overline{RLE}$ input is High, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is High, the receiver outputs are in the high-impedance state.

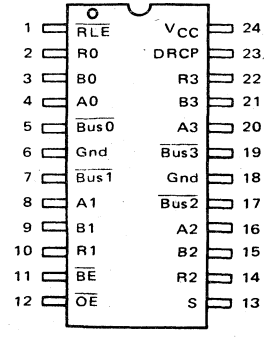
FEATURES

- Quad High-Speed LSI Bus Transceiver
- Three-state Bus Driver
- Two-port Input to D-type Register on Driver
- Bus Driver Output Can Sink 48 mA at 0.5 V Max
- Receiver Has Output Latch for Pipeline Operation
- Three-State Receiver Outputs Sink 12 mA
- Advanced Low-power Schottky Processing
- 100% Reliability Assurance Testing in Compliance With MIL-STD-883
- 3.5 V Minimum Output High Voltage for Direct Interface to MOS Microprocessors

TTL QUAD THREE-STATE BUS TRANSCEIVER WITH INTERFACE LOGIC



PIN ASSIGNMENT



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	MC2915APC
Hermetic DIP	0°C to +70°C	MC2915ALC
Hermetic DIP	-55°C to +125°C	MC2915ALM
Hermetic Flat Pack	-55°C to +125°C	MC2915AFM

DS9509

MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC}max
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, into Outputs (Except Bus)	30 mA
DC Output Current, into Bus	100 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

MC2915AXC − T_A = 0°C to +70°C, V_{CC} = 5.0 V ±5% (Commercial), Min = 4.75 V, Max = 5.25 V
MC2915AXM − T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10% (Military), Min = 4.5 V, Max = 5.5 V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameter	Description	Test Conditions (Note 1)		Min	Typ	Max	Unit
V_{OL}	Bus Output Low Voltage	V_{CC} = Min	I_{OL} = 24 mA			0.4	Volts
			I_{OL} = 48 mA			0.5	
V_{OH}	Bus Output High Voltage	V_{CC} = Min	Commercial, I_{OH} = −20 mA	2.4			Volts
			Military, I_{OH} = −15 mA	2.4			
I_O	Bus Leakage Current (High Impedance)	V_{CC} = Max, Bus Enable = 2.4 V	V_O = 0.4 V			−200	μA
			V_O = 2.4 V			50	
			V_O = 4.5 V			100	
I_{off}	Bus Leakage Current (Power off)	V_O = 4.5 V, V_{CC} = 0 V				100	μA
V_{IH}	Receiver Input High Threshold	Bus Enable = 2.4 V		2.0			Volts
V_{IL}	Receiver Input Low Threshold	Bus Enable = 2.4 V	Commercial			0.8	Volts
			Military			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = Max, V_O = 0 V		−50	−120	−225	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

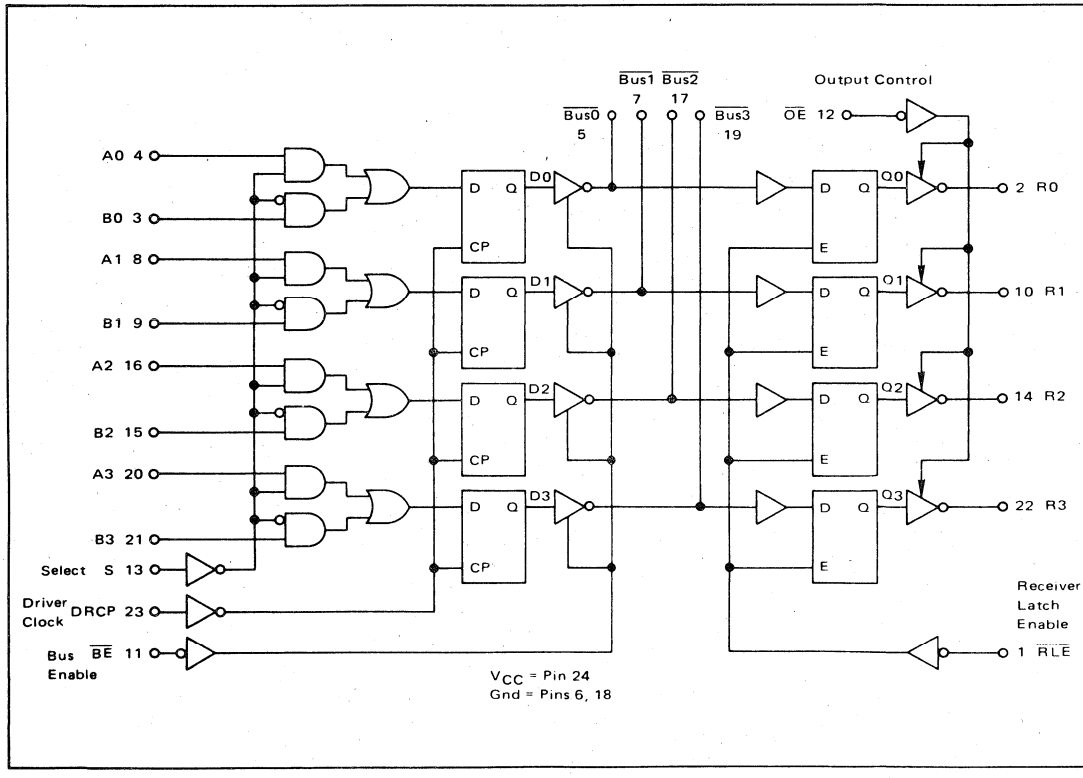
Parameter	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Unit
V_{OH}	Receiver Output High Voltage	V_{CC} = Min, V_{in} = V_{IL} or V_{IH}	Military, I_{OH} = −1.0 mA	2.4	3.4		Volts
			Commercial, I_{OH} = −2.6 mA	2.4	3.4		
		V_{CC} = 5.0 V, I_{OH} = −100 μA		3.5			
V_{OL}	Output Low Voltage (Except Bus)	V_{CC} = Min, V_{in} = V_{IL} or V_{IH}	I_{OL} = 4.0 mA		0.27	0.4	Volts
			I_{OL} = 8.0 mA		0.32	0.45	
			I_{OL} = 12 mA		0.37	0.5	
V_{IH}	Input High Level (Except Bus)	Guaranteed input logical High for all inputs		2.0			Volts
V_{IL}	Input Low Level (Except Bus)	Guaranteed input logical Low for all inputs	Military			0.7	Volts
			Commercial			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = Min, I_{in} = −18 mA				−1.2	Volts
I_{IL}	Input Low Current (Except Bus)	V_{CC} = Max, V_{in} = 0.4 V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input High Current (Except Bus)	V_{CC} = Max, V_{in} = 2.7 V				20	μA
I_I	Input High Current (Except Bus)	V_{CC} = Max, V_{in} = 7.0 V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = Max		−30		−130	mA
I_{CC}	Power Supply Current	V_{CC} = Max			63	95	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = Max	V_O = 2.4 V			50	μA
			V_O = 0.4 V			−50	

NOTES: 1. For conditions shown as Min or Max, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

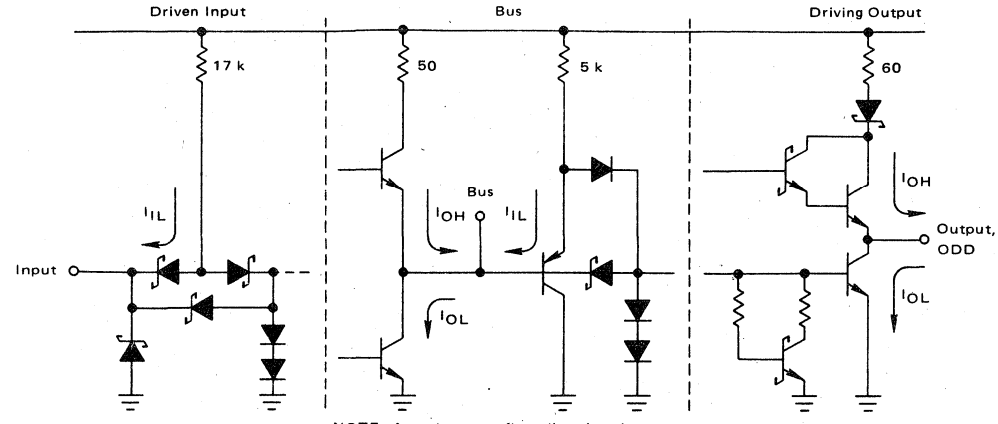
SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameter	Description	Test Conditions	MC2915AXM			MC2915AXC			Unit
			Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (Bus) = 50 pF	–	21	36	–	21	32	ns
t_{PLH}		R_L (Bus) = 130 Ω	–	21	36	–	21	32	
t_{ZH},t_{ZL}	Bus Enable ($\overline{BE}$) to Bus		–	13	26	–	13	23	ns
t_{HZ},t_{LZ}			–	13	21	–	13	18	
t_s	Data Inputs (A or B)	C_L = 15 pF	15	–	–	12	–	–	ns
t_h		R_L = 2.0 k	8.0	–	–	6.0	–	–	
t_s	Select Input (S)		28	–	–	25	–	–	ns
t_h			8.0	–	–	6.0	–	–	
t_{PW}	Driver Clock (DRCP) Pulse Width (High)		20	–	–	17	–	–	ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)		–	18	33	–	18	30	ns
t_{PHL}			–	18	30	–	18	27	
t_{PLH}	Latch Enable to Receiver Output		–	21	33	–	21	30	ns
t_{PHL}			–	21	30	–	21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		15	–	–	13	–	–	ns
t_h			6.0	–	–	4.0	–	–	
t_{ZH},t_{ZL}	Output Control to Receiver Output		–	14	26	–	14	23	ns
t_{HZ},t_{LZ}		C_L = 5 pF, R_L = 2.0 k	–	14	26	–	14	23	

LOGIC DIAGRAM



INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



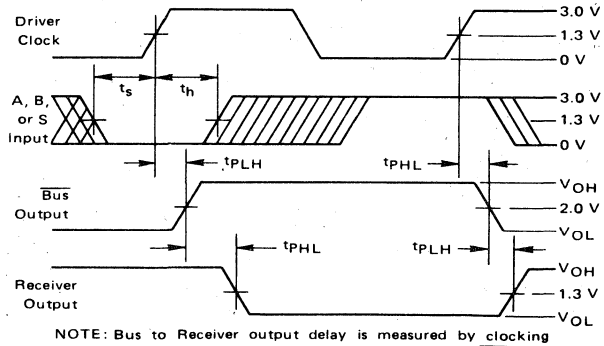
NOTE: Actual current flow direction shown.

FUNCTION TABLE

Inputs							Internal to Device		Bus	Output	
S	A_n	B_n	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_n	Q_n	$\overline{Bus_n}$	R_n	Function
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable
X	X	X	X	H	L	L	X	H	H	L	and receive data via Bus input
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

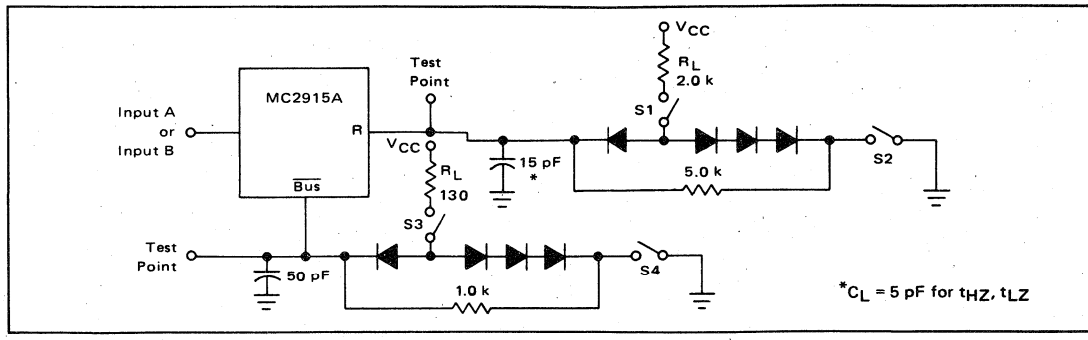
H = High Z = High impedance X = Don't care
L = Low NC = No change ↑ = Low-to-high transition

SWITCHING WAVEFORMS



NOTE: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{Bus}$ to R combinatorial delay.

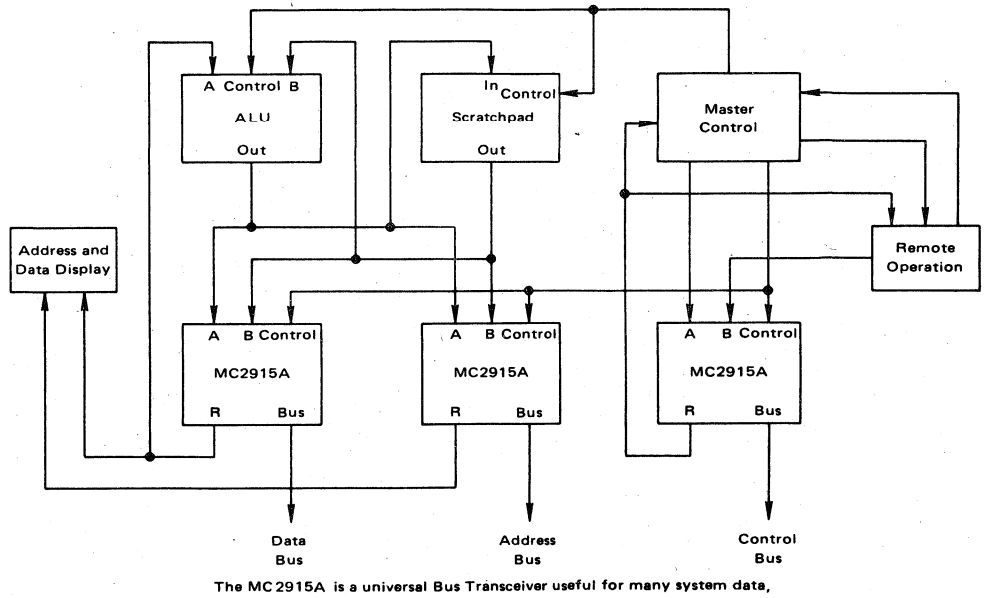
SWITCHING TEST CIRCUIT



DEFINITIONS OF FUNCTIONAL TERMS

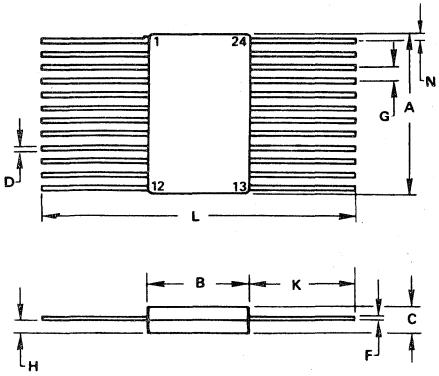
A0, A1, A2, A3	The "A" word data input into the two input multiplexers of the driver register.
B0, B1, B2, B3	The "B" word data input into the two input multiplexers of the driver register.
S	Select. When the select input is Low, the A data word is applied to the driver register. When the select input is High, the B word is applied to the driver register.
DRCP	Driver Clock Pulse. Clock pulse for the driver register.
$\overline{BE}$	$\overline{\text{Bus Enable}}$. When the Bus Enable is High, the four drivers are in the high impedance state.
$\overline{Bus0}$, $\overline{Bus1}$, $\overline{Bus2}$, $\overline{Bus3}$	The four driver outputs and receiver inputs (data is inverted).
R0, R1 R2, R3	The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.
$\overline{RLE}$	$\overline{\text{Receiver Latch Enable}}$. When $\overline{RLE}$ is Low, data on the Bus inputs is passed through the receiver latches. When $\overline{RLE}$ is High, the receiver latches are closed and will retain the data independent of all other inputs.
$\overline{OE}$	$\overline{\text{Output Enable}}$. When the $\overline{OE}$ input is High, the four three-state receiver outputs are in the high impedance state.

APPLICATIONS



The MC2915A is a universal Bus Transceiver useful for many system data, address, control, and timing input/output interfaces.

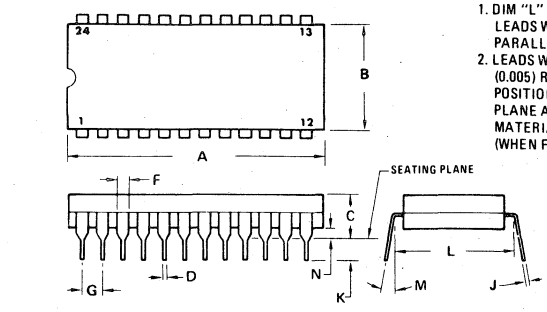
PACKAGE DIMENSIONS



NOTES:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

CASE 652

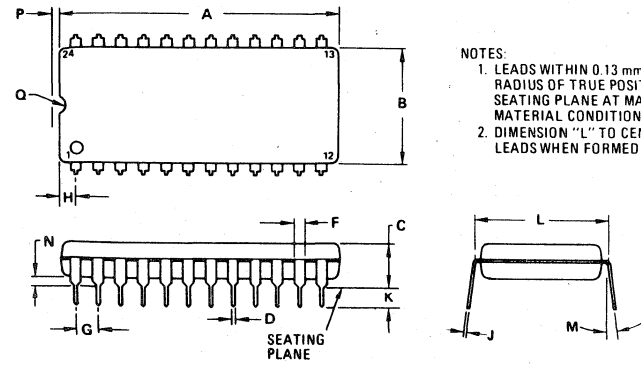
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.99	15.49	0.590	0.610
B	9.27	9.91	0.365	0.390
C	1.27	2.03	0.050	0.080
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.69	1.02	0.027	0.040
K	6.35	9.40	0.250	0.370
L	21.97	–	0.865	–
N	0.25	0.63	0.010	0.025



NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL)

CASE 623

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.29	4.06	0.090	0.160
L	15.24 BSC		0.600 BSC	
M	0^0	15^0	0^0	15^0
N	0.51	1.27	0.020	0.050



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

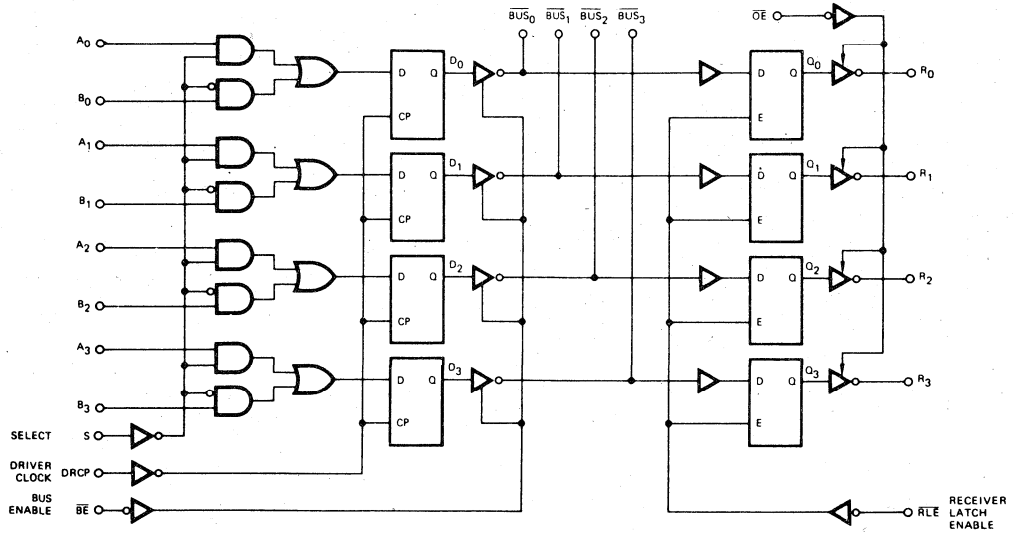
CASE 649

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

PRODUCT PREVIEW

MC2905 and MC2915 LSI Bus Transceivers

The MC2905 is a four-bit bus transceiver designed to drive a 100mA load on an open collector bus. The MC2915 is an identical circuit, designed to drive a three-state bus. They include a two-port input register and a latch on the receiver outputs. The latch is three-state. Delay from clock to bus is typically 21ns; from bus to receiver output is typically 18 ns.

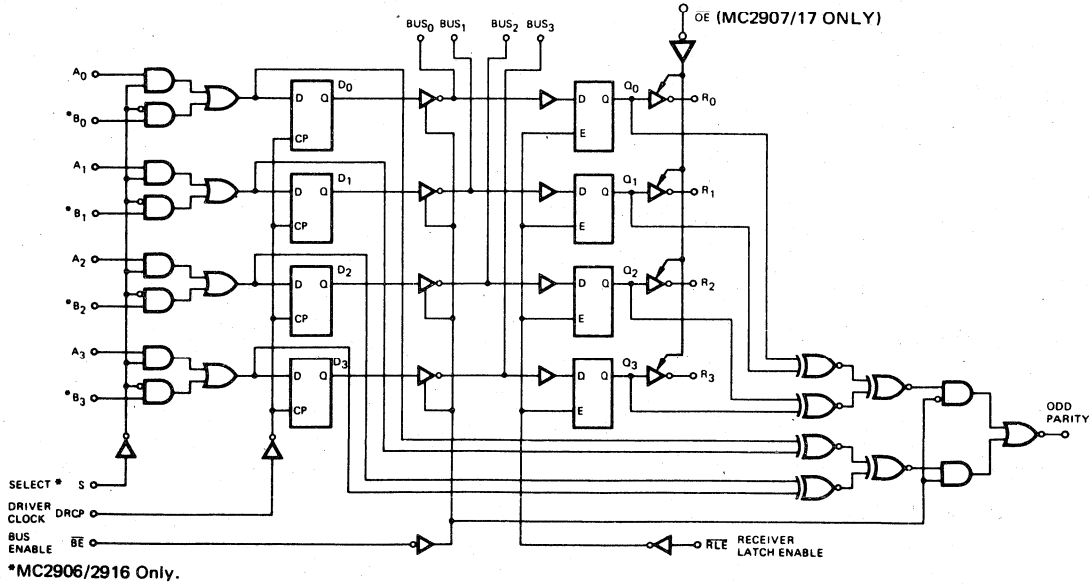


MC2906 and MC2916 LSI Bus Transceivers

Like the MC2905 and MC2915, but includes a parity generator/checker on chip.

MC2907 and MC2917 LSI Bus Transceivers

Like the MC2906 and MC2916, but has only one data input port on the driver register. Fits in space-saving, 20-pin package.



*MC2906/2916 Only.

MC2917A

QUAD THREE-STATE BUS TRANSCEIVER WITH INTERFACE LOGIC

The MC2917A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the Bus inputs) are one LS unit load. The three-state bus output can sink up to 48 mA at 0.5 V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is High, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_n data into this driver register on the Low-to-High transition.

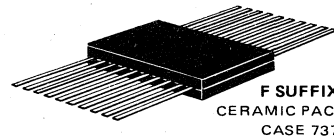
Data from the A input is inverted at the Bus output. Likewise, the data at the Bus input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is Low, the latch is open and the receiver outputs will follow the bus inputs (Bus data inverted and $\overline{OE}$ Low). When the $\overline{RLE}$ input is High, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is High, the receiver outputs are in the high-impedance state.

The MC2917A features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is Low (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is High, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated; and, if the driver is in the high-impedance state, the Bus parity is checked.

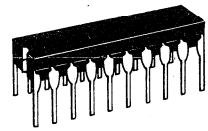
FEATURES

- Quad High-speed LSI Bus Transceiver
- Three-state Bus Driver
- D-type Register on Driver
- Bus Driver Output Can Sink 48 MA at 0.5 V Max
- Internal Odd 4-bit Parity Checker/Generator
- Receiver Has Output Latch for Pipeline Operation
- Three-state Receiver Outputs Sink 12 mA
- Advanced Low-power Schottky Processing
- 100% Reliability Assurance Testing in Compliance With MIL-STD-883
- 3.5 V Minimum Output High Voltage for Direct Interface to MOS Microprocessors

TTL
QUAD THREE-STATE
BUS TRANSCEIVER
WITH INTERFACE LOGIC

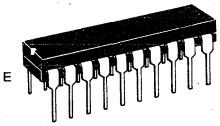


F SUFFIX
CERAMIC PACKAGE
CASE 737

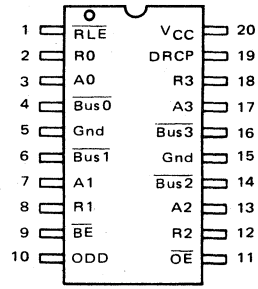


L SUFFIX
CERAMIC PACKAGE
CASE 732

P SUFFIX
PLASTIC PACKAGE
CASE 738



PIN ASSIGNMENT



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	MC2917APC
Hermetic DIP	0°C to +70°C	MC2917ALC
Hermetic DIP	−55°C to +125°C	MC2917ALM
Hermetic Flat Pack	−55°C to +125°C	MC2917AFM

MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, into Outputs (Except Bus)	30 mA
DC Output Current, into Bus	100 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

MC2917AXC — T_A = 0°C to +70°C, V_{CC} = 5.0 V ±5% (Commercial), Min = 4.75 V, Max = 5.25 V
MC2917AXM — T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10% (Military), Min = 4.5 V, Max = 5.5 V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameter	Description	Test Conditions (Note 1)			Min	Typ	Max	Unit
V_{OL}	Bus Output Low Voltage	V_{CC} = Min	I_{OL} = 24 mA				0.4	Volts
			I_{OL} = 48 mA				0.5	
V_{OH}	Bus Output High Voltage	V_{CC} = Min	Commercial, I_{OH} = −20 mA		2.4			Volts
			Military, I_{OH} = −15 mA		2.4			
I_O	Bus Leakage Current (High Impedance)	V_{CC} = Max, Bus Enable = 2.4 V	V_O = 0.4 V				−200	μA
			V_O = 2.4 V				50	
			V_O = 4.5 V				100	
I_{off}	Bus Leakage Current (Power off)	V_O = 4.5 V, V_{CC} = 0 V					100	μA
V_{IH}	Receiver Input High Threshold	Bus Enable = 2.4 V			2.0			Volts
V_{IL}	Receiver Input Low Threshold	Bus Enable = 2.4 V		Commercial			0.8	Volts
				Military			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = Max, V_O = 0 V			−50	−120	−225	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

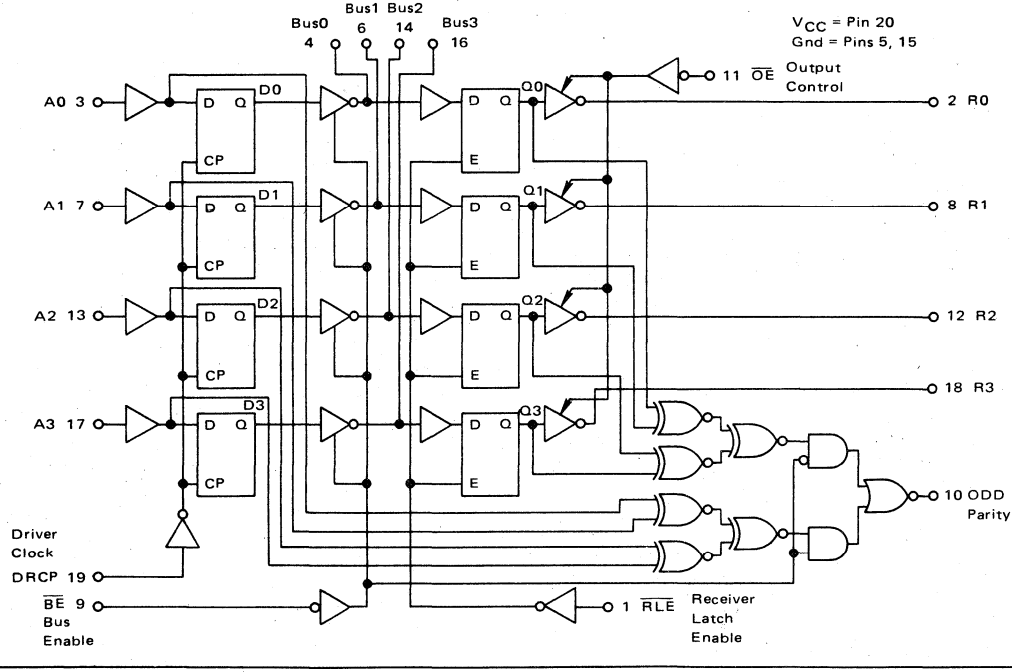
Parameter	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Unit
V_{OH}	Receiver Output High Voltage	V_{CC} = Min, V_{in} = V_{IL} or V_{IH}	Military, I_{OH} = −1.0 mA		2.4	3.4		Volts
			Commercial, I_{OH} = −2.6 mA		2.4	3.4		
		V_{CC} = 5.0 V, I_{OH} = −100 μA			3.5			
V_{OH}	Parity Output High Voltage	V_{CC} = Min, I_{OH} = −660 μA, V_{in} = V_{IH} or V_{IL}		Military	2.5	3.4		Volts
				Commercial	2.7	3.4		
V_{OL}	Output Low Voltage (Except Bus)	V_{CC} = Min, V_{in} = V_{IL} or V_{IH}	I_{OL} = 4.0 mA			0.27	0.4	Volts
			I_{OL} = 8.0 mA			0.32	0.45	
			I_{OL} = 12 mA			0.37	0.5	
V_{IH}	Input High Level (Except Bus)	Guaranteed input logical High for all inputs			2.0			Volts
V_{IL}	Input Low Level (Except Bus)	Guaranteed input logical Low for all inputs		Military			0.7	Volts
				Commercial			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = Min, I_{in} = −18 mA					−1.2	Volts
I_{IL}	Input Low Current (Except Bus)	V_{CC} = Max, V_{in} = 0.4 V	$\overline{BE}$, $\overline{RLE}$				−0.72	mA
			All other inputs				−0.36	
I_{IH}	Input High Current (Except Bus)	V_{CC} = Max, V_{in} = 2.7 V					20	μA
I_I	Input High Current (Except Bus)	V_{CC} = Max, V_{in} = 7.0 V					100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = Max		Receiver	−30		−130	mA
				Parity	−20		−100	
I_{CC}	Power Supply Current	V_{CC} = Max				63	95	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = Max	V_O = 2.4 V				50	μA
			V_O = 0.4 V				−50	

NOTES: 1. For conditions shown as Min or Max, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

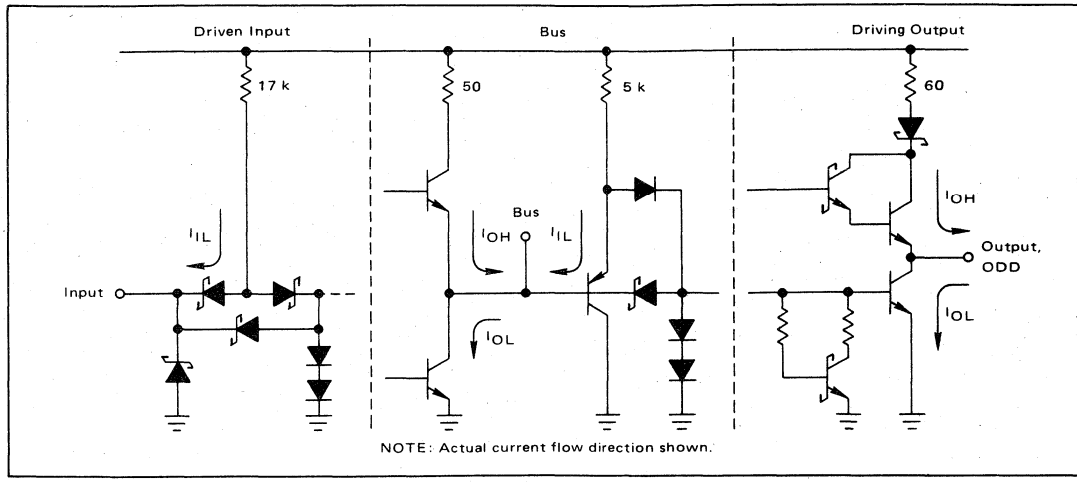
SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameter	Description	Test Conditions	MC2917AXM			MC2917AXC			Unit
			Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (Bus) = 50 pF	–	21	36	–	21	32	ns
t_{PLH}		R_L (Bus) = 130 Ω	–	21	36	–	21	32	
t_{ZH},t_{ZL}	Bus Enable ($\overline{BE}$) to Bus		–	13	26	–	13	23	ns
t_{HZ},t_{LZ}			–	13	21	–	13	18	
t_s	A Data Input	C_L = 15 pF	15	–	–	12	–	–	ns
t_h		R_L = 2.0 k	8.0	–	–	6.0	–	–	
t_{PW}	Clock Pulse Width (High)		20	–	–	17	–	–	ns
t_{PLH}	Bus to Receiver Output		–	18	33	–	18	30	ns
t_{PHL}	(Latch Enabled)		–	18	30	–	18	27	
t_{PLH}	Latch Enable to Receiver Output		–	21	33	–	21	30	ns
t_{PHL}			–	21	30	–	21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		15	–	–	13	–	–	ns
t_h			6.0	–	–	4.0	–	–	
t_{PLH}	A Data to Odd Parity Out		–	32	46	–	32	42	ns
t_{PHL}	(Driver Enabled)		–	26	40	–	26	36	
t_{PLH}	Bus to Odd Parity Out		–	21	36	–	21	32	ns
t_{PHL}	(Driver Inhibit)		–	21	36	–	21	32	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd		–	21	36	–	21	32	ns
t_{PHL}	Parity Output		–	21	36	–	21	32	
t_{ZH},t_{ZL}	Output Control to Output		–	14	26	–	14	23	ns
t_{HZ},t_{LZ}		C_L = 5 pF, R_L = 2.0 k	–	14	26	–	14	23	

LOGIC DIAGRAM



INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



NOTE: Actual current flow direction shown.

FUNCTION TABLE

		Inputs			Internal to Device		Bus	Output	
A_n	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_n	Q_n	Bus_n	R_n	Function
X	X	H	X	X	X	X	H	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = High Z = High impedance X = Don't care
L = Low NC = No change ↑ = Low-to-high transition

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	Odd Parity Output
L	ODD = A0 ⊕ A1 ⊕ A2 ⊕ A3
H	ODD = Q0 ⊕ Q1 ⊕ Q2 ⊕ Q3

DEFINITIONS OF FUNCTIONAL TERMS

DRCP — Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ — Bus Enable. When the Bus Enable is Low, the four drivers are in the high impedance state.

Bus0, Bus1, Bus2, Bus3 — The four driver outputs and receiver inputs (data is inverted).

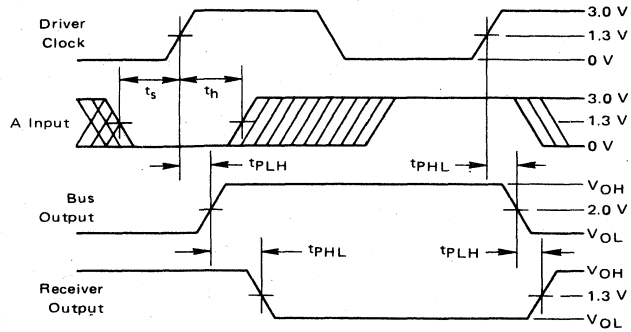
R0, R1, R2, R3 — The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ — Receiver Latch Enable. When $\overline{RLE}$ is Low, data on the Bus inputs is passed through the receiver latches. When $\overline{RLE}$ is High, the receiver latches are closed and will retain the data independent of all other inputs.

ODD — Odd parity output generates parity with the driver enabled. Checks parity with the driver in the high impedance state.

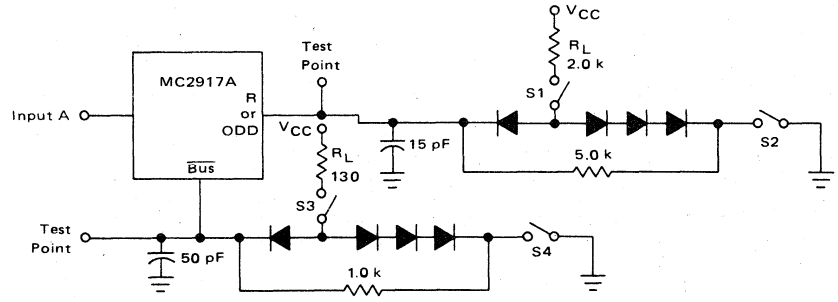
$\overline{OE}$ — Output Enable. When the $\overline{OE}$ input is High, the four three-state receiver outputs are in the high impedance state.

SWITCHING WAVEFORMS

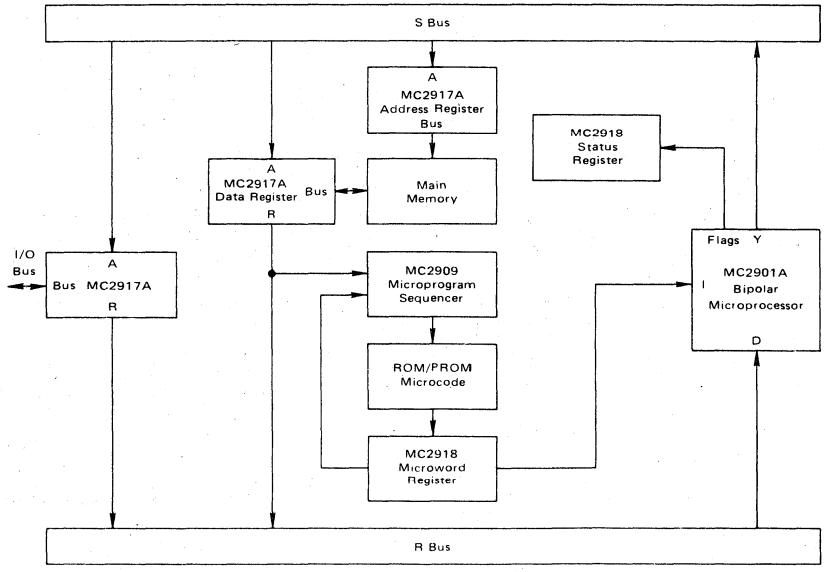


NOTE: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the Bus to R combinatorial delay.

SWITCHING TEST CIRCUIT

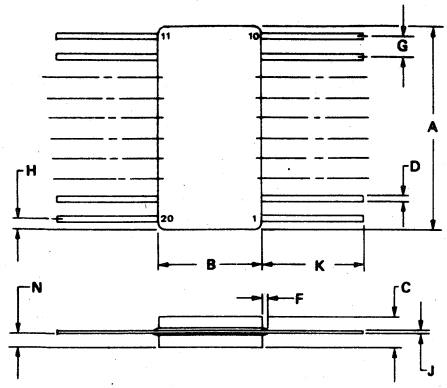


APPLICATIONS



The MC2917A can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high speed microprocessor systems.

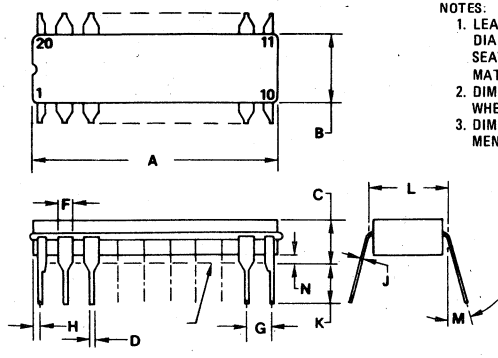
PACKAGE DIMENSIONS



NOTE:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

CASE 737

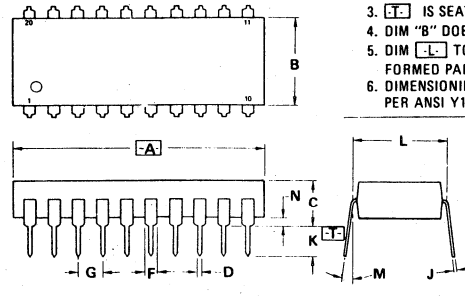
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	13.08	–	0.515
B	5.84	6.60	0.230	0.260
C	1.52	2.16	0.060	0.085
D	0.41	0.46	0.016	0.018
F	–	0.25	–	0.010
G	1.27 BSC		0.050 BSC	
H	1.14	1.40	0.045	0.055
J	0.08	0.13	0.003	0.005
K	–	9.14	–	0.360
N	–	1.02	–	0.040



NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

CASE 732

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	24.38	25.15	0.960	0.990
B	6.86	7.49	0.270	0.295
C	4.32	5.08	0.170	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	5°	15°	5°	15°
N	0.51	0.76	0.020	0.030



NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS;
   ⌖ Ø 0.25 (0.010) Ⓜ T A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM "B" DOES NOT INCLUDE MOLD FLASH.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

CASE 738

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.65	27.18	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.94	4.19	0.155	0.165
D	0.38	0.56	0.015	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	2.79	3.56	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

MC2918

QUAD D REGISTER WITH STANDARD AND THREE-STATE OUTPUTS

New Schottky circuits such as the MC2918 register provide the design engineer with additional flexibility in system configuration—especially with regard to bus structure, organization, and speed. The MC2918 is a quadruple D-type register with four standard totem pole outputs and four three-state bus-type outputs. The 16-pin device also features a buffered common clock (CP) and a buffered common output control ($\overline{OE}$) for the Y outputs. Information meeting the setup and hold requirements on the D inputs is transferred to the Q outputs on the Low-to-High transition of the clock.

The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is Low. When the $\overline{OE}$ input is High, the Y outputs are in the high-impedance state.

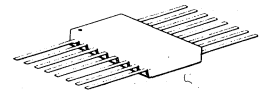
The MC2918 register can be used in bipolar microprocessor designs as an address register, status register, instruction register or for various data or microword register applications. Because of the unique design of the three-state output, the device features very short propagation delay from the clock to the Q or Y outputs. Thus, system performance and architectural design can be improved by using the MC2918 register. Other applications of MC2918 register can be found in microprogrammed display systems, communication systems and most general or special purpose digital signal processing equipment.

FEATURES

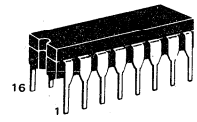
- Advanced Schottky Technology
- Four D-type Flip-flops
- Four Standard Totem Pole Outputs
- Four Three-state Outputs
- 75 MHz Clock Frequency
- 100% Reliability Assurance Testing in Compliance With MIL-STD-883

TTL

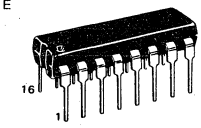
QUAD D REGISTER WITH STANDARD AND THREE-STATE OUTPUTS



F SUFFIX
CERAMIC PACKAGE
CASE 650

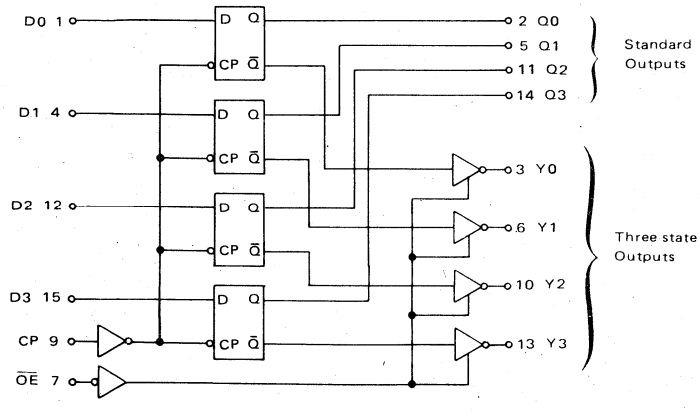


L SUFFIX
CERAMIC PACKAGE
CASE 620

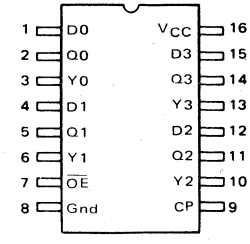


P SUFFIX
PLASTIC PACKAGE
CASE 648

LOGIC DIAGRAM



PIN ASSIGNMENT



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	MC2918PC
Hermetic DIP	0°C to +70°C	MC2918LC
Hermetic DIP	−55°C to +125°C	MC2918LM
Hermetic Flat Pack	−55°C to +125°C	MC2918FM

DS9512

MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} Max
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

MC2918XC – T_A = 0°C to +70°C, V_{CC} = 5.0 V ±5% (Commercial), Min = 4.75 V, Max = 5.25 V
MC2918XM – T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10% (Military), Min = 4.5 V, Max = 5.5 V

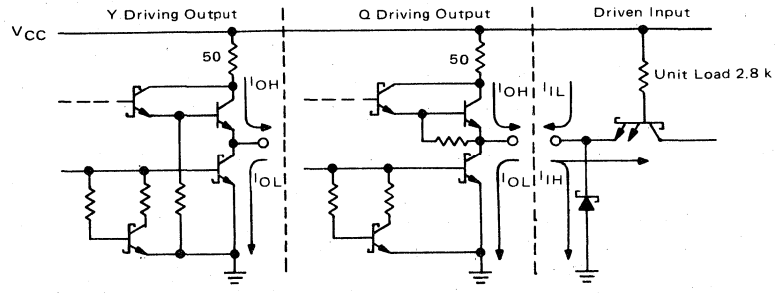
Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output High Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	Q	I_{OH} = −1 mA, Military	2.5	3.4	–	Volts
				I_{OH} = −1 mA, Commercial	2.7	3.4	–	
			Y	Military, I_{OH} = −2 mA	2.4	3.4	–	
				Commercial, I_{OH} = −6.5 mA	2.4	3.4	–	
V_{OL}	Output Low Voltage (Note 6)	V_{CC} = Min, I_{OL} = 20 mA, V_{IN} = V_{IH} or V_{IL}			–	–	0.5	Volts
V_{IH}	Input High Level	Guaranteed input logical High voltage for all inputs			2.0	–	–	Volts
V_{IL}	Input Low Level	Guaranteed input logical Low voltage for all inputs			–	–	0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min, I_{in} = −18 mA			–	–	−1.2	Volts
I_{IL} (Note 3)	Input Low Current	V_{CC} = Max, V_{in} = 0.5 V			–	–	−2.0	mA
I_{IH} (Note 3)	Input High Current	V_{CC} = Max, V_{in} = 2.7 V			–	–	50	μA
I_I	Input High Current	V_{CC} = Max, V_{in} = 5.5 V			–	–	1.0	mA
I_O	Y Output Off-State Leakage Current	V_{CC} = Max		V_O = 2.4 V	–	–	50	μA
				V_O = 0.4 V	–	–	−50	
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = Max			−40	–	−100	mA
I_{CC}	PowerSupply Current	V_{CC} = Max (Note 5)			–	80	130	mA

NOTES: 1. For conditions shown as Min or Max, use the appropriate value specified under Electrical Characterisitcs for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (see Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured with all inputs at 4.5 V and all outputs open.
6. Measured on Y outputs with Q outputs open. Measured on Q outputs with Y outputs open.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0 V, R_L = 280 Ω)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Q Output		C_L = 15 pF	–	6.0	9.0	ns
t_{PHL}				–	8.5	13	
t_{PW}	Clock Pulse Width	High		7.0	–	–	ns
		Low		9.0			
t_s	Data			5.0	–	–	ns
t_h	Data			3.0	–	–	ns
t_{PLH}	Clock to Y Output ($\overline{OE}$ Low)			–	6.0	9.0	ns
t_{PHL}				–	8.5	13	
t_{ZH}	Output Control to Output		C_L = 15 pF	–	12.5	19	ns
t_{ZL}				–	12	18	
t_{HZ}			C_L = 5.0 pF	–	4.0	6.0	
t_{LZ}				–	7.0	10.5	
f_{max}	Maximum Clock Frequency		C_L = 15 pF	75	100	–	MHz

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



NOTE: Actual current flow direction shown.

TRUTH TABLE

Inputs			Outputs		
$\overline{OE}$	Clock CP	D	Q	Y	Notes
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

L = Low
H = High
X = Don't care

NC = No change
↑ = Low to high transition
Z = High impedance

NOTE 1. When $\overline{OE}$ is Low, the Y output will be in the same logic state as the Q output.

DEFINITIONS OF FUNCTIONAL TERMS

D_n The four data inputs to the register.

Q_n The four data outputs of the register with standard totem pole active pull-up outputs. Data is passed non-inverted.

Y_n The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A High on the "output control" input forces the Y_n outputs to the high-impedance state.

CP Clock The buffered common clock for the register. Enters data on the Low-to-High Transition.

$\overline{OE}$ Output Control. When the $\overline{OE}$ input is High, the Y_n outputs are in th high-impedance state. When the $\overline{OE}$ input is Low, the TRUE register data is present at the Y_n outputs.

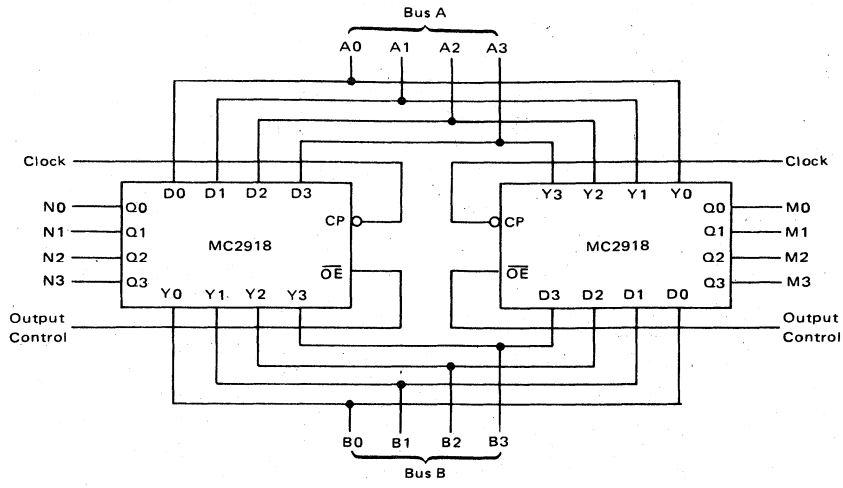
LOADING RULES
(In Unit Loads)

Input/ Output	Pin Numbers	Input Unit Load	Fan-out	
			Output High	Output Low
D0	1	1	–	–
Q0	2	–	20	10*
Y0	3	–	40/130	10*
D1	4	1	–	–
Q1	5	–	20	10*
Y1	6	–	40/130	10*
$\overline{OE}$	7	1	–	–
Gnd	8	–	–	–
CP	9	1	–	–
Y2	10		40/130	10*
Q2	11	–	20	10*
D2	12	1	–	–
Y3	13	–	40/130	10*
Q3	14	–	20	10*
D3	15	1	–	–
V_{CC}	16	–	–	–

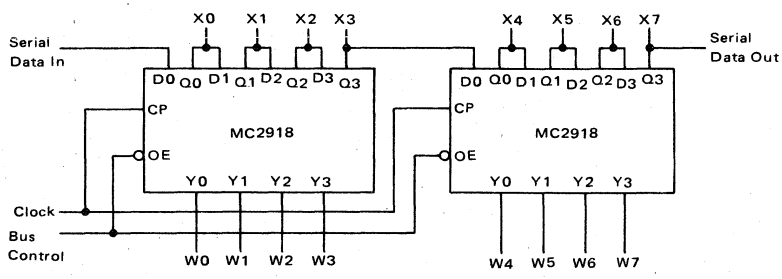
A Schottky TTL unit load is defined as 50 μA measured at 2.7 V High and −2.0 mA measured at 0.5 V Low.

*Fan-out on each Q_n and Y_n output pair should not exceed 15 unit loads (30 mA).

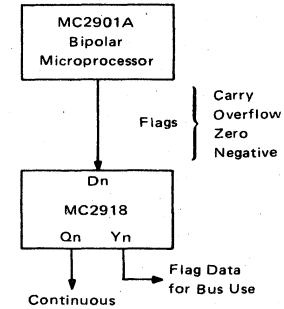
APPLICATIONS



The MC2918 can be connected for bidirectional interface between two buses. The device on the left stores data from the A bus and drives the A bus. The device on the right stores data from the B bus and drives the A bus. The output control is used to place either or both drivers in the high-impedance state. The contents of each register are available for continuous usage at the N and M ports of the device.

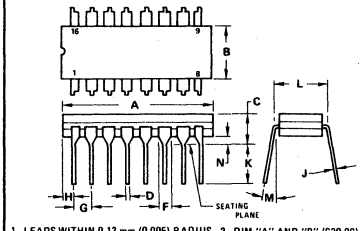


8-bit serial-to-parallel converter with three-state output (W) and direct access to the register word (X).



The MC2918 as a 4-bit status register.

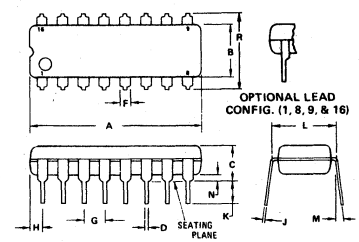
PACKAGE DIMENSIONS



1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "A" AND "B" (620-06) DO NOT INCLUDE GLASS RUN-OUT.
4. DIM "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW BODY).

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	5.08	0.125	0.200
L	7.49	8.89	0.295	0.350
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

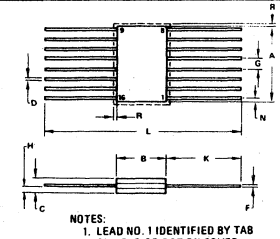
CASE 620



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	22.10	–	0.870
B	6.10	6.60	0.240	0.260
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	–	1.78	–	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.28	0.38	0.008	0.015
K	2.92	–	0.115	–
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	–	0.020	–
R	–	8.26	–	0.325

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. DIMENSION "R" TO BE MEASURED AT THE TOP OF THE LEADS (NOT AT THE TIPS).

CASE 648



NOTES:
1. LEAD NO. 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
2. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.22	7.24	0.245	0.285
C	1.52	2.03	0.060	0.080
D	0.41	0.48	0.016	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.64	0.89	0.025	0.035
K	6.35	9.40	0.250	0.370
L	18.92	–	0.745	–
R	–	0.51	–	0.020
R	–	0.38	–	0.015

CASE 650

MEMORIES

The following Random Access Memories and Programmable Read Only Memories are designed for use with LSTTL logic devices and the M2900 microprocessor family.

The PROMs are manufactured with nichrome links which can be "blown" to break metallization patterns and implement a specific program. Extra test rows and columns are included in addition to the storage array; fuses in these test rows are blown prior to shipment to assure high programmability and guarantee performance.

RAMs

MEMORY SIZE	ORGANIZATION	PART NUMBER	ACCESS TIME ns MAX	OUTPUT	NO. OF PINS
1024	1024 x 1	MCM93415	45	Open Collector	16
1024	1024 x 1	MCM93425	45	Three-State	16
1024	256 x 4	MCM93422*	45	Three-State	22

PROMs

MEMORY SIZE	ORGANIZATION	PART NUMBER	ACCESS TIME ns MAX	OUTPUT	NO. OF PINS
8192	2048 x 4	MCM7684*	80	Open Collector	18
8192	2048 x 4	MCM7685*	80	Three-State	18
8192	2048 x 4	MCM7686*	TBD	Output Register	20
8192	2048 x 4	MCM7687*	TBD	Output Latch	20
8192	1024 x 8	MCM7680	70	Open Collector	24
8192	1024 x 8	MCM7681	70	Three-State	24
8192	1024 x 8	MCM82707*	70	Open Collector	24
8192	1024 x 8	MCM82708*	70	Three State	24
4096	1024 x 4	MCM7642	70	Open Collector	18
4096	1024 x 4	MCM7643	70	Three-State	18
4096	512 x 8	MCM7640	70	Open Collector	24
4096	512 x 8	MCM7641	70	Three-State	24
2048	512 x 4	MCM7620	50	Open Collector	16
2048	512 x 4	MCM7621	50	Three-State	16
256	64 x 8	MCM5003/5303	125	Open Collector	24
256	64 x 8	MCM5004/5304	125	2k Pullup	24

*To be introduced.

See Chapter 7 for Packaging.

MOTOROLA Semiconductors

MCM93415

1024-BIT RANDOM ACCESS MEMORY

The MCM93415 is a 1024-bit Read/Write RAM organized 1024 words by 1 bit.

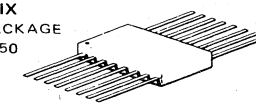
The MCM93415 is designed for buffer control storage and high performance main memory applications, and has a typical access time of 35 ns.

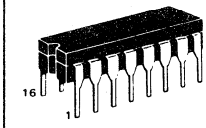
The MCM93415 has full decoding on-chip, separate data input and data output lines, and an active low chip select. The device is fully compatible with standard DTL and TTL logic families and features an uncommitted collector output for ease of memory expansion.

- Uncommitted Collector Output
- TTL Inputs and Output
- Non-Inverting Data Output
- High Speed –
  - Access Time – 35 ns Typical
  - Chip Select – 15 ns Typical
- Power Dissipation Decreases with Increasing Temperature
- Power Dissipation 0.5 mW/Bit Typical
- Organized 1024 Words X 1 Bit

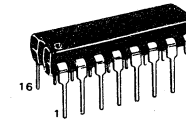
TTL
1024 X 1 BIT
RANDOM ACCESS MEMORY

F SUFFIX
CERAMIC PACKAGE
CASE 650



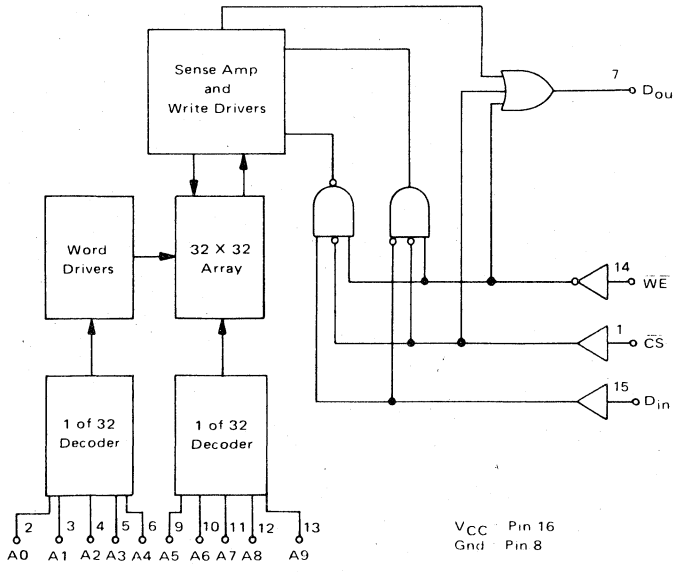


D SUFFIX
CERAMIC PACKAGE
CASE 620

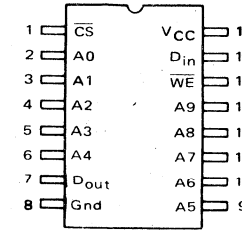


P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM



PIN ASSIGNMENT



Pin Designation

$\overline{CS}$	Chip Select
A0 – A9	Address Inputs
$\overline{WE}$	Write Enable
D_{in}	Data Input
D_{out}	Data Output

DS 9447
(formerly NP-73)

FUNCTIONAL DESCRIPTION

The MCM93415 is a fully decoded 1024-bit Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The Chip Select input provides for memory array expansion. For large memories, the fast chip select access time permits the decoding of Chip Select ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$, Pin 14). With $\overline{WE}$ held low and the chip selected, the data at D_{in} is written into the addressed location. To read, $\overline{WE}$ is held high and the chip selected. Data in the specified location is presented at D_{out} and is non-inverted.

Uncommitted collector outputs are provided to allow wired-OR applications. In any application an external pull-up resistor of R_L value must be used to provide a high at the output when it is off. Any R_L value within the range specified below may be used.

$$\frac{V_{CC}(Min)}{I_{OL} - FO(1.6)} \leq R_L \leq \frac{V_{CC}(Min) - V_{OH}}{n(I_{CEX}) + FO(0.04)}$$

R_L is in kΩ
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output High Level at Output Node
I_{OL} = Output Low Current

The minimum R_L value is limited by output current sinking ability. The maximum R_L value is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}. One Unit Load = 40 μA High/1.6 mA Low.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	
Ceramic Package (D and F Suffix)	-55°C to +165°C
Plastic Package (P Suffix)	-55°C to +125°C
Operating Junction Temperature, T_J	
Ceramic Package (D and F Suffix)	< 165°C
Plastic Package (P Suffix)	< 125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
Input Voltage (dc)	-0.5 V to +5.5 V
Voltage Applied to Outputs (Output High)	-0.5 V to +5.5 V
Output Current (dc) (Output Low)	+20 mA
Input Current (dc)	-12 mA to +5.0 mA

TRUTH TABLE

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D_{in}	Open Collector	Mode
H	X	X	H	Not Selected
L	L	L	H	Write "0"
L	L	H	H	Write "1"
L	H	X	D_{out}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't Care (High or Low)

NOTE 1: Device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

GUARANTEED OPERATING RANGES (Note 2)

Part Number	Supply Voltage (V_{CC})			Ambient Temperature (T_A)
	Min	Nom	Max	
MCM93415DC, PC	4.75 V	5.0 V	5.25 V	0°C to +75°C
MCM93415FM, DM	4.50 V	5.0 V	5.50 V	-55°C to +125°C

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

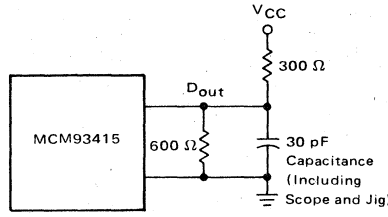
Symbol	Characteristic	Limits		Unit	Conditions
		Min	Max		
V_{OL}	Output Low Voltage		0.45	Vdc	V_{CC} = Min, I_{OL} = 16 mA
V_{IH}	Input High Voltage	2.1		Vdc	Guaranteed Input High Voltage for All Inputs
V_{IL}	Input Low Voltage		0.8	Vdc	Guaranteed Input Low Voltage for All Inputs
I_{IL}	Input Low Current		-400	μAdc	V_{CC} = Max, V_{in} = 0.4 V
I_{IH}	Input High Current		40	μAdc	V_{CC} = Max, V_{in} = 4.5 V
			1.0	mAdc	V_{CC} = Max, V_{in} = 5.25 V
I_{CEX}	Output Leakage Current		100	μAdc	V_{CC} = Max, V_{out} = 4.5 V
V_{CD}	Input Diode Clamp Voltage		-1.5	Vdc	V_{CC} = Max, I_{in} = -10 mA
I_{CC}	Power Supply Current		130	mAdc	T_A = Max; V_{CC} = Max, All Inputs Grounded
			155	mAdc	T_A = 0°C; V_{CC} = Max, All Inputs Grounded
			170	mAdc	T_A = Min; V_{CC} = Max, All Inputs Grounded

AC OPERATING CONDITIONS AND CHARACTERISTICS

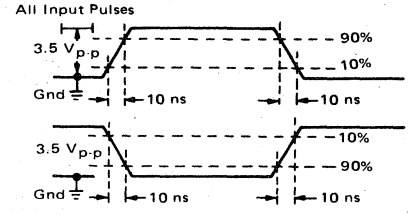
(Full operating voltage and temperature unless otherwise noted)

AC TEST LOAD AND WAVEFORM

Loading Condition



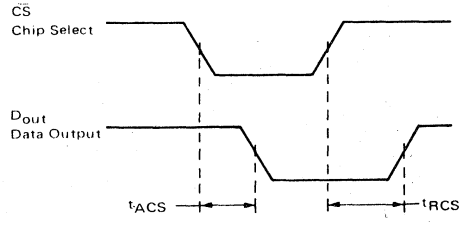
Input Pulses



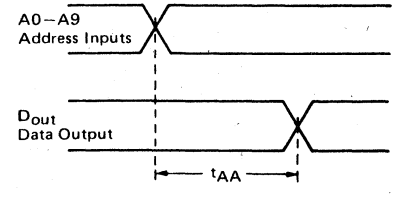
Symbol	Characteristic (Notes 2, 3)	MCM93415DC, PC Min	MCM93415DC, PC Max	MCM93415DM, FM Min	MCM93415DM, FM Max	Unit	Conditions
READ MODE	DELAY TIMES					ns	
t_{ACS}	Chip Select Time		35		45		See Test Circuit
t_{RCS}	Chip Select Recovery Time		35		50		and Waveforms
t_{AA}	Address Access Time		45		60		
WRITE MODE	DELAY TIMES					ns	
t_{WS}	Write Disable Time		35		45		See Test Circuit
t_{WR}	Write Recovery Time		40		50		and Waveforms
	INPUT TIMING REQUIREMENTS					ns	
t_W	Write Pulse Width (to guarantee write)	30		40			See Test Circuit
t_{WSD}	Data Setup Time Prior to Write	5		5			and Waveforms
t_{WHD}	Data Hold Time After Write	5		5			
t_{WSA}	Address Setup Time (at t_W - Min)	10		15			
t_{WHA}	Address Hold Time	10		10			
t_{WSCS}	Chip Select Setup Time	5		5			
t_{WHCS}	Chip Select Hold Time	5		5			

READ OPERATION TIMING DIAGRAM

Propagation Delay from Chip Select

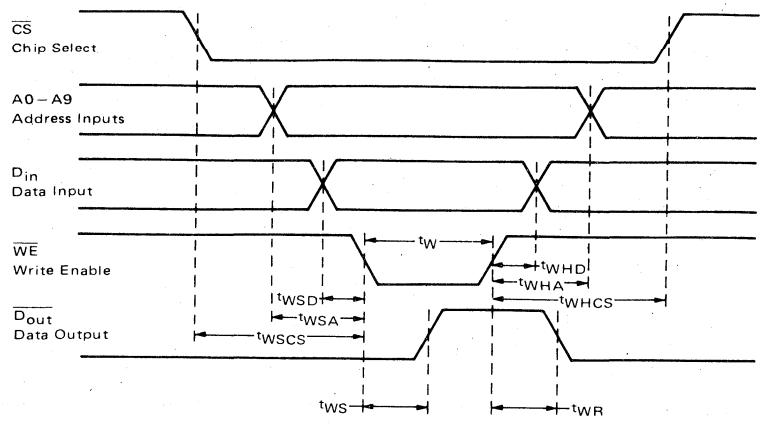


Propagation Delay from Address Inputs



(All Time Measurements Referenced to 1.5 V)

WRITE CYCLE TIMING



(All Time Measurements Referenced to 1.5 V)

NOTE 2: DC and AC specifications limits guaranteed with 500 linear feet per minute blown air. Contact your Motorola Sales Representative if extended temperature or modified operating conditions are desired.

Package	θ_{JA} (Junction to Ambient)		θ_{JC} (Junction to Case)
	Blown	Still	
D Suffix	50°C/W	85°C/W	15°C/W
F Suffix	55°C/W	90°C/W	15°C/W
P Suffix	65°C/W	100°C/W	25°C/W

NOTE 3: The AC limits are guaranteed to be the worst case bit in the memory.

MOTOROLA Semiconductors

MCM93425

1024-BIT RANDOM ACCESS MEMORY

The MCM93425 is a 1024-bit Read/Write RAM, organized 1024 words by 1 bit.

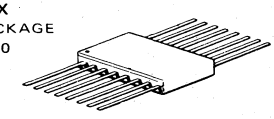
The MCM93425 is designed for high performance main memory and control storage applications and has a typical address time of 35 ns.

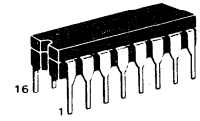
The MCM93425 has full decoding on-chip, separate data input and data output lines, and an active low-chip select and write enable. The device is fully compatible with standard DTL and TTL logic families. A three-state output is provided to drive bus-organized systems and/or highly capacitive loads.

- Three-State Output
- TTL Inputs and Output
- Non-Inverting Data Output
- High Speed –
  - Access Time – 35 ns Typical
  - Chip Select – 15 ns Typical
- Power Dissipation – 0.5 mW/Bit Typical
- Power Dissipation Decreases With Increasing Temperature

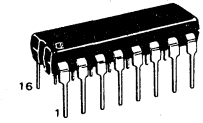
TTL
1024 X 1 BIT
RANDOM ACCESS MEMORY

F SUFFIX
CERAMIC PACKAGE
CASE 650



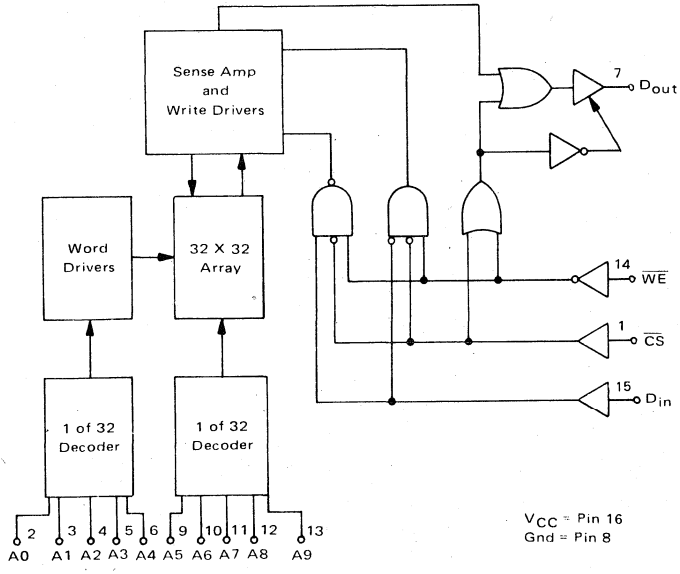


D SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

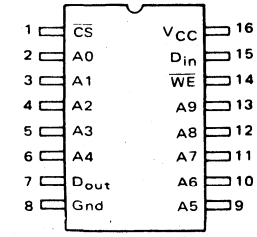
BLOCK DIAGRAM



V_{CC} = Pin 16
Gnd = Pin 8

NOTE: Logic driving sense amp/write drivers depicts negative-only write used on C4m.

PIN ASSIGNMENT



Pin Description

$\overline{CS}$	Chip Select
A0 - A9	Address Inputs
$\overline{WE}$	Write Enable
D_{in}	Data Input
D_{out}	Data Output

DS 9448
(formerly NP-74)

FUNCTIONAL DESCRIPTION

The MCM93425 is a fully decoded 1024-bit Random Access Memory organized 1024 words by one bit. Word selection is achieved by means of a 10-bit address, A0 – A9.

The Chip Select ($\overline{CS}$) input provides for memory array expansion. For large memories, the fast chip select time permits the decoding of chip select from the address without increasing address access time.

The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$, Pin 14). With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{in} is written into the addressed location. To read, $\overline{WE}$ is held high and $\overline{CS}$ held low. Data in the specified location is presented at D_{out} and is non-inverted.

The three-state output provides drive capability for higher speeds with capacitive load systems. The third state (high impedance) allows bus organized systems where multiple outputs are connected to a common bus.

During writing, the output is held in the high-impedance state.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	
Ceramic Package (D and F Suffix)	-55°C to +165°C
Plastic Package (P Suffix)	-55°C to +125°C
Operating Junction Temperature, T_J	
Ceramic Package (D and F Suffix)	< 165°C
Plastic Package (P Suffix)	< 125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
Input Voltage (dc)	-0.5 V to +5.5 V
Voltage Applied to Outputs (Output High)	-0.5 V to +5.5 V
Output Current (dc) (Output Low)	+20 mA
Input Current (dc)	-12 mA to +5.0 mA

TRUTH TABLE

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}	Mode
H	X	X	High Z	Not Selected
L	L	L	High Z	Write "0"
L	L	H	High Z	Write "1"
L	H	X	D_{out}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't Care (High or Low)

NOTE 1: Device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

GUARANTEED OPERATING RANGES (Notes 2 and 3)

Part Number	Supply Voltage (V_{CC})			Ambient Temperature (T_A)
	Min	Nom	Max	
MCM93425DC, PC	4.75 V	5.0 V	5.25 V	0°C to +75°C
MCM93425FM, DM	4.50 V	5.0 V	5.50 V	-55°C to +125°C

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

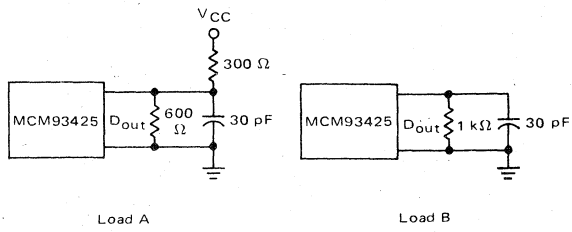
Symbol	Characteristic		Limits Min	Limits Max	Units	Conditions	
V_{OL}	Output Low Voltage			0.45	Vdc	V_{CC} = Min, I_{OL} = 16 mA	
V_{IH}	Input High Voltage		2.1		Vdc	Guaranteed Input High Voltage for all Inputs	
V_{IL}	Input Low Voltage			0.8	Vdc	Guaranteed Input Low Voltage for all Inputs	
I_{IL}	Input Low Current			-400	μAdc	V_{CC} = Max, V_{in} = 0.4 V	
I_{IH}	Input High Current			40	μAdc	V_{CC} = Max, V_{in} = 4.5 V	
				1.0	mAdc	V_{CC} = Max, V_{in} = 5.25 V	
I_{off}	Output Current (High Z)			50	μAdc	V_{CC} = Max, V_{out} = 2.4 V	
				-50		V_{CC} = Max, V_{out} = 0.5 V	
I_{OS}	Output Current Short Circuit to Ground			-100	mAdc	V_{CC} = Max	
V_{OH}	Output High Voltage	MCM93425DC, PC	2.4		Vdc	I_{OH} = -10.3 mA, V_{CC} = 5.0 V ±5%	
		MCM93425FM, DM	2.4		Vdc	I_{OH} = -5.2 mA	
V_{CD}	Input Diode Clamp Voltage			-1.5	Vdc	V_{CC} = Max, I_{in} = -10 mA	
I_{CC}	Power Supply Current			130	mAdc	T_A = Max	V_{CC} = Max, All Inputs Grounded
				155	mAdc	T_A = 0°C	
				170	mAdc	T_A = Min	

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

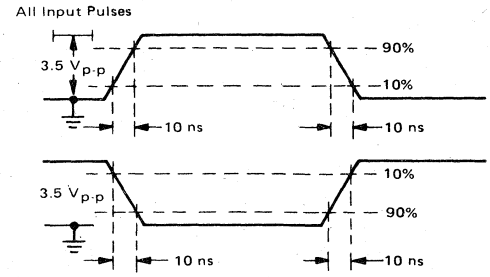
AC TEST LOAD AND WAVEFORMS

Loading Conditions



Load A Load B

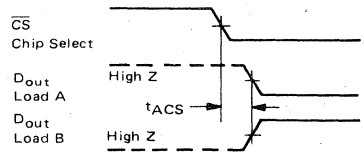
Input Pulses



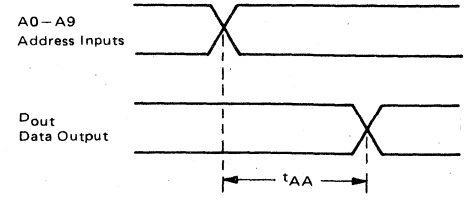
Symbol	Characteristic (Notes 2, 4)	MCM93425DC, PC Min	MCM93425DC, PC Max	MCM93425DM, FM Min	MCM93425DM, FM Max	Units	Conditions
READ MODE	DELAY TIMES					ns	
t_{ACS}	Chip Select Time		35		45		See Test Circuit
t_{ZRCS}	Chip Select to High Z		35		50		and Waveforms
t_{AA}	Address Access Time		45		60		
WRITE MODE	DELAY TIMES					ns	
t_{ZWS}	Write Disable to High Z		35		45		See Test Circuit
t_{WR}	Write Recovery Time		40		50		and Waveforms
	INPUT TIMING REQUIREMENTS					ns	
t_W	Write Pulse Width (to guarantee write)	30		40			See Test Circuit
t_{WSD}	Data Setup Time Prior to Write	5		5			and Waveforms
t_{WHD}	Data Hold Time After Write	5		5			
t_{WSA}	Address Setup Time (at t_W = Min)	10		15			
t_{WHA}	Address Hold Time	10		10			
t_{WSCS}	Chip Select Setup Time	5		5			
t_{WHCS}	Chip Select Hold Time	5		5			

READ OPERATION TIMING DIAGRAM

Propagation Delay from Chip Select

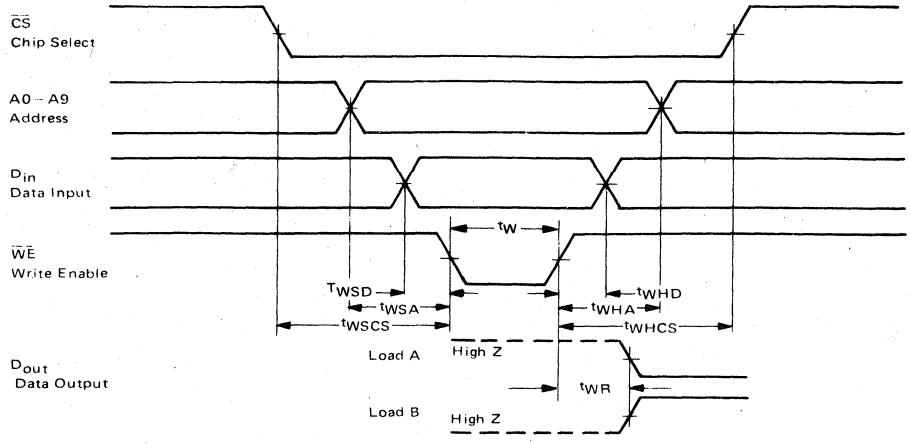


Propagation Delay from Address Inut



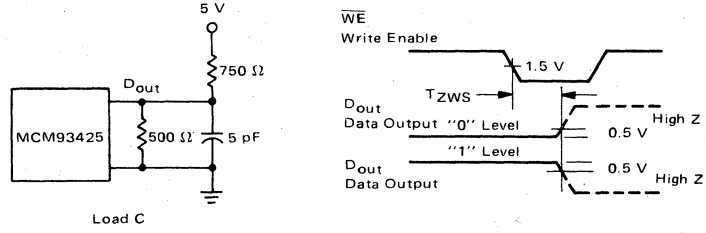
(All time measurements referenced to 1.5 V)

WRITE CYCLE TIMING

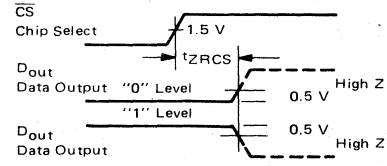


(All above measurements reference to 1.5 V)

WRITE ENABLE TO HIGH Z DELAY



Propagation Delay from Chip Select to High Z



(All t_{ZXXX} parameters are measured at a delta of 0.5 V from the logic level and using Load C)

NOTE 2: DC and AC specifications limits guaranteed with 500 linear feet per minute blown air. Contact your Motorola Sales Representative if extended temperature or modified operating conditions are desired.

Package	θ_{JA} (Junction to Ambient) Blown	θ_{JA} (Junction to Ambient) Still	θ_{JC} (Junction to Case)
D Suffix	50°C/W	85°C/W	15°C/W
F Suffix	55°C/W	90°C/W	15°C/W
P Suffix	65°C/W	100°C/W	25°C/W

NOTE 3: Output short circuit conditions must not exceed 1 second duration.
NOTE 4: The maximum address access time is guaranteed to be the worst case bit in the memory.

MOTOROLA Semiconductors

MCM7680
MCM7681

8192-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM7680/81 together with the MCM7620/21, MCM7640/43 comprise a complete, compatible family having common dc electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable ROMs and are available in commonly used organizations, with both open-collector and three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom-programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time, and features temperature and voltage compensation to minimize access time variations.

Pinouts are compatible to industry-standard PROMs and ROMs. In addition, the MCM7680 and 81 are pin compatible replacement for the 512 X 8 with pin 22 connected as A9 on the 1024 X 8.

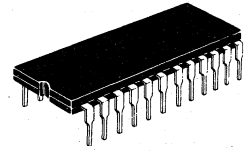
In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (0.1 second per 1024 Bits, Typical)
- Expandable — Open-Collector or Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
  Low Input Current — 250 μA Logic "0", 40 μA Logic "1"
  Full Output Drive — 16 mA Sink, 2.0 mA Source
- Fast Access Time — Guaranteed for Worst-Case N^2 Sequencing, Over Commercial and Military Temperature Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs

MTTL

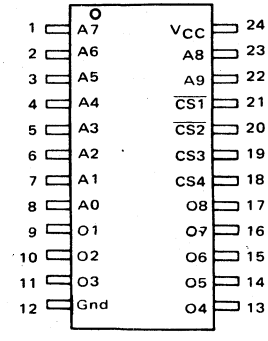
8192-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7680 — 1024 X 8 — Open-Collector
MCM7681 — 1024 X 8 — Three-State



L SUFFIX
CERAMIC PACKAGE
CASE 623

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage (operating)	V_{CC}	+7.0	Vdc
Input Voltage	V_{in}	+5.5	Vdc
Output Voltage (operating)	V_{OH}	+7.0	Vdc
Supply Current	I_{CC}	650	mAdc
Input Current	I_{in}	-20	mAdc
Output Sink Current	I_o	100	mAdc
Operating Temperature Range MCM76xxDM MCM76xxDC	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Maximum Junction Temperature	T_J	+175	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

MTTL is a trademark of Motorola Inc.

DC OPERATING CONDITIONS AND CHARACTERISTICS

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}				Vdc
MCM76xxDM		4.50	5.0	5.50	
MCM76xxDC		4.75	5.0	5.25	
Input High Voltage	V_{IH}	2.0	–	–	Vdc
Input Low Voltage	V_{IL}	–	–	0.8	Vdc

DC CHARACTERISTICS

			Open-Collector Output			Three-State Output			
Symbol	Parameter	Test Conditions	Min	Typ	Max	Min	Typ	Max	Unit
I_{RA}, I_{RE}	Address/Enable "1"	$V_{IH} = V_{CC}$ Max	–	–	40	–	–	40	µAdc
I_{FA}, I_{FE}	Input Current "0"	V_{IL} = 0.45 V	–	-0.1	-0.25	–	-0.1	-0.25	mAdc
V_{OH}	Output Voltage "1"	I_{OH} = -2.0 mA, $V_{CC} = V_{CC}$ Min	N/A	–	–	2.4	3.4	–	Vdc
V_{OL}	"0"	I_{OL} = +16 mA, $V_{CC} = V_{CC}$ Min	–	0.35	0.45	–	0.35	0.45	Vdc
I_{OHE}	Output Disabled "1"	V_{OH}, $V_{CC} = V_{CC}$ Max	–	–	100	–	–	100	µAdc
I_{OLE}	Current "0"	V_{OL} = +0.3 V, $V_{CC} = V_{CC}$ Max	–	–	N/A	–	–	-100	µAdc
I_{OH}	Output Leakage "1"	V_{OH}, $V_{CC} = V_{CC}$ Max	–	–	100	–	–	N/A	µAdc
V_{CL}	Input Clamp Voltage	I_{in} = -10 mA	–	–	-1.5	–	–	-1.5	Vdc
I_{OS}	Output Short Circuit Current	$V_{CC} = V_{CC}$ Max, V_{out} = 0.0 V One Output Only for 1 s Max	N/A	–	N/A	15	–	70	mAdc
I_{CC}	Power Supply Current	$V_{CC} = V_{CC}$ Max							
	MCM7680/MCM7681DC	All Inputs Grounded	–	110	150	–	110	150	mAdc
	MCM7680/MCM7681DM		–	110	170	–	110	170	mAdc

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

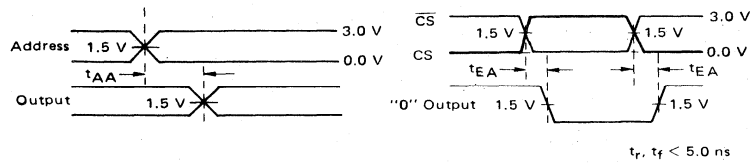
Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	8.0	pF
Output Capacitance	C_{out}	8.0	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

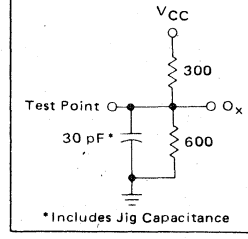
(Full operating voltage and temperature unless otherwise noted)

		0 to +70°C		-55 to +125°C		
Characteristic	Symbol	Typ	Max	Typ	Max	Unit
Address to Output Access Time	t_{AA}	45	70	45	85	ns
Chip Enable Access Time MCM7680/81	t_{EA}	30	40	30	50	ns

TIMING DIAGRAM



AC TEST LOAD



PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the sepcifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

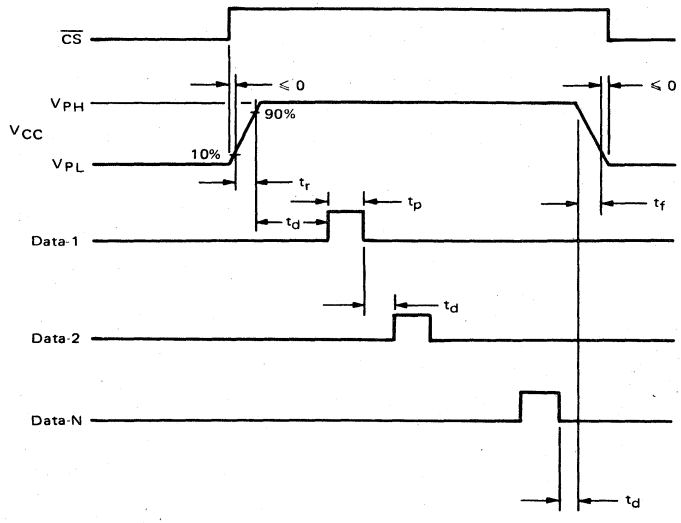
1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying inputs highs (V_{IH}) to the $\overline{CS}$ inputs. CS inputs must remain at V_{IH} for program and verify. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the $\overline{CS}$ inputs.
9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulses of durations shorter than 1.0 ms may be used to enhance programming speed.
10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occurred.

TABLE 1
PROGRAMMING SPECIFICATIONS

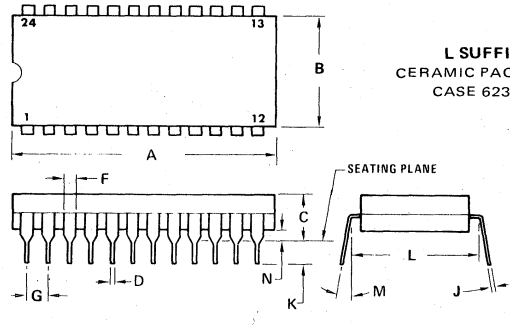
Symbol	Parameter	Min	Typ	Max	Unit
V_{IH} V_{IL}	Address Input Voltage(1)	2.4 0.0	5.0 0.4	5.0 0.8	V V
V_{PH} V_{PL}	Programming/Verify Voltage to V_{CC}	11.75 4.5	12.0 4.5	12.25 5.5	V V
I_{CCP}	Programming Voltage Current Limit Programming (V_{CC})	600	600	650	mA
t_r t_f	Voltage Rise and Fall Time	1 1	1 1	10 10	µs µs
t_d	Programming Delay	10	10	100	µs
t_p	Programming Pulse Width	100	–	1000	µs
DC	Programming Duty Cycle	–	50	90	%
V_{OPE} V_{OPD}	Output Voltage Enable Disable(2)	10.0 4.5	10.5 5.0	11.0 5.5	V V
I_{OPE}	Output Voltage Enable Current	2	4	10	mA
T_C	Case Temperature	–	25	75	°C

(1) Address and chip select should not be left open for V_{IH}.
(2) Disable condition will be met with output open circuit.

FIGURE 1 – TYPICAL PROGRAMMING WAVEFORMS



OUTLINE DIMENSIONS



L SUFFIX
CERAMIC PACKAGES
CASE 623-03

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.29	4.06	0.090	0.160
L	15.24 BSC		0.600 BSC	
M	0^0	15^0	0^0	15^0
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL)

MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MCM82707L,P
MCM82708L,P

Product Preview

TTL
1024 X 8 BIT
PROGRAMMABLE
READ ONLY MEMORY

8192-BIT PROGRAMMABLE READ ONLY MEMORY

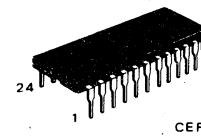
The MCM82707 (open collector output) and MCM82708 (three-state output) are monolithic bipolar 8192-bit Programmable Read Only Memories (PROMs) organized as 1024 words by 8 bits per word. They are supplied with all bits storing a logical "1" (output high), and can be selectively programmed for a logical "0" (output low).

The MCM82707 and MCM82708 both use Motorola's standard fuse technology and are pin compatible withe the MCM68708 MOS EPROM.

The field-programmable PROM can be custom programmed to any pattern using a simple programming procedure. The Schottky Bipolar circuitry provides extremely fast access time.

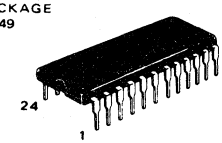
In addition to the conventional storage array, two test rows and two test columns are included to test programmability, and guarantee parametric and A.C. performance.

The MCM82707/82708 is a direct replacement for the MOS EPROM.



L SUFFIX
CERAMIC PACKAGE
CASE 623

P SUFFIX
PLASTIC PACKAGE
CASE 649



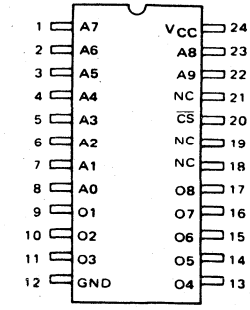
FEATURES

- Pin Compatible with MCM68708 MOS EPROM
- 1024 Words, 8-Bits per Word
- Simple, High Speed Programming Procedure
- Inputs and Outputs TTL Compatible
  - >Low Input Current-10μA Logic "0", 10μA Logic "1" (typical)
  - >Full Output Drive – 15mA Sink/2mA Source
- Fast Access Time – 40ns Typical
- Enable Access Time 20ns Typical
- Expandable – "Wired-Or" Outputs with Chip Select
- 24-Pin Package

APPLICATIONS:

- Microcomputers
- Bipolar Bit Slices
- Look-Up Tables
- Microprograms
- Decode Functions
- Code Conversion
- Number Conversion
- Character Generation

PIN ASSIGNMENT



MOTOROLA Semiconductors

MCM7640 thru MCM7643

4096-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM7640 through 43 PROMs comprise a completely compatible family having common dc electrical characteristics and identical programming requirements. They are fully-decoded, high-speed, field-programmable ROMs and are available in commonly used organizations, with both open-collector and three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time, and features temperature and voltage compensation to minimize access time variations.

All pinouts are compatible to industry-standard PROMs and ROMs.

In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

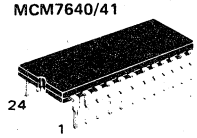
- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (1 Second per 1024 Bits, Typical)
- Expandable – Open-Collector or Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
  Low Input Current – 250 μA Logic "0", 40 μA Logic "1"
  Full Output Drive – 16 mA Sink, 2.0 mA Source
- Fast Access Time – Guaranteed for Worst-Case N^2 Sequencing, Over Commercial and Military Temperature and Voltage Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs

MTTL

4096-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7640 – 512 x 8 – Open-Collector
MCM7641 – 512 x 8 – Three-State
MCM7642 – 1024 x 4 – Open-Collector
MCM7643 – 1024 x 4 – Three-State

MCM7640/41

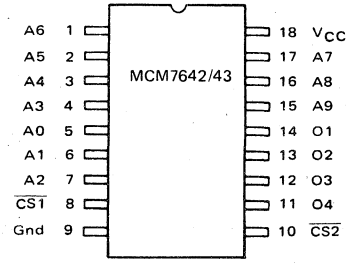


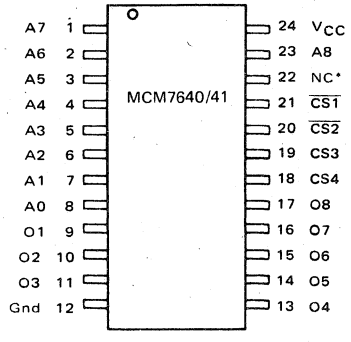
D SUFFIX
CERAMIC PACKAGE

MCM7642/43

D SUFFIX
CERAMIC PACKAGE

PIN ASSIGNMENT





*No Connection

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage (operating)	V_{CC}	+7.0	Vdc
Input Voltage	V_{in}	+5.5	Vdc
Output Voltage (operating)	V_{OH}	+7.0	Vdc
Supply Current	I_{CC}	650	mAdc
Input Current	I_{in}	-20	mAdc
Output Sink Current	I_o	100	mAdc
Operating Temperature Range MCM76xxDM MCM76xxDC	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Maximum Junction Temperature	T_J	+175	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

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DS 9424

DC OPERATING CONDITIONS AND CHARACTERISTICS

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}				Vdc
MCM76xxDM		4.50	5.0	5.50	
MCM76xxDC		4.75	5.0	5.25	
Input High Voltage	V_{IH}	2.0	–	–	Vdc
Input Low Voltage	V_{IL}	–	–	0.8	Vdc

DC CHARACTERISTICS

				Open-Collector Output			Three-State Output			
Symbol	Parameter		Test Conditions	Min	Typ	Max	Min	Typ	Max	Unit
I_{RA}, I_{RE}	Address/Enable	"1"	$V_{IH} = V_{CC}$ Max	–	–	40	–	–	40	μAdc
I_{FA}, I_{FE}	Input Current	"0"	V_{IL} = 0.45 V	–	-0.1	-0.25	–	-0.1	-0.25	mAdc
V_{OH}	Output Voltage	"1"	I_{OH} = -2.0 mA, $V_{CC} = V_{CC}$ Min	N/A	–	–	2.4	3.4	–	Vdc
V_{OL}		"0"	I_{OL} = +16 mA, $V_{CC} = V_{CC}$ Min	–	0.35	0.45	–	0.35	0.45	Vdc
I_{OHE}	Output Disabled	"1"	V_{OH}, $V_{CC} = V_{CC}$ Max	–	–	100	–	–	100	μAdc
I_{OLE}	Current	"0"	V_{OL} = +0.3 V, $V_{CC} = V_{CC}$ Max	–	–	N/A	–	–	-100	μAdc
I_{OH}	Output Leakage	"1"	V_{OH}, $V_{CC} = V_{CC}$ Max	–	–	100	–	–	N/A	μAdc
V_{CL}	Input Clamp Voltage		I_{in} = -10 mA	–	–	-1.5	–	–	-1.5	Vdc
I_{OS}	Output Short Circuit Current		$V_{CC} = V_{CC}$ Max, V_{out} = 0.0 V One Output Only for 1 s Max	N/A	–	N/A	15	–	70	mAdc
I_{CC}	Power Supply Current		$V_{CC} = V_{CC}$ Max							
	MCM7640/MCM7641		All Inputs Grounded	–	100	140	–	100	140	mAdc
	MCM1642/MCM7643			–	100	140	–	100	140	mAdc

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

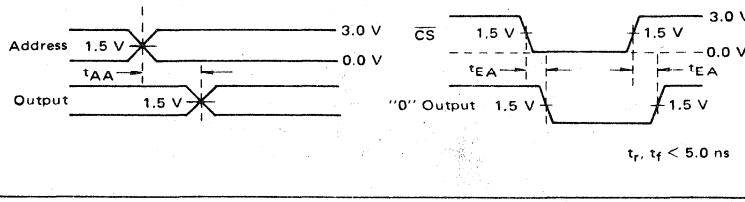
Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	8.0	pF
Output Capacitance	C_{out}	8.0	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

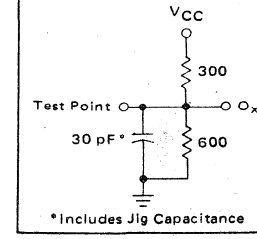
(Full operating voltage and temperature unless otherwise noted)

		0 to +70°C		-55 to +125°C		
Characteristic	Symbol	Typ	Max	Typ	Max	Unit
Address to Output Access Time	t_{AA}	45	70	45	85	ns
Chip Enable Access Time	t_{EA}					ns
MCM7640/7641		30	40	30	50	
MCM7642/7643		15	25	15	30	

TIMING DIAGRAM



AC TEST LOAD



PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the sepcifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

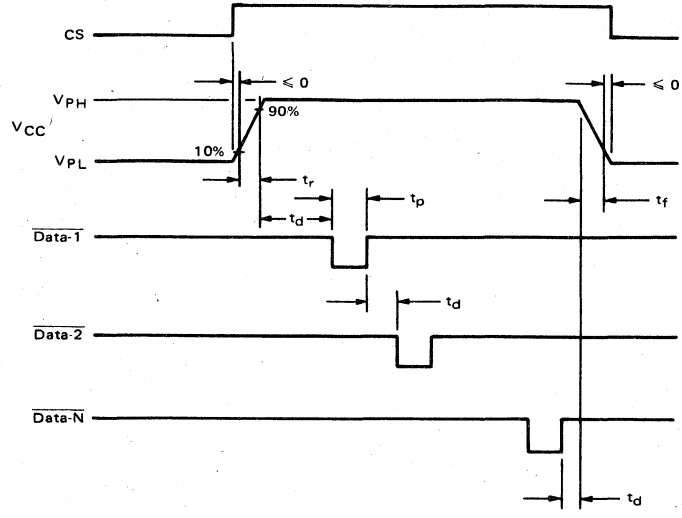
1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying input highs (V_{IH}) to the $\overline{CS}$ input(s). CS inputs (MCM7640/41 only) must remain at V_{IH} for program and verify. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the $\overline{CS}$ input(s).
9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulses of durations shorter than 1.0 ms may be used to enhance programming speed.
10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occurred.

TABLE 1
PROGRAMMING SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Address Input	2.4	5.0	5.0	V
V_{IL}	Voltage(1)	0.0	0.4	0.8	V
V_{PH}	Programming/Verify	11.75	12.0	12.25	V
V_{PL}	Voltage to V_{CC}	4.5	4.5	5.5	V
I_{CCP}	Programming Voltage Current Limit Programming (V_{CC})	600	600	650	mA
t_r	Voltage Rise and	1	1	10	µs
t_f	Fall Time	1	1	10	µs
t_d	Programming Delay	10	10	100	µs
t_p	Programming Pulse Width	100	–	1000	µs
DC	Programming Duty Cycle	–	50	90	%
	Output Voltage				
V_{OPE}	Enable	10.0	10.5	11.0	V
V_{OPD}	Disable(2)	4.5	5.0	5.5	V
I_{OPE}	Output Voltage Enable Current	2	4	10	mA
T_C	Case Temperature	–	25	75	°C

(1) Address and chip select should not be left open for V_{IH}.
(2) Disable condition will be met with output open circuit.

FIGURE 1 – TYPICAL PROGRAMMING WAVEFORMS



MOTOROLA Semiconductors

MCM7621
MCM7620

MTTL

2048-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7620 – 512 X 4 – Open-Collector
MCM7621 – 512 X 4 – Three-State

2048-BIT PROGRAMMABLE READ ONLY MEMORY

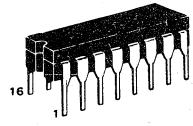
The MCM7620/MCM7621 have common dc electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable ROMs and are available with open-collector or three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time, and features temperature and voltage compensation to minimize access time variations.

All pinouts are compatible to industry-standard PROMs and ROMs.

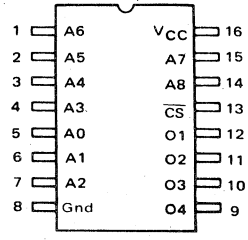
In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (0.1 Second per 1024 Bits, Typical)
- Expandable – Open-Collector or Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
  Low Input Current – 250 μA Logic "0", 40 μA Logic "1"
  Full Output Drive – 16 mA Sink, 2.0 mA Source
- Fast Access Time – Guaranteed for Worst-Case N^2 Sequencing, Over Commercial and Military Temperature and Voltage Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs



L SUFFIX
CERAMIC PACKAGE
CASE 620

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage (operating)	V_{CC}	+7.0	Vdc
Input Voltage	V_{in}	+5.5	Vdc
Output Voltage (operating)	V_{OH}	+7.0	Vdc
Supply Current	I_{CC}	650	mAdc
Input Current	I_{in}	-20	mAdc
Output Sink Current	I_o	100	mAdc
Operating Temperature Range MCM76xxDM MCM76xxDC	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Maximum Junction Temperature	T_J	+175	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

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DC OPERATING CONDITIONS AND CHARACTERISTICS

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}				Vdc
MCM76xxDM		4.50	5.0	5.50	
MCM76xxDC		4.75	5.0	5.25	
Input High Voltage	V_{IH}	2.0	–	–	Vdc
Input Low Voltage	V_{IL}	–	–	0.8	Vdc

DC CHARACTERISTICS

			Open-Collector Output			Three-State Output			
Symbol	Parameter	Test Conditions	Min	Typ	Max	Min	Typ	Max	Unit
I_{RA}, I_{RE}	Address/Enable "1"	$V_{IH} = V_{CC}$ Max	–	–	40	–	–	40	µAdc
I_{FA}, I_{FE}	Input Current "0"	$V_{IL} = 0.45$ V	–	-0.1	-0.25	–	-0.1	-0.25	mAdc
V_{OH}	Output Voltage "1"	$I_{OH} = -2.0$ mA, $V_{CC} = V_{CC}$ Min	N/A	–	–	2.4	3.4	–	Vdc
V_{OL}	"0"	$I_{OL} = +16$ mA, $V_{CC} = V_{CC}$ Min	–	0.35	0.45	–	0.35	0.45	Vdc
I_{OHE}	Output Disabled "1"	V_{OH}, $V_{CC} = V_{CC}$ Max	–	–	100	–	–	100	µAdc
I_{OLE}	Current "0"	$V_{OL} = +0.3$ V, $V_{CC} = V_{CC}$ Max	–	–	N/A	–	–	-100	µAdc
I_{OH}	Output Leakage "1"	V_{OH}, $V_{CC} = V_{CC}$ Max	–	–	100	–	–	N/A	µAdc
V_{CL}	Input Clamp Voltage	$I_{in} = -10$ mA	–	–	-1.5	–	–	-1.5	Vdc
I_{OS}	Output Short Circuit Current	$V_{CC} = V_{CC}$ Max, $V_{out} = 0.0$ V One Output Only for 1 s Max	N/A	–	N/A	15	–	70	mAdc
I_{CC}	Power Supply Current MCM7620/MCM7621	$V_{CC} = V_{CC}$ Max All Inputs Grounded	–	60	100	–	60	100	mAdc

CAPACITANCE (f = 1.0 MHz, $T_A = 25^oC$, periodically sampled rather than 100% tested.)

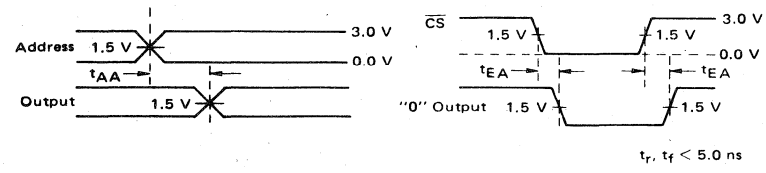
Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	8.0	pF
Output Capacitance	C_{out}	8.0	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

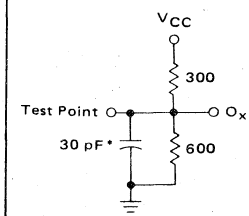
(Full operating voltage and temperature unless otherwise noted)

		0 to +70°C		-55 to +125°C		
Characteristic	Symbol	Typ	Max	Typ	Max	Unit
Address to Output Access Time	t_{AA}	45	70	45	85	ns
Chip Enable Access Time MCM7620/7621	t_{EA}	15	25	15	30	ns

TIMING DIAGRAM



AC TEST LOAD



PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the sepcifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

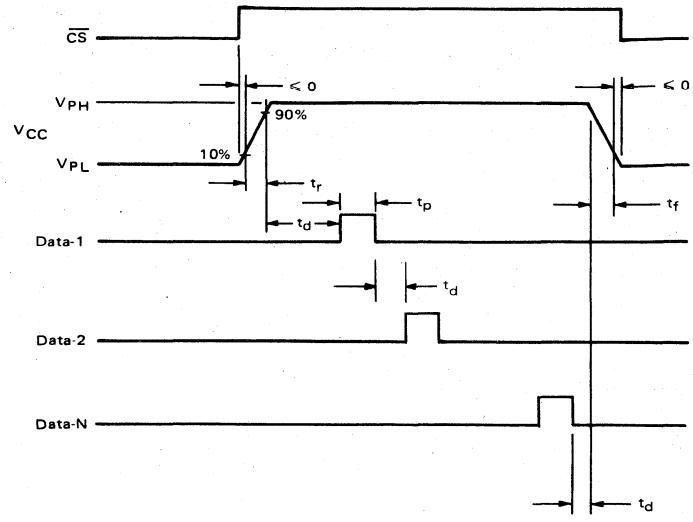
1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying input highs (V_{IH}) to the $\overline{CS}$ input. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the $\overline{CS}$ input.
9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulses of durations shorter than 1.0 ms may be used to enhance programming speed.
10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occurred.

TABLE 1
PROGRAMMING SPECIFICATIONS

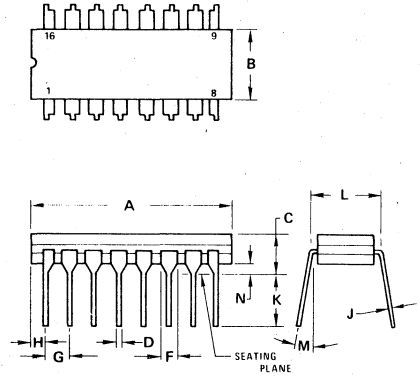
Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Address Input	2.4	5.0	5.0	V
V_{IL}	Voltage(1)	0.0	0.4	0.8	V
V_{PH}	Programming/Verify	11.75	12.0	12.25	V
V_{PL}	Voltage to V_{CC}	4.5	4.5	5.5	V
I_{CCP}	Programming Voltage Current Limit Programming (V_{CC})	600	600	650	mA
t_r	Voltage Rise and	1	1	10	µs
t_f	Fall Time	1	1	10	µs
t_d	Programming Delay	10	10	100	µs
t_p	Programming Pulse Width	100	–	1000	µs
DC	Programming Duty Cycle	–	50	90	%
	Output Voltage				
V_{OPE}	Enable	10.0	10.5	11.0	V
V_{OPD}	Disable(2)	4.5	5.0	5.5	V
I_{OPE}	Output Voltage Enable Current	2	4	10	mA
T_C	Case Temperature	–	25	75	°C

(1) Address and chip select should not be left open for V_{IH}.
(2) Disable condition will be met with output open circuit.

FIGURE 1 – TYPICAL PROGRAMMING WAVEFORMS



OUTLINE DIMENSIONS



L SUFFIX
CERAMIC PACKAGE
CASE 620-06

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.94	0.750	0.785
B	6.22	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.38	0.51	0.015	0.020
F	0.89	1.65	0.035	0.065
G	2.54 BSC		0.100 BSC	
H	0.38	1.52	0.015	0.060
J	0.20	0.30	0.008	0.012
K	3.18	5.08	0.125	0.200
L	7.37	8.13	0.290	0.320
M	–	15°	–	15°
N	0.51	1.27	0.020	0.050

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "A" AND "B" (620-06) DO NOT INCLUDE GLASS RUN-OUT.
4. DIM "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW BODY).

MOTOROLA Semiconductors

MCM5303
MCM5003
MCM5304
MCM5004

MTTL

512-BIT PROGRAMMABLE READ ONLY MEMORY

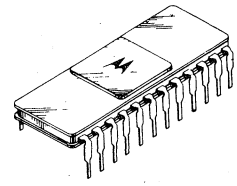
512-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM5303/5003 and MCM5304/5004 are monolithic bipolar 512-bit Programmable Read Only Memories (PROMs) organized as 64 eight-bit words. These memories are field programmable, i.e., the user can custom program these memories himself. Metal interconnections establish each bit initially in the logic "0" state. By "blowing" appropriate nichrome resistors and thus breaking metalization links these bits can be changed to the logic "1" state to meet specific program requirements. Detailed programming instructions are contained in this data sheet.

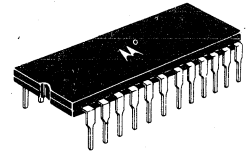
The MCM5303/5003 and MCM5304/5004 have six address inputs to select the proper word and two chip enable inputs, as well as outputs for each of the eight bits.

The MCM5303 and MCM5304 are specified over an operating temperature range of -55°C to +125°C. The MCM5003 and MCM5004 are specified over an operating temperature range of 0°C to +70°C.

The MCM5303 and MCM5003 have positive enables with open collector outputs. The MCM5304 and MCM5004 have positive enables with 2.0 kilohm pullup resistors on the collector outputs.



AL SUFFIX
CASE 684
CERAMIC PACKAGE

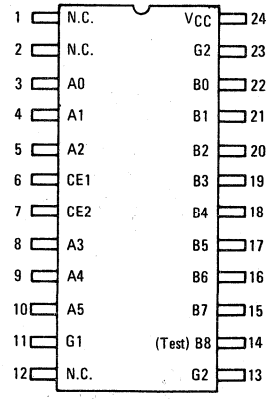


L SUFFIX
CERAMIC PACKAGE
CASE 623

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	Vdc
Input Voltage	V_{in}	-1.0 to +5.5	Vdc
Output Voltage (Open collectors)	V_{OH}	-0.5 to +7.0	Vdc
Thermal Resistance	θ_{JA}	100	°C/W
Operating Temperature Range MCM5303, MCM5304 MCM5003, MCM5004	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +165	°C

PIN ASSIGNMENT



FEATURES:

- Positive Logic for Both Inputs and Outputs
  Logic "0" = Output Device ON (V_{OL})
  Logic "1" = Output Device OFF (V_{OH})
- Logic Levels Compatible with MDTL and All MTTL Families
- Ninth Bit Available for Circuit Test
- Access Time < 75 ns
- Outputs Sink 12 mA Open Collector, 10 mA with Pullup Resistors
- Field Programmable by Blowing Nichrome Links
- Hermetic Package

APPLICATIONS:

- Look Up Tables
- Micro Programs
- Decode Functions
- Code Conversion
- Number Conversion
- Random Logic
- Character Generation

MTTL and MDTL are trademarks of Motorola Inc.

DC ELECTRICAL CHARACTERISTICS (T_A = -55°C to +125°C for MCM5303 and MCM5304, 0°C to +70°C for MCM5003 and MCM5004 unless otherwise noted)

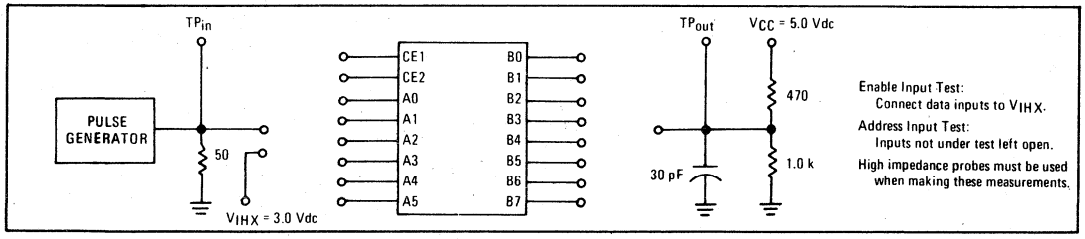
Characteristic		Symbol	Min	Max	Unit
Input Forward Current (V_{IL} = 0.4 Vdc, V_{CC} = 5.25 Vdc)		I_{IL}	–	1.6	mAdc
Input Leakage Current (V_{IH} = V_{CC} = 5.25 Vdc)		I_{IH}	–	100	µAdc
Logic "0" Output Voltage*		V_{OL}			Vdc
(T_A = 0°C to +125°C for MCM5303 and MCM5304, 0°C to +70°C for MCM5003 and MCM5004)					
(I_{OL} = 12 mAdc, V_{CC} = 4.75 Vdc)	Open Collectors		–	0.45	
(I_{OL} = 10 mAdc, V_{CC} = 4.75 Vdc)	Pullup Resistors		–	0.45	
(T_A = -55°C for MCM5303 and MCM5304)					
(I_{OL} = 12 mAdc, V_{CC} = 4.75 Vdc)	Open Collectors		–	0.50	
(I_{OL} = 10 mAdc, V_{CC} = 4.75 Vdc)	Pullup Resistors		–	0.50	
Logic "1" Output Voltage (I_{OH} = −0.5 mAdc, V_{CC} = 4.75 Vdc)	Pullup Resistors	V_{OH}	2.5	–	Vdc
Output Leakage Current (V_{CC} = V_{CEX} = 5.25 Vdc)	Open Collectors	I_{CEX}	–	200	µAdc
Power Supply Drain Current		I_{CC}			mAdc
(Enable and all other inputs	Open Collectors		–	95	
grounded, V_{CC} = 5.0 Vdc)	Pullup Resistors		–	120	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, T_A = 25°C)

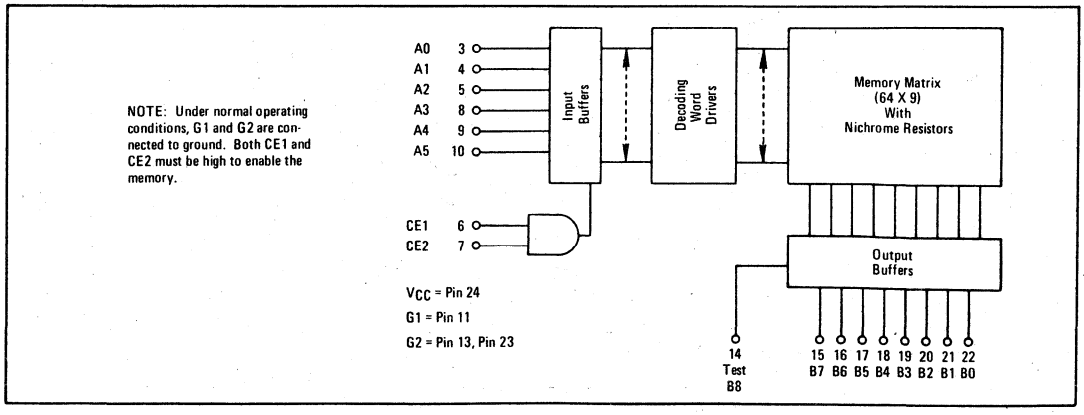
Access Times* (30pF Load)				ns
Address to Output	t_{AO}	25	75	
Enable to Output	t_{EO}	25	75	

*Pin 13 is schematically connected to G2. For optimum propagation delay and V_{OL} characteristics, externally tie Pin 13 to Pin 23 (G2).

SWITCHING TIME TEST CIRCUIT



BLOCK DIAGRAM



PROGRAMMING THE MCM5303/5003 AND MCM5304/5004

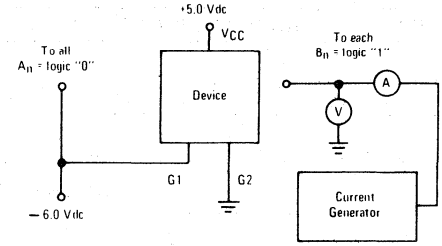
The table and diagram below give instructions for field programming the MCM5303/5003 and MCM5304/5004. All data given is for ambient temperatures of 25°C. If necessary, further programming aid can be obtained from Motorola engineering and product marketing personnel by contacting your nearest Motorola sales office.

Programming Voltage Limits

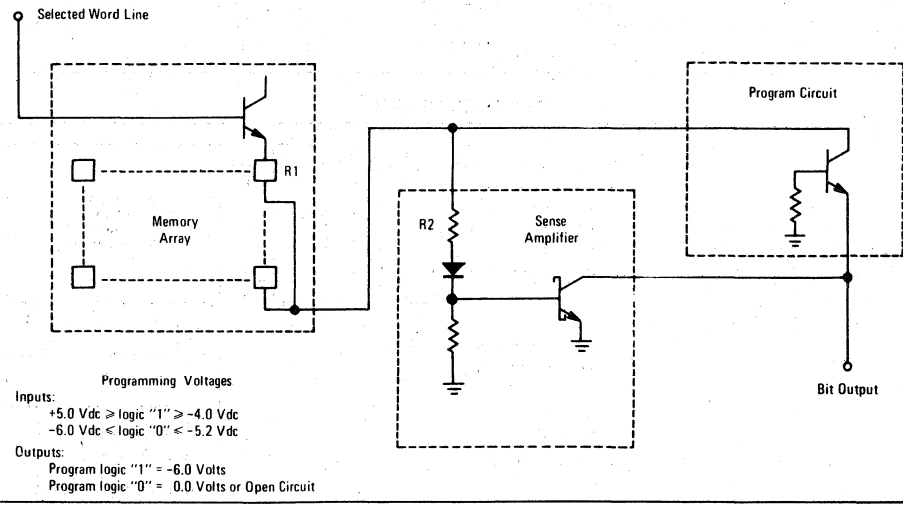
	Symbol	Value	Unit
Address and Chip Enable Voltages	V_{IH} V_{IL}	−4.0 to +5.0 −6.0 to −5.2	Vdc
Power Supply Voltage	V_{CC}	+5.0 ±5%	Vdc
G1 Voltage	V_{G1}	-6.0 ±5%	Vdc
G2 Voltage	V_{G2}	0.0	Vdc
Program Voltage at Desired Bit Output	V_{BP}	-6.0 ±5%	Vdc

Programming Procedure

1. Select the address code desired. Connect low (logic "0") inputs to −6.0 Vdc nominal. Leave high (logic "1") inputs unconnected.
2. With the output voltage of a 120-mA current generator clamped to −6.0 Vdc, apply a negative-going current pulse of 800 ms duration to any output to be programmed as a logic "1".
3. Repeat step 2 for each output to be programmed as a logic "1", one bit at a time.
4. Select next address code desired and repeat steps 2 and 3.



Link Programming Diagram



TRUTH TABLE FORMAT

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WORD 0								
WORD 1								
WORD 2								
WORD 3								
WORD 4								
WORD 5								
WORD 6								
WORD 7								
WORD 8								
WORD 9								
WORD 10								
WORD 11								
WORD 12								
WORD 13								
WORD 14								
WORD 15								
WORD 16								
WORD 17								
WORD 18								
WORD 19								
WORD 20								
WORD 21								
WORD 22								
WORD 23								
WORD 24								
WORD 25								
WORD 26								
WORD 27								
WORD 28								
WORD 29								
WORD 30								
WORD 31								

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WORD 32								
WORD 33								
WORD 34								
WORD 35								
WORD 36								
WORD 37								
WORD 38								
WORD 39								
WORD 40								
WORD 41								
WORD 42								
WORD 43								
WORD 44								
WORD 45								
WORD 46								
WORD 47								
WORD 48								
WORD 49								
WORD 50								
WORD 51								
WORD 52								
WORD 53								
WORD 54								
WORD 55								
WORD 56								
WORD 57								
WORD 58								
WORD 59								
WORD 60								
WORD 61								
WORD 62								
WORD 63								

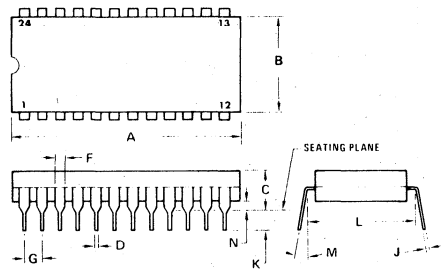
WHY THE NINTH BIT?

The ninth bit was designed into the MCM5303/MCM5003 and the MCM5304/MCM5004 because field-programmable ROMs present testing problems not encountered with conventional mask-programmable ROMs.

Three areas of testing are affected: Program Element Testing, Functional Testing, and AC Testing. The ninth bit helps to solve the problem of Program Element Testing by assuring that links can be blown without destroying any of the normal 64x8 bit array.

Functional and ac performance are assured by verifying that changes do occur at the outputs as the addresses change. This is important in that all of the outputs are in a logic "0" state regardless of the address selected, and no way is available to determine whether the functions are correctly operating without the ninth testing bit.

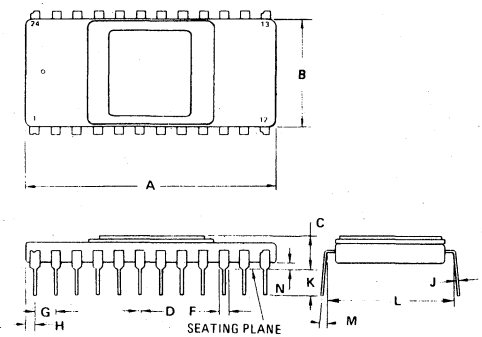
PACKAGE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.06	5.08	0.160	0.200
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	15.37 BSC		0.605 BSC	
M	5°	15°	5°	15°
N	0.51	0.76	0.020	0.030

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL)

CASE 623

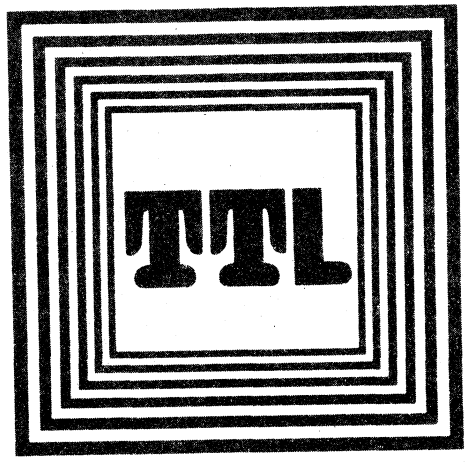


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	29.34	30.86	1.155	1.215
B	12.70	14.22	0.500	0.560
C	3.05	3.94	0.120	0.155
D	0.38	0.51	0.015	0.020
F	0.89	1.40	0.035	0.055
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.30	0.008	0.012
K	2.92	3.68	0.115	0.145
L	14.86	15.87	0.585	0.625
M		15°		15°
N	0.51	1.14	0.020	0.045

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE WITH MAXIMUM MATERIAL CONDITION.
2. LEAD NO. 1 CUT FOR IDENTIFICATION, OR BUMP ON TOP.
3. DIM "L" TO INSIDE OF LEADS. (MEASURED 0.51 mm (0.020) BELOW PKG BASE)

CASE 684

LOW POWER SCHOTTKY



Reliability Data

STANDARD PROGRAMS

MIL-STD-883 OPERATIONS METHOD	PROCESSING PER 5004/5005	HIGH RELIABILITY PROCESSED PROGRAMS		MIL-M-38510 JAN QUALIFIED
SCREEN	**CLASS B METHOD**	**"SNC"**	**"SNJ"**	**CLASS B**
Internal Visual (Precap)	2010 Condition B and 38510	100%	100%	100%
Stabilization Bake	1008 Condition C	100%	100%	100%
Temperature Cycling	1010 Condition C	100%	100%	100%
Constant Acceleration	2001 Condition E (min.) Y_1 plane	100%	100%	100%
Seal (a) Fine (b) Gross	1014, Condition B 1014, Condition C	100%	100%	100% 100%
Interim Electrical Parameters	Per applicable device specification	Optional[1]	Optional[1]	Optional[1]
Burn-in Test	1015 160 Hrs. @ 125° C Min.	100%	100%	100%
Final Electrical Tests (a) Static tests (1) 25°C (subgroup 1, table 1, 5005) (2) Max. and min. rated operating temp. (subgroups 2 and 3, table 1, 5005) (b) Dynamic tests and/or switching tests @ 25°C (subgroup 4 and 9, table 1, 5005) (c) Functional test @ 25°C (subgroup 7, table 1, 5005)	Per applicable device specification	 100% (2) (2) —	 100% 100% 100% 100%	 100% 100% 100% 100%
Qualification or Quality Conformance Inspection	5005	Group A[3]	Group A[3]	per 38510[3]
External Visual	2009	100%	100%	100%

[1]When specified in the applicable device specification, 100% of the devices shall be tested at Manufacturer's option.

[2]100% DC guard band tested @ 25°C.

[3]Full 5005 Conformance testing performed on Jan qualified product. Group A performed on Motorola High Reliability processed product with either Generic or group B, C, D testing available.

ORDERING & MARKING
of "SNC" & "SNJ" HIGH RELIABILITY PROGRAMS

SNC54LS00J

PROGRAM PREFIX	GENERIC PART NUMBER	PACKAGE SUFFIX
1. SNC 2. SNJ		J = DUAL-IN-LINE CERAMIC TIN PLATE LEADS W = CERAMIC FLAT PACK TIN PLATE LEADS

ORDERING & MARKING of JAN QUALIFIED PROGRAM

JM38510/30001BCB

MILITARY DESIGNATOR	CLASS	LEAD FINISH
device type as designated by the applicable military specification (slash sheet)		1. A—HOT SOLDER DIP 2. B—TIN PLATE 3. C—GOLD PLATE 4. X—DON'T CARE

CASE OUTLINE

1. A—¼" × ¼" flat pack, 14-pin
2. B—⅛" × ¼" flat pack, 14-pin
3. C—¼" × ¾" dual-in-line, 14-pin
4. D—¼" × ⅜" flat pack, 14-pin
5. E—¼" × ¾" dual-in-line, 16-pin
6. F—¼" × ⅜" flat pack, 16-pin
7. G—8-lead can
8. H—¼" × ¼" flat pack, 10-lead
9. I—10-lead can
10. J—½" × 1¼" dual-in-line, 24-pin
11. K—⅜" × ⅝" flat pack, 24-pin
12. L—⅜" × ½" flat pack, 24-pin
13. M—12-lead can
14. N—(Size *N/D) flat pack, 24-pin
15. P—¼" × ⅜" dual-in-line, 8-pin
16. Q—0.60" × 2.00" dual-in-line, 40-pin
17. R—(Size *N/D) dual-in-line, 20-pin
18. S—(Size *N/D) flat pack, 20-pin
19. T—(Size *N/D) flat pack, 22-pin
20. U—0.40" × 0.40" leadless flat pack, 24-pin
21. V—0.30" × 1.00" dual-in-line, 18-pin
22. W—0.40" × 1.10" dual-in-line, 22-pin
23. X } Variable per applicable slash sheet
24. Y }
25. Z—¼" × ⅜" flat pack, 24-pin

*N/D — NOT DEFINED

THE "BETTER" PROGRAM

Motorola's reliability and quality-enhancement program was developed to provide improved levels of quality and reliability for standard commercial products.

The "BETTER" program is offered on TTL/LS, in dual-in-line ceramic and plastic packages.

Motorola standard commercial integrated circuits are manufactured under stringent in-process controls and quality inspections combined with the industries' finest outgoing quality inspections. The "BETTER" program offers three levels of extra processing, each tailored to meet different user needs at nominal costs.

The program is designed to:

- Eliminate incoming electrical inspection
- Eliminate need for independent test labs and associated extra time and costs
- Reduce field failures
- Reduce service calls
- Reduce equipment downtime
- Reduce board and system rework
- Reduce infant mortality
- Save time and money
- Increase end-customer satisfaction

BETTER PROCESSING – STANDARD PRODUCT PLUS:

LEVEL I (Suffix S)

- 100% temperature cycling per MIL-STD-883A. Method 1010, ten cycles from −25°C to +150°C.
- 100% high temperature functional test at +100°C.

LEVEL II (Suffix D)

- 100% burn-in to MIL-STD-883A test conditions equivalent to 160 hours at +125°C.
- 100% post burn-in DC parametric test at 25°C.

LEVEL III (Suffix DS)

- Combination of Levels I and II above.

"BETTER" AQL GUARANTEES

TEST	CONDITION	AQL[2]		
		LEVEL I	LEVEL II	LEVEL III
HIGH TEMPERATURE FUNCTIONAL	TA = 100°C	0.15	0.15*	0.10
DC PARAMETRIC	TA = 25°C	0.28	0.28	0.28
DC PARAMETRIC	TA MIN, TA MAX	0.40	0.40	0.40
AC PARAMETRIC	TA = 25°C	0.65	0.65	0.65
EXTERNAL VISUAL AND MECHANICAL[1]	MAJOR	0.11	0.11	0.11
	MINOR	2.50	2.50	2.50
HERMETICITY (NOT APPLICABLE TO PLASTIC PACKAGES)	GROSS	0.40	0.40	0.40
	FINE	1.00	1.00	1.00

*25°C
[1]MAJOR DEFECTS — AFFECTS FORM, FIT, OR FUNCTION. MINOR DEFECTS — COSMETIC
[2]GENERAL INSPECTION LEVEL II

HOW TO ORDER

SN74LS00 — **Part Identification**

N — **Standard Package Suffix**

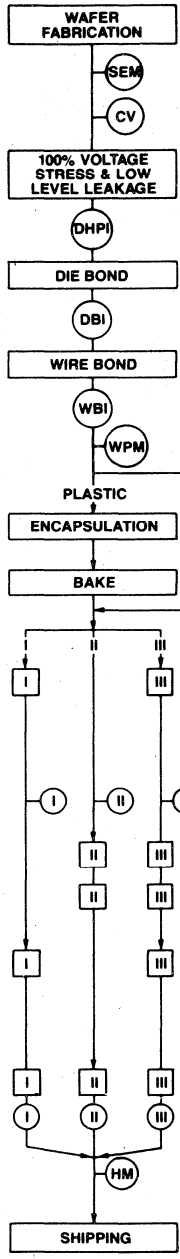
S — **BETTER PROCESSING**
LEVEL I = SUFFIX S
LEVEL II = SUFFIX D
LEVEL III = SUFFIX DS

PART MARKING

The Standard Motorola part number with the corresponding "BETTER" suffix can be ordered from your local authorized Motorola distributor or Motorola sales offices. "BETTER" pricing will be quoted as an adder to standard commercial product price.

GENERALIZED PRODUCT FLOW

Generalized product flow for all Motorola Bipolar Integrated Circuits purchased to the "BETTER" program.



Scanning Electron Microscope Wafer Process Control Monitor: To control oxide step profiles, contact coverage, and metallization integrity.

CV Plot Wafer Process Control Monitor: To control field inversion potential, base inversion — surface channel formation, and to detect any spurious contamination problems.

Performed at final wafer probe (or, optionally, at final electrical test) to screen out potential pinhole shorts, interlayer metal shorts, N+ crossunder shorts, diffusion faults, and similar defects that cannot be detected by visual die high-power inspection.

Die High-Power Sample Gate Inspection: Performed by in-process Q.A. to an 8.0% AQL to detect any damage caused by 100% wafer probe or mechanical scribe and break operation, or any scratches, metallization smears, or glass on bonding pads.

Die Bond Sample Gate Inspection: Performed by in-process Q.A. to a 1.0% AQL to detect any misaligned or tilted die and to assure adequate "wetting" for low thermal resistance and high die shear strength.

Wire Bond Sample Gate Inspection: Performed by in-process Q.A. to a 1.0% AQL to detect any improper wire bonds or wire dress, and any wire bonder damage.

Wire Pull Monitor: Performed by in-process Q.A. to maintain process control of bond strength values per MIL-STD-883A, Method 2011, Condition D.

Motorola Proprietary Epoxy Molding Compound: Meets or exceeds U.L. flame-retarding level UL94V-1.

Post Encapsulation Bake: Eight hours at 150°C. Final cure for molding compound; also stresses wire and die bonds and helps eliminate marginal devices.

100% Temperature Cycling: MIL-STD-883A, Method 1010, ten cycles −25°C to +150°C. Exercising circuits ten times over a 175°C range stresses the die and wire bonds and generally eliminates any marginal bonds and also screens out some types of wafer defects (pinholes, interlayer metal shorts, marginal step coverage, N+ crossunder shorts) and marginal seals in hermetic packages. This screening is superior to thermal shock screening because it does not introduce latent failures in ceramic packages (microcracks in seals) or in plastic packages (entrapped liquid) that can result from liquid-to-liquid thermal shock.

Hermeticity Monitor: Hermetic packages only — conbination fine/gross leak test per modification of MIL-STD-883A, Method 1014B. (5×10^{-8} ATM CC/SEC to 1×10^{-4} ATM CC/SEC). Sampled to a 0.65% AQL.

100% Electrical: Functional and DC parametrics at 25°C.

100% Burn-In: MIL-STD-883A, Method 1015, for 160 hours minimum at TA of 125°C minimum (or equivalent, per Arrhenius equation with 1.0eV activation energy). Test condition depends on device type, but generally condition A or C.

100% High-Temperature Functional: Devices are functionally tested at 100°C, 15°C to 30°C above maximum rated operating temperatures, to assure reliable operation at elevated temperatures and to screen out marginally performing devices that could otherwise lower field reliability. Although epoxy molding compounds have essentially eliminated the thermal intermittent failure mode, this screen provides protection from any "maverick" intermittent device being shipped to a customer. This screening is more effective than hot rail "continuity" testing because non-functional devices can often pass a continuity test.

100% Electrical: Functional and DC parametrics at 25°C.

Q.A. Electrical and Mechanical Final Acceptance Tests: Sampled to the tightened AQL levels of Table I.

Hermeticity Monitor: Hermetic packages only. Fine leak per MIL-STD-883A, Method 1014B (5×10^{-8} ATM CC/SEC) and gross leak per MIL-STD-883A, Method 1014C2. Sampled to a combined AQL of .46%.

"RAP"
RELIABILITY AUDIT PROGRAM
for
BIPOLAR DIGITAL INTEGRATED CIRCUITS

1.0 INTRODUCTION

In January, 1977, Motorola Bipolar Digital Reliability Engineering implemented "RRAP" (Rapid Reliability Assessment Program) to provide rapid assessment of the reliability of newly introduced TTL Low-Power Schottky (LS) devices. This RRAP concept permits rapid feedback of information on any reliability problems to the Product Engineering group so that corrective action can be quickly implemented. The RRAP program is performed by the Reliability Engineering Department on samples submitted by Product, Process, or Package Engineering for obtaining a rapid look at the reliability of new products, processes, or packages. This program has been extended to standard TTL, TTL Memories, MDTL, MHTL, Diode Arrays, MECL III, MECL 10K, MECL Memories, and Phase Lock Loop (PLL) product families. The details of the RRAP program are outlined in Section 2.0.

In March, 1977, an addition was made to the RRAP program for the purpose of auditing the reliability of outgoing TTL Low-Power Schottky (LS) product. This new audit presently called the Reliability Audit Program ("RAP"), is performed weekly and reported monthly by the Quality Assurance Group but will be directed by Bipolar Digital Reliability Engineering. The details of this new program are outlined in Section 3.0.

2.0 RAPID RELIABILITY ASSESSMENT PROGRAM (RRAP)

2.1 Hermetic Packaged Devices (50 Units per Evaluation Sample)

a. Electrical I (initial rejects removed from test)
b. Temp Cycling - 30 cycles (–65°C/+150°C) per Method 1010C
c. Electrical I (plus Hermeticity per Method 1014 B & C for package evaluations only)
d. "Equivalent" Burn-In for 40 hrs at 145°C per Method 1015 A or C
e. Electrical I
f. De-cap for Internal Visual Inspection - (3 units) per Method 2014
g. Solderability - (3 units) per Method 2003

2.2 Plastic Packaged Devices (100 Units per Evaluation Sample)

S/G 1 (30 Units)

a. Electricals I & II
b. Thermal Shock - 200 cycles (–55°C/+125°C - 30 Sec. dwell) Method 1011B, modified
c. Electricals I & II

S/G 2 (40 Units)

a. Electricals I & II
b. 16 hrs, PTHB; Rated V_{CC} (15 psig, 100%RH, 121°C) Motorola test method
c. Electrical IV

S/G 3 (30 Units)

a. Electricals I & II
b. Temp Cycling - 30 cycles (–65°C/+150°C). Method 1010C
c. Electricals II & III
d. "Equivalent" Burn-In (40 hrs @ 145°C) per Method 1015 A or C
e. Electricals I & II
f. De-cap for internal visual - (3 units) per Method 2014
g. Solderability - (3 units) per Method 2003

NOTES:

1. All tests per MIL-STD-883 unless stated otherwise.
2. Electrical I = DC @ 25°C and Hi Temp + AC @ 25°C - Go/No/Go
3. Electrical II = Bond Integrity (continuity) @ 125°C - Go/No/Go
4. Electrical III = DC @ 25°C & Hi Temp - Go/No/Go
5. Electrical IV = DC @ 25°C - Go/No/Go
6. 40 hr/145°C burn-in is "equivalent" to 160 hr/125°C burn-in using 1.0eV activation energy and the Arrhenius equation for determining acceleration factor.
7. 16 hrs of PTHB testing is equivalent to approximately 800 hrs of standard 85°C/85% RH THB testing for $V_{CC} < 15$ V, based on comparative tests performed by Motorola Reliability Engineering.
8. For each evaluation, the goal is zero failures. Any indicated failure is first verified and then submitted to the Product Analysis Lab for detailed analysis. Results of evaluation, along with analysis of any failure(s), are reviewed promptly with responsible product, process, or package engineer.

3.0 RELIABILITY AUDIT PROGRAM (RAP) - per 12MRM15301A

3.1 **PTHB** - 15 psig/121°C/100% RH at nominal V_{CC} for 16 hours - performed on a weekly basis - 0 rejects allowed out of 40 devices. (To be performed on plastic encapsulated devices only.)

3.2 **Temp Cycling** - MIL-STD-883, Method 1010, 1000 cycles, Condition C, –65°C/+150°C. Interim readout at 30 cycles (plastic and hermetic packages). Sample pulled on weekly basis - 0 rejects allowed out of 45 devices after 30 cycles; 1 reject allowed out of 45 devices after 1000 cycles.

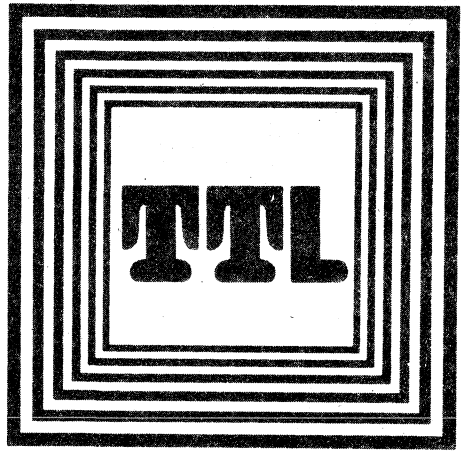
3.3 **Op. Life Text** - MIL-STD-883, Method 1005, Condition A (Reverse Bias) or C (Power plus Reverse Bias), T_A = 145°C; readouts at 40 hrs and 250 hrs (plastic and hermetic packages). Sample pulled on weekly basis - 1 reject allowed out of 55 devices at 40 hr readout. No additional rejects allowed at 250 hrs. If no rejects at 40 hrs, 1 reject allowed at 250 hrs.

3.4 **Report** - Monthly QA Data Base computer printout summarizing test results.

NOTES:

1. All standard 48A Group A parameters will be measured Go/No/Go at each readout.
2. Any indicated failure is first verified (R&R) and then submitted to the Product Analysis Lab for detailed analysis.
3. If both plastic and hermetic packages are available, package type will be alternated weekly.
4. Device types sampled will be by generic type within each digital I/C product family (MDTL, MTTL, MTTL-LS, etc.) and will include all major package assembly options (U/S bond, TC bond, ball bond, M.E.S.A., etc.) and all assembly locations (Korea, Malaysia, etc.).
5. 16 hrs PTHB is equivalent to approximately 800 hrs of 85°C/85% RH THB for $V_{CC} \leqslant 15$ V.
6. Only moisture related failures (like corrosion) are criteria for failure on PTHB test.
7. 40 hr/145°C Op Life is equivalent to 160 hr/125°C using 1.0eV in Arrhenius equation.
8. 250 hrs/145°C Op Life is equivalent to 1000 hrs/125°C using 1.0eV in Arrhenius equation.
9. Special device specifications (48A's) for digital products will reference 12MRM15301A as source of generic data for any customer required monthly audit reports.

LOW POWER SCHOTTKY



Ordering Information and Package Outlines

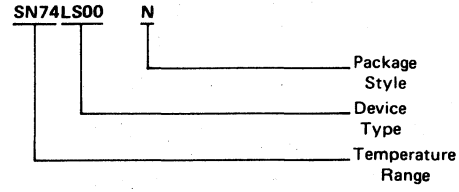
LOW POWER SCHOTTKY ORDERING INFORMATION AND PACKAGE OUTLINES

TEMPERATURE RANGE

54LS = Military −55°C to +125°C
74LS = Commercial 0°C to +70°C

PACKAGE STYLE

J = Dual In-Line — Ceramic (Hermetic)
N = Dual In-Line — Plastic
W = Flat Package



In order to accommodate varying die sizes (SSI, MSI, etc.), numbers of pins (14, 16, 24, etc.), and package outlines, a number of different package forms are required in each of the three package style categories.

The following lists indicate the specific package codes currently used for each device type. The detailed outline dimensions corresponding to each package code is shown at the end of this section.

DEVICE	MILITARY (54LS) −55°C to +125°C		DEVICE	COMMERCIAL (74LS) INDUSTRIAL 0°C to +70°C		
	CERAMIC DIP (J)	FLATPAK (W)		CERAMIC DIP (J)	PLASTIC DIP (N)	FLATPAK (W)
54LS00	632	717	74LS00	632	646	717
54LS01	632	717	74LS01	632	646	717
54LS02	632	717	74LS02	632	646	717
54LS03	632	717	74LS03	632	646	717
54LS04	632	717	74LS04	632	646	717
54LS05	632	717	74LS05	632	646	717
54LS08	632	717	74LS08	632	646	717
54LS09	632	717	74LS09	632	646	717
54LS10	632	717	74LS10	632	646	717
54LS11	632	717	74LS11	632	646	717
54LS12	632	717	74LS12	632	646	717
54LS13	632	717	74LS13	632	646	717
54LS14	632	717	74LS14	632	646	717
54LS15	632	717	74LS15	632	646	717
54LS20	632	717	74LS20	632	646	717
54LS21	632	717	74LS21	632	646	717
54LS22	632	717	74LS22	632	646	717
54LS26	632	717	74LS26	632	646	717
54LS27	632	717	74LS27	632	646	717

DEVICE	MILITARY (54LS) −55°C to +125°C		DEVICE	COMMERCIAL (74LS) INDUSTRIAL 0°C to +70°C		
	CERAMIC DIP (J)	FLATPAK (W)		CERAMIC DIP (J)	PLASTIC DIP (N)	FLATPAK (W)
54LS28	632	717	74LS28	632	646	717
54LS30	632	717	74LS30	632	646	717
54LS32	632	717	74LS32	632	646	717
54LS33	632	717	74LS33	632	646	717
54LS37	632	717	74LS37	632	646	717
54LS38	632	717	74LS38	632	646	717
54LS40	632	717	74LS40	632	646	717
54LS42	620	650	74LS42	620	648	650
54LS47	620	650	74LS47	620	648	650
54LS48	620	650	74LS48	620	648	650
54LS49	620	650	74LS49	620	648	650
54LS51	632	717	74LS51	632	646	717
54LS54	632	717	74LS54	632	646	717
54LS55	632	717	74LS55	632	646	717
54LS73A	632	717	74LS73A	632	646	717
54LS74A	632	717	74LS74A	632	646	717
54LS75	620	650	74LS75	620	648	650
54LS76A	620	650	74LS76A	620	648	650
54LS77	632	717	74LS77	632	646	717
54LS78A	632	717	74LS78A	632	646	717
54LS83A	620	650	74LS83A	620	648	650
54LS86	632	717	74LS86	632	646	717
54LS89	620	650	74LS89	620	648	650
54LS90	632	717	74LS90	632	646	717
54LS92	632	717	74LS92	632	646	717
54LS93	632	717	74LS93	632	646	717
54LS95B	632	717	74LS95B	632	646	717
54LS107A	632	717	74LS107A	632	646	717
54LS109A	620	650	74LS109A	620	648	650
54LS112A	620	650	74LS112A	620	648	650
54LS113A	632	717	74LS113A	632	646	717
54LS114A	632	717	74LS114A	632	646	717
54LS122	632	717	74LS122	632	646	717
54LS123	620	650	74LS123	620	648	650
54LS124	620	650	74LS124	620	648	650
54LS125A	632	717	74LS125A	632	646	717
54LS126A	632	717	74LS126A	632	646	717
54LS132	632	717	74LS132	632	646	717
54LS133	620	650	74LS133	620	648	650
54LS136	632	717	74LS136	632	646	717
54LS138	620	650	74LS138	620	648	650
54LS139	620	650	74LS139	620	648	650
54LS145	620	650	74LS145	620	648	650
54LS151	620	650	74LS151	620	648	650
54LS153	620	650	74LS153	620	648	650
54LS155	620	650	74LS155	620	648	650
54LS156	620	650	74LS156	620	648	650
54LS157	620	650	74LS157	620	648	650
54LS158	620	650	74LS158	620	648	650

DEVICE	MILITARY (54LS) −55°C to +125°C		DEVICE	COMMERCIAL (74LS) INDUSTRIAL 0°C to +70°C		
	CERAMIC DIP (J)	FLATPAK (W)		CERAMIC DIP (J)	PLASTIC DIP (N)	FLATPAK (W)
54LS160A	620	650	74LS160A	620	648	650
54LS161A	620	650	74LS161A	620	648	650
54LS162A	620	650	74LS162A	620	648	650
54LS163A	620	650	74LS163A	620	648	650
54LS164	632	717	74LS164	632	646	717
54LS165	620	650	74LS165	620	648	650
54LS168	620	650	74LS168	620	648	650
54LS169	620	650	74LS169	620	648	650
54LS170	620	650	74LS170	620	648	650
54LS173	620	650	74LS173	620	648	650
54LS174	620	650	74LS174	620	648	650
54LS175	620	650	74LS175	620	648	650
54LS181	623	652	74LS181	623	649	652
54LS182	620	650	74LS182	620	648	650
54LS189	620	650	74LS189	620	648	650
54LS190	620	650	74LS190	620	648	650
54LS191	620	650	74LS191	620	648	650
54LS192	620	650	74LS192	620	648	650
54LS193	620	650	74LS193	620	648	650
54LS194A	620	650	74LS194A	620	648	650
54LS195A	620	650	74LS195A	620	648	650
54LS196	632	717	74LS196	632	646	717
54LS197	632	717	74LS197	632	646	717
54LS221	620	650	74LS221	620	648	650
54LS240	732	737	74LS240	732	738	737
54LS241	732	737	74LS241	732	738	737
54LS242	632	717	74LS242	632	646	717
54LS243	632	717	74LS243	632	646	717
54LS244	732	737	74LS244	732	738	737
54LS245	732	737	74LS245	732	738	737
54LS247	620	650	74LS247	620	648	650
54LS248	620	650	74LS248	620	648	650
54LS249	620	650	74LS249	620	648	650
54LS251	620	650	74LS251	620	648	650
54LS253	620	650	74LS253	620	648	650
54LS256	620	650	74LS256	620	648	650
54LS257A	620	650	74LS257A	620	648	650
54LS258A	620	650	74LS258A	620	648	650
54LS259	620	650	74LS259	620	648	650
54LS260	632	717	74LS260	632	646	717
54LS266	632	717	74LS266	632	646	717
54LS273	732	737	74LS273	732	738	737
54LS279	620	650	74LS279	620	648	650
54LS280	632	717	74LS280	632	646	717
54LS283	620	650	74LS283	620	648	650
54LS289	620	650	74LS289	620	648	650

DEVICE	MILITARY (54LS) −55°C to +125°C		DEVICE	COMMERCIAL (74LS) INDUSTRIAL 0°C to +70°C		
	CERAMIC DIP (J)	FLATPAK (W)		CERAMIC DIP (J)	PLASTIC DIP (N)	FLATPAK (W)
54LS290	632	717	74LS290	632	646	717
54LS293	632	717	74LS293	632	646	717
54LS295A	632	717	74LS295A	632	646	717
54LS298	620	650	74LS298	620	648	650
54LS299	732	737	74LS299	732	738	737
54LS322	732	737	74LS322	732	738	737
54LS323	732	737	74LS323	732	738	737
54LS324	632	717	74LS324	632	646	717
54LS325	620	650	74LS325	620	648	650
54LS326	620	650	74LS326	620	648	650
54LS327	632	717	74LS327	632	646	717
54LS352	620	650	74LS352	620	648	650
54LS353	620	650	74LS353	620	648	650
54LS365A	620	650	74LS365A	620	648	650
54LS366A	620	650	74LS366A	620	648	650
54LS367A	620	650	74LS367A	620	648	650
54LS368A	620	650	74LS368A	620	648	650
54LS373	732	737	74LS373	732	738	737
54LS374	732	737	74LS374	732	738	737
54LS375	620	650	74LS375	620	648	650
54LS377	732	737	74LS377	732	738	737
54LS378	620	650	74LS378	620	648	650
54LS379	620	650	74LS379	620	648	650
54LS384	620	650	74LS384	620	648	650
54LS385	732	737	74LS385	732	738	737
54LS386	632	717	74LS386	632	646	717
54LS390	620	650	74LS390	620	648	650
54LS393	632	717	74LS393	632	646	717
54LS395A	620	650	74LS395A	620	648	650
54LS398	732	737	74LS398	732	738	737
54LS399	620	650	74LS399	620	648	650
54LS490	620	650	74LS490	620	648	650
54LS502	620	650	74LS502	620	648	650
54LS503	620	650	74LS503	620	648	650
54LS504	623	652	74LS504	623	649	652
54LS540	732	737	74LS540	732	738	737
54LS541	732	737	74LS541	732	738	737
54LS568	732	737	74LS568	732	738	737
54LS569	732	737	74LS569	732	738	737
54LS573	732	737	74LS573	732	738	737
54LS574	732	737	74LS574	732	738	737
54LS640	732	737	74LS640	732	738	737
54LS641	732	737	74LS641	732	738	737
54LS642	732	737	74LS642	732	738	737
54LS645	732	737	74LS645	732	738	737
54LS670	620	650	74LS670	620	648	650

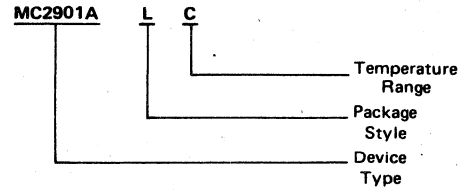
MOTOROLA 2900 MICROPROCESSOR FAMILY

TEMPERATURE RANGE

M = Military −55°C to +125°C
C = Commercial 0°C to +70°C

PACKAGE STYLE

L = Dual In-Line-Ceramic
P = Dual In-Line-Plastic
F = Flat Package



DEVICE	MILITARY (M) −55°C to +125°C		DEVICE	COMMERCIAL (C) 0°C to +70°C		
	CERAMIC DIP (L)	FLATPAK (F)		CERAMIC DIP (L)	PLASTIC DIP (P)	FLATPAK (F)
2901A–M	734	735	2901A–C	734	–	735
2902 –M	620	650	2902 –C	620	648	650
2903 –M	*	*	2903 –C	*	*	*
2905 –M	623	652	2905 –C	623	649	652
2906 –M	623	652	2906 –C	623	649	652
2907 –M	732	737	2907 –C	732	738	737
2909 –M	733	–	2909 –C	733	710	–
2910 –M	734	735	2910 –C	734	–	735
2911 –M	732	737	2911 –C	732	738	737
2915A–M	623	652	2915A–C	623	649	652
2916A–M	623	652	2916A–C	623	649	652
2917A–M	732	737	2917A–C	732	738	737
2918 –M	620	650	2918 –C	620	648	650
82100–M	733	–	82100–C	733	710	–
82101–M	733	–	82101–C	733	710	–

*48 pin package

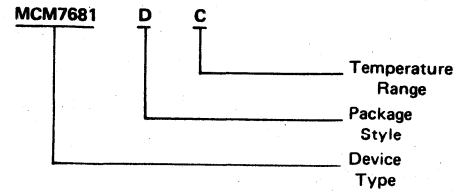
MOTOROLA PROM AND RAM TTL MEMORIES

TEMPERATURE RANGE

M = Military −55°C to +125°C
C = Commercial 0°C to +70°C

PACKAGE STYLE

D = Dual In-Line-Ceramic
P = Dual In-Line-Plastic
F = Flat Package



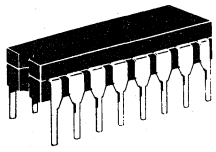
DEVICE	MILITARY −55°C to +125°C		DEVICE	COMMERCIAL 0°C to +70°C		
	CERAMIC DIP (D)	FLATPAK (F)		CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
5303	623	–	5003	623	–	–
5304	623	–	5004	623	–	–
7620 –M	620	–	7620 –C	620	–	–
7621 –M	620	–	7621 –C	620	–	–
7640 –M	623	–	7640 –C	623	–	–
7641 –M	623	–	7641 –C	623	–	–
7642 –M	726	–	7642 –C	726	–	–
7643 –M	726	–	7643 –C	726	–	–
7680 –M	623	–	7680 –C	623	–	–
7681 –M	623	–	7681 –C	623	–	–
7684 –M	726	–	7684 –C	726	–	–
7685 –M	726	–	7685 –C	726	–	–
7686 –M	732	–	7686 –C	732	–	–
7687 –M	732	–	7687 –C	732	–	–
82707–M	623	–	82707–C	623	–	–
82708–M	623	–	82708–C	623	–	
93415–M	620	650	93415–C	620	648	650
93425–M	620	650	93425–C	620	648	650
93422–M	*	*	93422–C	*	*	*

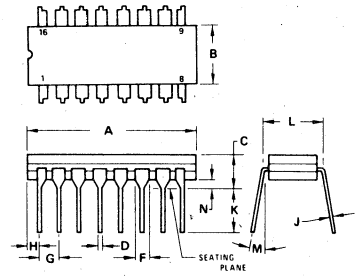
*22 pin package

PACKAGE OUTLINES

CERAMIC DUAL IN-LINE

Case 620-06
16-Pin Ceramic Dual In-Line

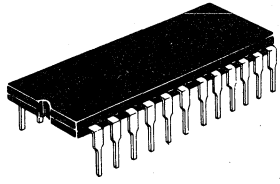


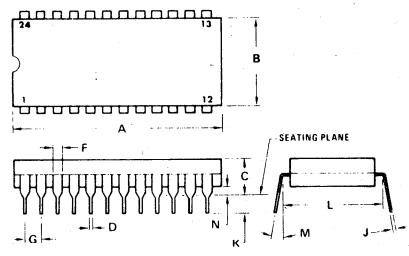


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	5.08	0.125	0.200
L	7.49	8.89	0.295	0.350
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "A" AND "B" (620-06) DO NOT INCLUDE GLASS RUN-OUT.
4. DIM "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW BODY).

Case 623-03
24-Pin Ceramic Dual In-Line

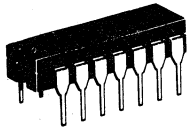


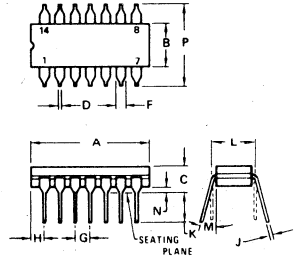


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.29	4.06	0.090	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL)

Case 632-06
14-Pin Ceramic Dual In-Line





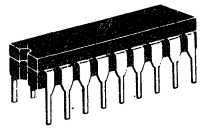
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.58	0.015	0.023
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	1.91	2.29	0.075	0.090
J	0.20	0.38	0.008	0.015
K	3.18	5.08	0.125	0.200
L	7.49	8.89	0.295	0.350
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

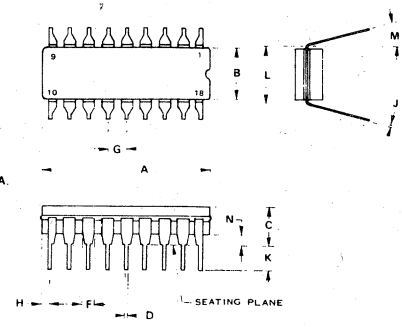
NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH MO-001 AA OUTLINE SHALL APPLY
2. DIMENSION "A" AND "B" (632-06) DO NOT INCLUDE GLASS RUN-OUT
3. DIMENSION "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW BODY) (632-06)

PACKAGE OUTLINES

CERAMIC DUAL IN-LINE (continued)

Case 726-01
18-Pin Ceramic Dual In-Line

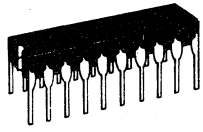


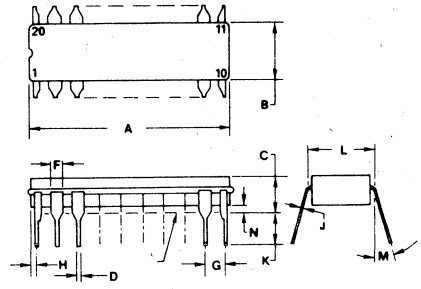


NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.63	7.24	0.261	0.285
C	–	5.08	–	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.76	1.02	0.030	0.040
J	0.13	0.38	0.005	0.015
K	–	4.44	–	0.175
L	7.37	8.00	0.290	0.315
M	0°	15°	0°	15°
N	0.51	0.76	0.020	0.030

Case 732-02
20-Pin Ceramic Dual In-Line

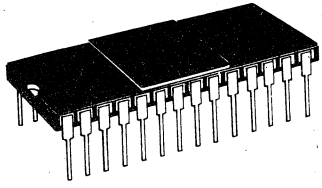


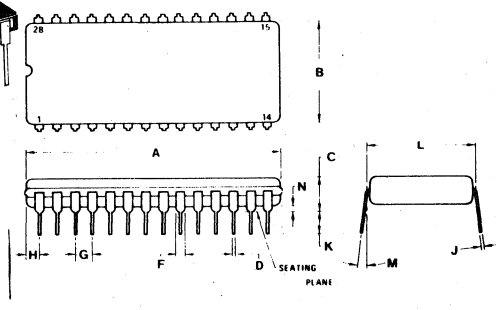


NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA , TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	24.38	25.15	0.960	0.990
B	6.86	7.49	0.270	0.295
C	4.32	5.08	0.170	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	5°	15°	5°	15°
N	0.51	0.76	0.020	0.030

Case 733-01
28-Pin Ceramic Dual In-Line





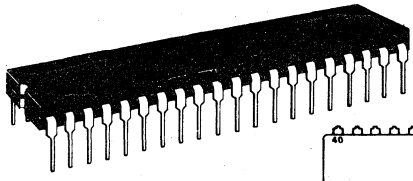
NOTES
1. LEADS WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION OF SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL
3. DIM A AND B INCLUDES MENISCUS

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.83	37.59	1.450	1.480
B	12.70	13.46	0.500	0.530
C	5.08	5.84	0.200	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54	BSC	0.100	BSC
H	2.03	2.29	0.080	0.090
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24	BSC	0.600	BSC
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

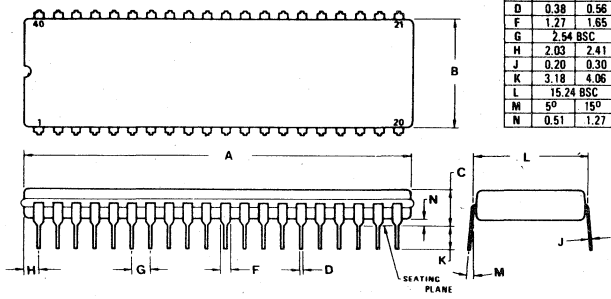
PACKAGE OUTLINES

CERAMIC DUAL IN-LINE (continued)

Case 734-01
40-Pin Ceramic Dual In-Line



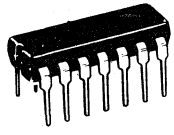
NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.



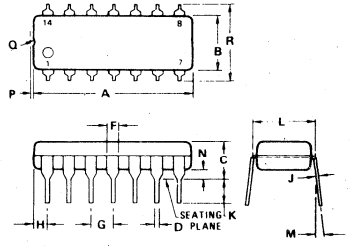
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	52.32	53.09	2.060	2.090
B	12.70	13.72	0.500	0.540
C	5.08	5.84	0.200	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
H	2.03	2.41	0.080	0.095
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

PLASTIC

Case 646-04
14-Pin Plastic

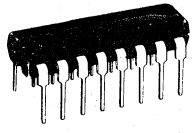


NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. DIMENSION "R" TO BE MEASURED AT THE TOP OF THE LEADS (NOT AT THE TIPS).

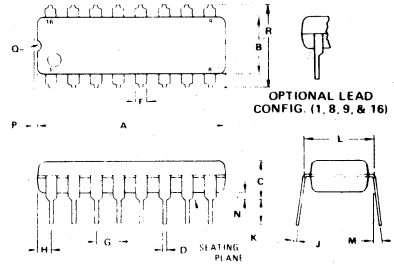


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.03	19.56	0.710	0.770
B	6.10	6.60	0.240	0.260
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	–	0.115	–
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	–	0.020	–
R	–	8.26	–	0.325

Case 648-04
16-Pin Plastic



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. DIMENSION "R" TO BE MEASURED AT THE TOP OF THE LEADS (NOT AT THE TIPS).

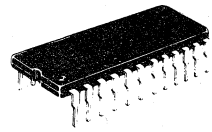


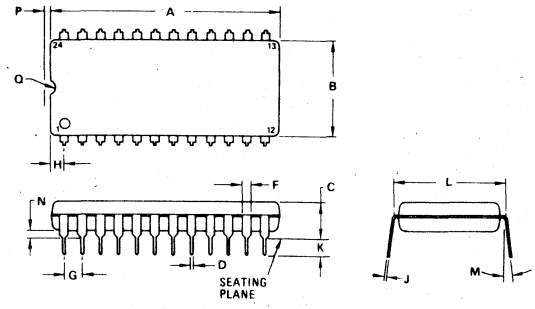
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	22.10	–	0.870
B	6.10	6.60	0.240	0.260
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F		1.78	–	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	–	0.115	–
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51		0.020	–
R	–	8.26	–	0.325

PACKAGE OUTLINES

PLASTIC (continued)

Case 649-03
24-Pin Plastic

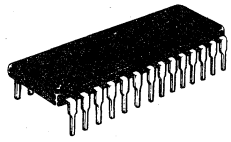


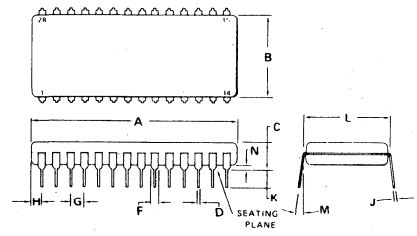


NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

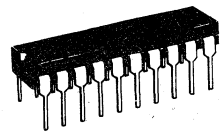
Case 710-01
28-Pin Plastic

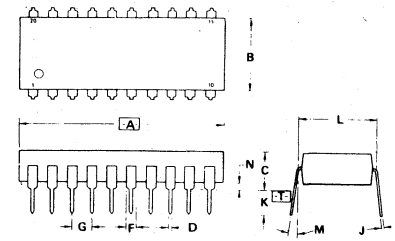




DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.32	37.34	1.430	1.470
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	14.99	15.49	0.590	0.610
M	0^0	10^0	0^0	10^0
N	0.51	1.02	0.020	0.040

Case 738-01
20-Pin Plastic





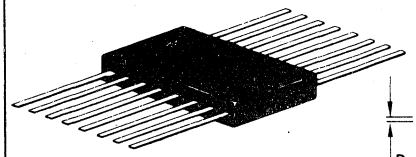
NOTES:
1. DIM [A] IS DATUM.
2. POSITIONAL TOL FOR LEADS.
   [⌖] [Ø 0.25 (0.010) Ⓜ] [T] [A Ⓜ]
3. [T] IS SEATING PLANE.
4. DIM "B" DOES NOT INCLUDE MOLD FLASH.
5. DIM [L] TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.65	27.18	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.94	4.19	0.155	0.165
D	0.38	0.56	0.015	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	2.79	3.56	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0^0	15^0	0^0	15^0
N	0.51	1.02	0.020	0.040

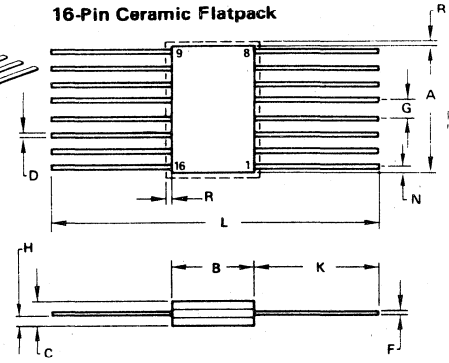
PACKAGE OUTLINES

CERAMIC FLATPACK

Case 650-03
16-Pin Ceramic Flatpack

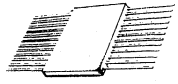


NOTES:
1. LEAD NO. 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
2. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

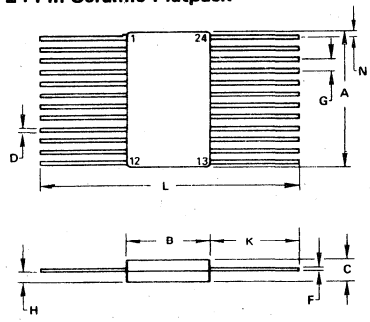


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.22	7.24	0.245	0.285
C	1.52	2.03	0.060	0.080
D	0.41	0.48	0.016	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.64	0.89	0.025	0.035
K	6.35	9.40	0.250	0.370
L	18.92	–	0.745	–
N	–	0.51	–	0.020
R	–	0.38	–	0.015

Case 652-02
24-Pin Ceramic Flatpack

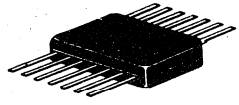


NOTES:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

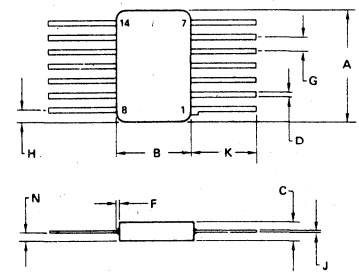


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.99	15.49	0.590	0.610
B	9.27	9.91	0.365	0.390
C	1.27	2.03	0.050	0.080
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.69	1.02	0.027	0.040
K	6.35	9.40	0.250	0.370
L	21.97	–	0.865	–
N	0.25	0.63	0.010	0.025

Case 717-01
14-Pin Ceramic Flatpack



NOTE:
1. DIM "F" IS FOR GLASS OVERRUN.
2. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA TO DIM "A" & "B" AT MAXIMUM MATERIAL CONDITION.

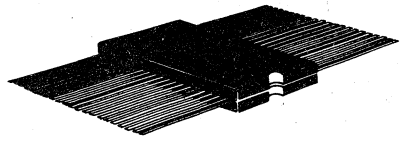


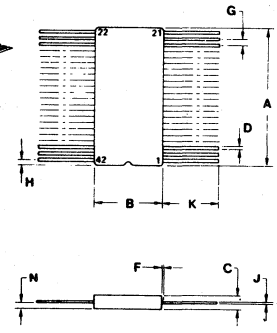
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	9.91	–	0.390
B	–	6.73	–	0.265
C	–	2.03	0.060	0.080
D	0.38	0.48	0.015	0.019
F	–	0.25	–	0.010
G	1.27 BSC		0.050 BSC	
H	0.89	1.14	0.035	0.045
J	0.08	0.15	0.003	0.006
K	–	8.26	–	0.325
N	0.64	0.89	0.025	0.035

PACKAGE OUTLINES

CERAMIC FLATPACK (continued)

Case 735-02
42-Pin Ceramic Flatpack

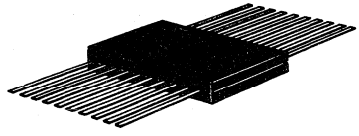


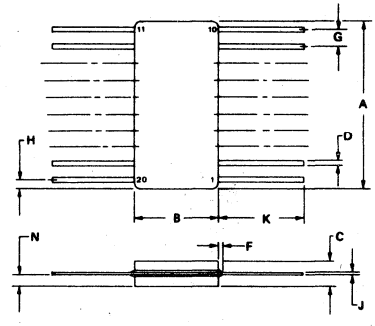


NOTE:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	26.92	27.60	1.060	1.090
B	13.72	14.22	0.540	0.560
C	2.41	3.18	0.095	0.125
D	0.43	0.53	0.017	0.023
F	–	0.38	–	0.015
G	1.27 BSC		0.050 BSC	
H	0.89	1.14	0.035	0.045
J	0.20	0.30	0.008	0.012
K	–	11.94	–	0.470
N	–	1.27	–	0.050

Case 737-01
20-Pin Ceramic Flatpack





NOTE:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	13.08	–	0.515
B	5.84	6.60	0.230	0.260
C	1.52	2.16	0.060	0.085
D	0.41	0.46	0.016	0.018
F	–	0.25	–	0.010
G	1.27 BSC		0.050 BSC	
H	1.14	1.40	0.045	0.055
J	0.08	0.13	0.003	0.005
K	–	9.14	–	0.360
N	–	1.02	–	0.040

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